HVCMOS Sensors for CEPC

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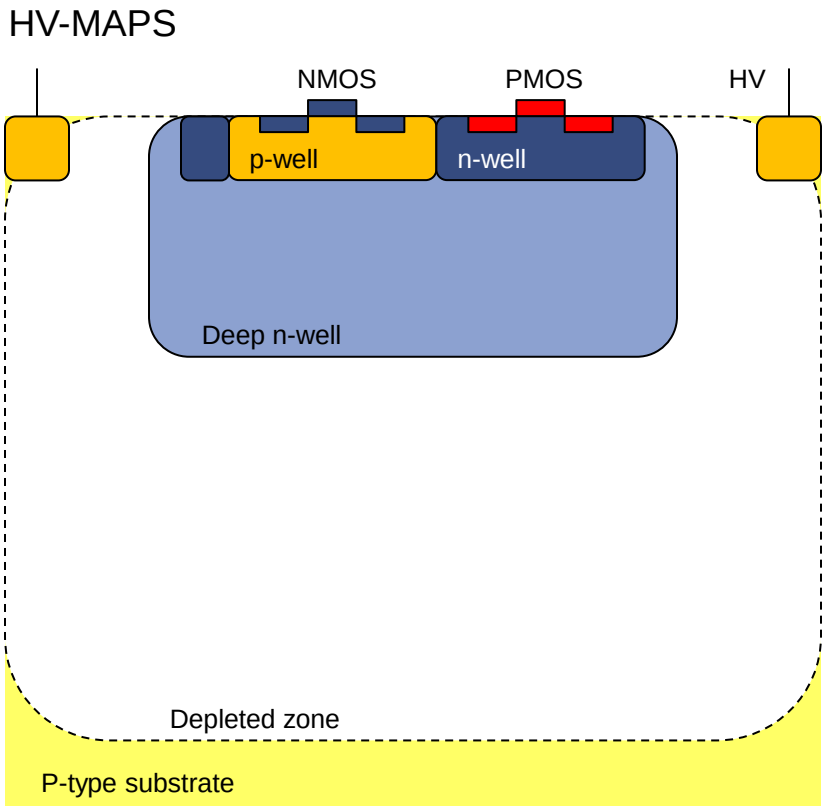
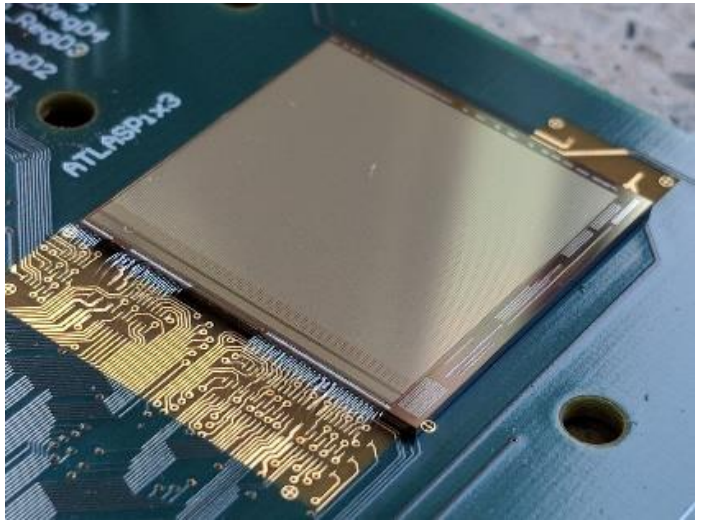
- for KIT CEPCE team
- Ivan Peric, Rudolf Schimassek und Hui Zhang
- New Postdoc Ruoshi Dong should join in 2022 – his position is funded by OCPC

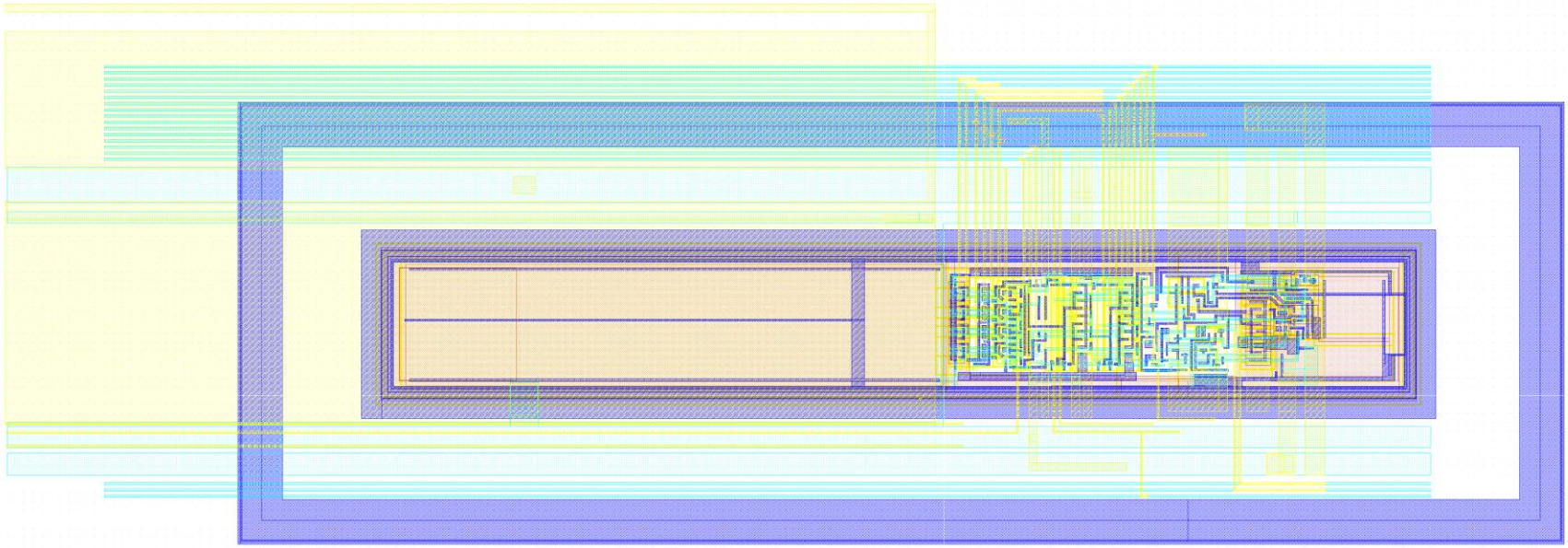
- HV-CMOS sensors
- Pixel is based on a deep n well with electronics inside
- Charge collection by drift, short drift distance
- Good time resolution
- Radiation tolerant
- Can be thin
- Use of commercial technology with customized substrates and deep p-well implant (quadruple well process)
- Substrates from 300Ωcm to ~20kΩcm (uniformly doped)
- Commercial technology, not expensive



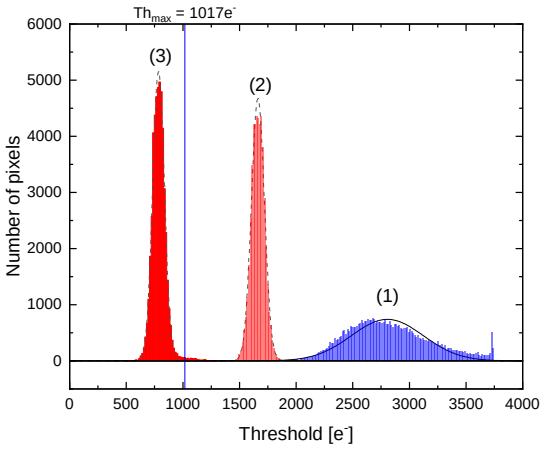
- ATLASPIX3 sensor was originally developed for ATLAS, it is now used as technology demonstrator for HVCMOS, several sensors are based on ATLASPIX3 design
- Features pixels of 50µm x 150µm
- Pixels contain amplifiers and comparator with threshold tune circuit
- Chip size 2.2 cm x 2.0 cm
- Matrix size 132 x 372
- Comparator is NMOS only
- Triggered and unteiggered readout
- Data output 1.28 Gbit/s 64b66b, or 1.6 Gbit/2 8b10b
- Serial powering
- Clock data recovery from command in
- Power consumption 140mW/cm^2

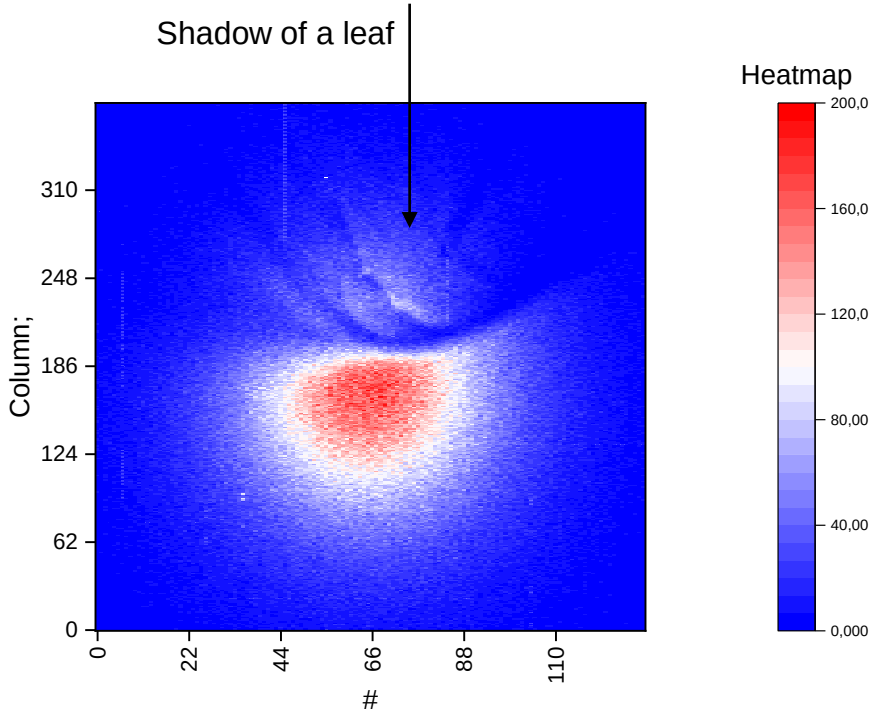


I. Peric et al., High-Voltage CMOS Active Pixel Sensor, IEEE JSSC, Volume: 56, Issue: 8, Aug. 2021
https://ieeexplore.ieee.org/document/9373986

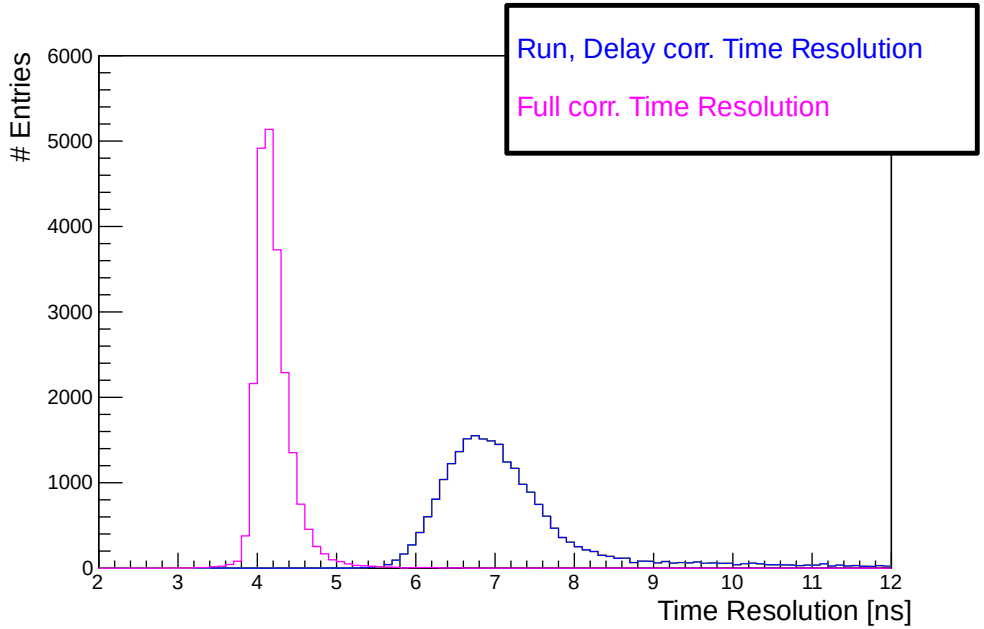


- Some results with ATLASPIX3
- Threshold can be tuned to 800e, threshold dispersion 60e, noise around 70e
- Example: ^{55}Fe source measurement

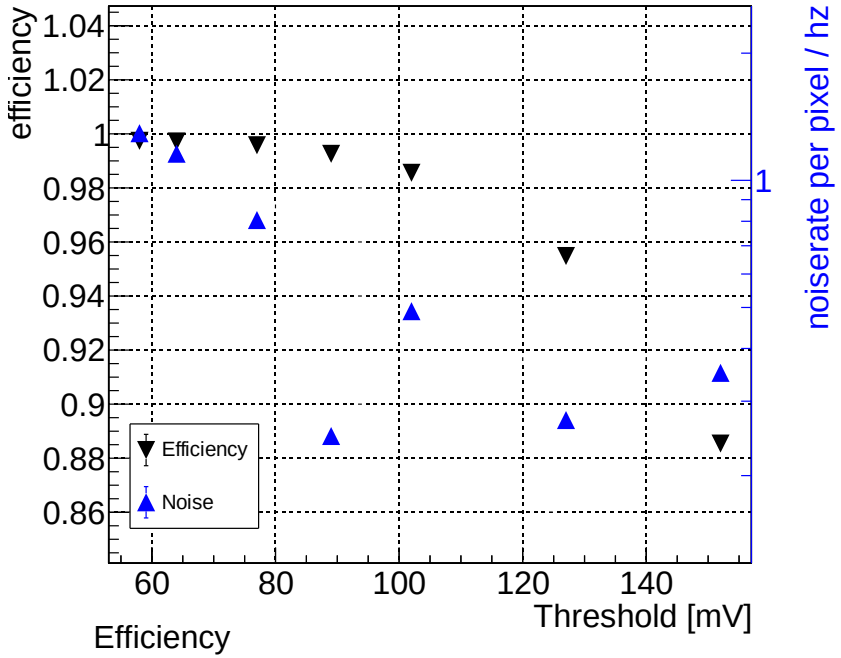




- Time resolution and efficiency measured in PSI test beam (Dohun Kim and Heidelberg team)

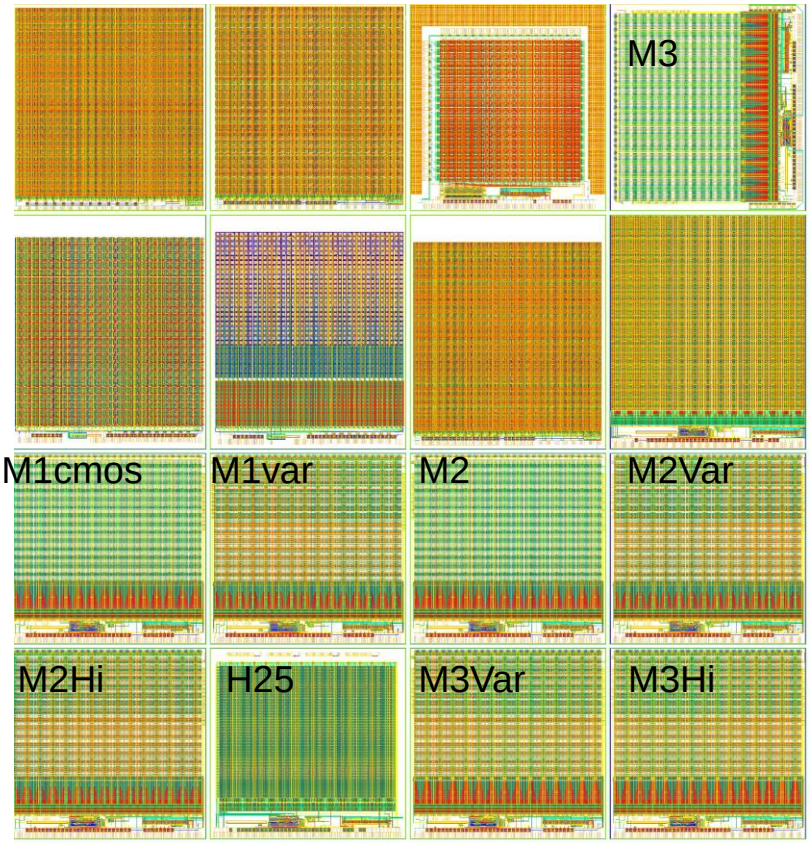


Time resolution (RMS) for every pixel
Uncorrected 6.7ns +- 0.5ns
ToT corrected 4.1ns +- 0.1



Efficiency

- Improvements for tracking detectors for electron colliders
- Run 2020 and 2021
- Designs for CLIC, CEPC, DESY telescope upgrade (TELEPIX)
- Pixels 25µm X 165µm (layout)



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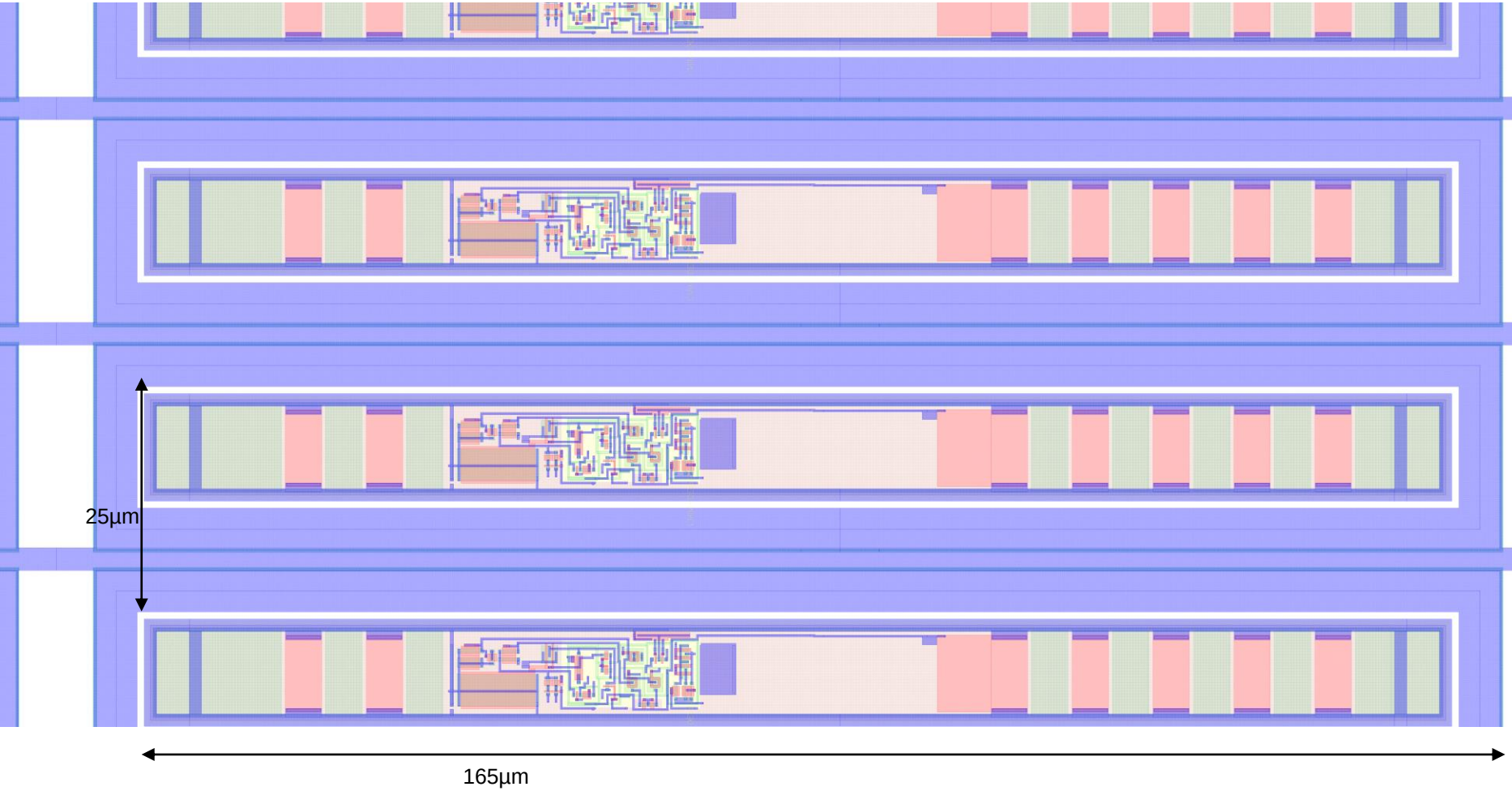
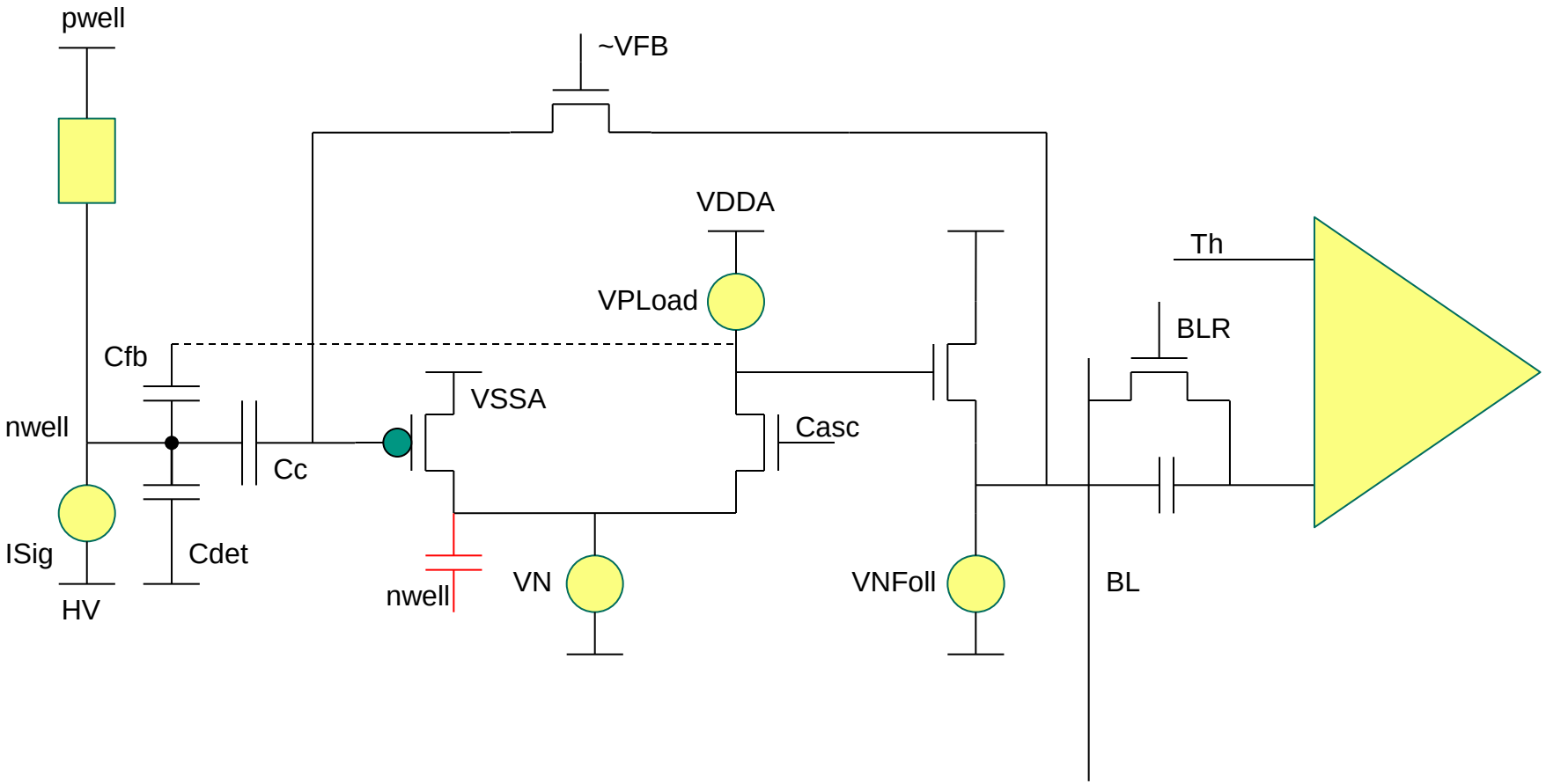

25µm
165µm

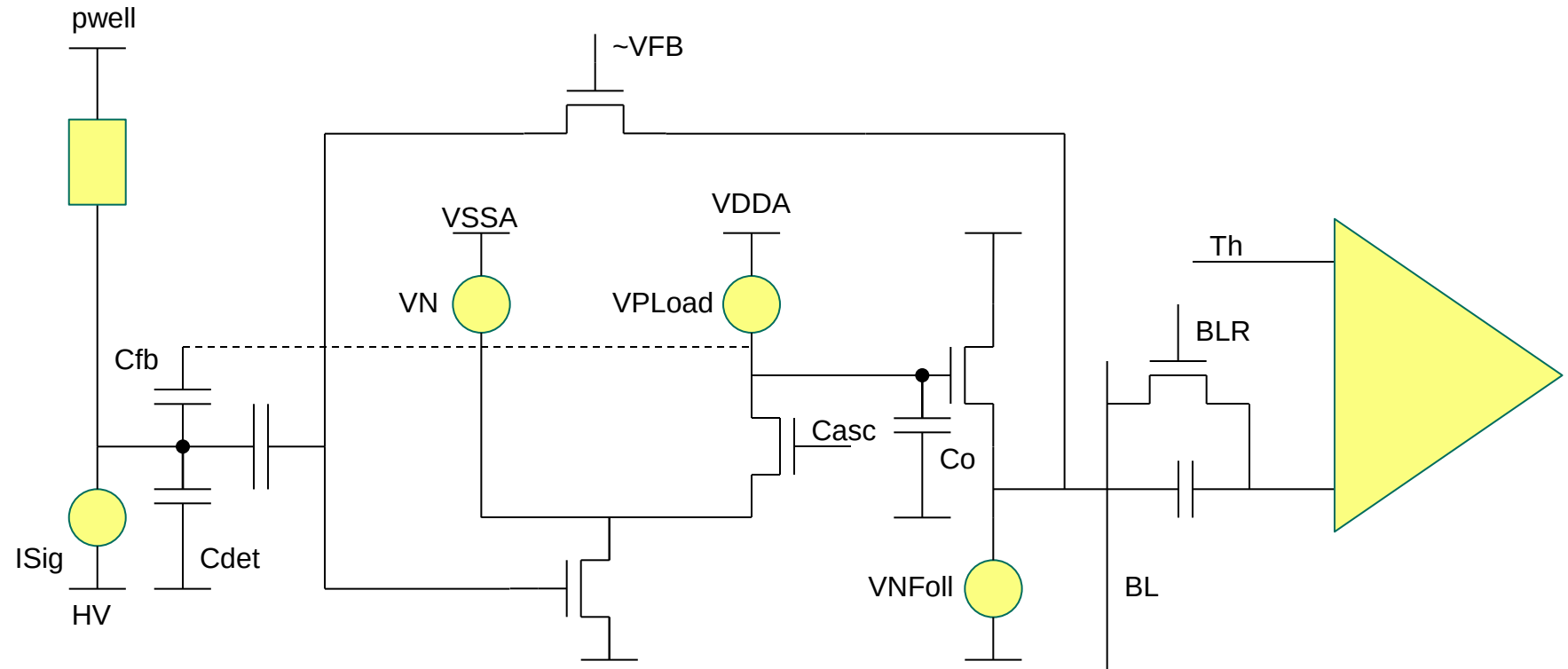
Sensor Prototypes for EC - Improvements

- Improved breakdown voltage by better design of guard ring (60V -> 120V)
- Reduction of power consumption by optimized amplifier and comparator designs

- PMOS amplifier
- Standard amplifier – behaves well



- NMOS amplifier
- Should be faster at small bias current, has higher gain (transconductance g_m)



$$T_r = \frac{C_{det} C_o}{C_{fb} g_m}$$

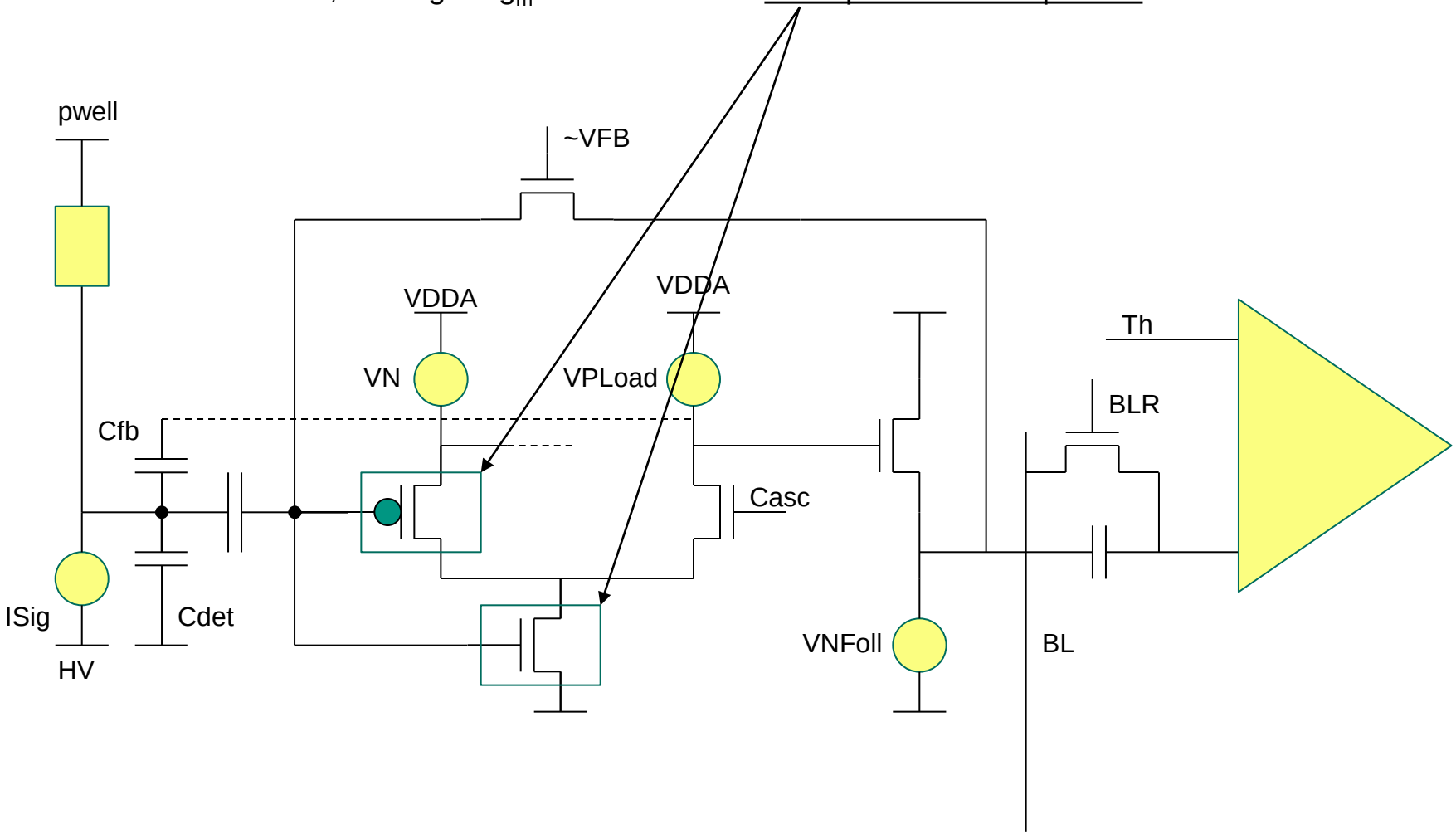
$$g_m = \sqrt{2 I \mu C_{ox} \frac{W}{L}}$$

Strong inversion

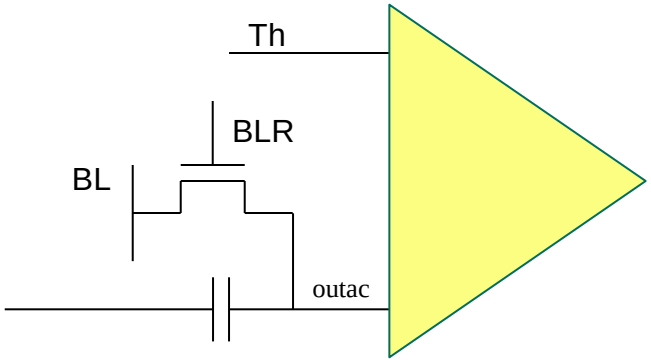
$$g_m = \frac{I}{n U_T}$$

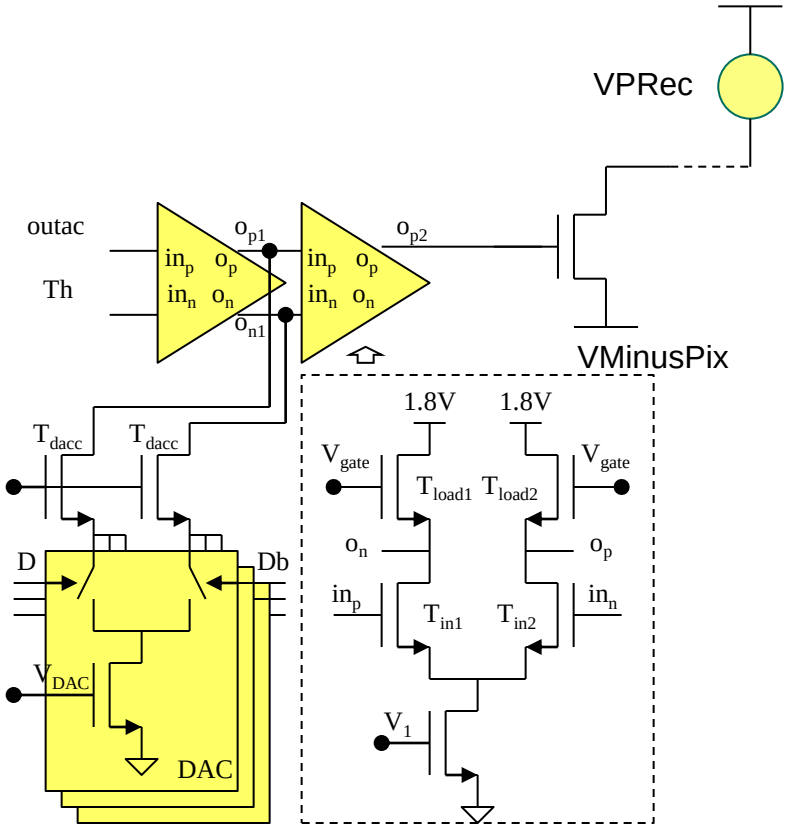
Weak inversion

- CMOS amplifier
- Combination of both, has higher g_m because it uses <u>two input devices in parallel</u>

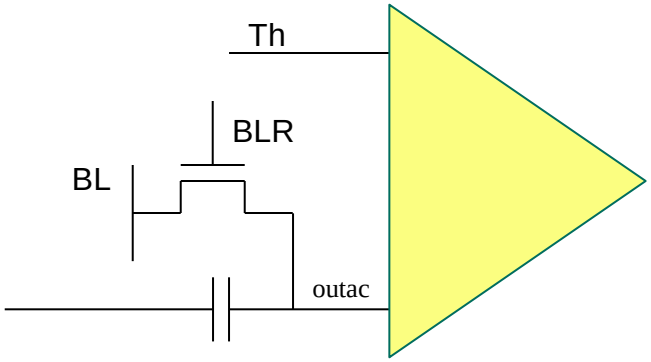


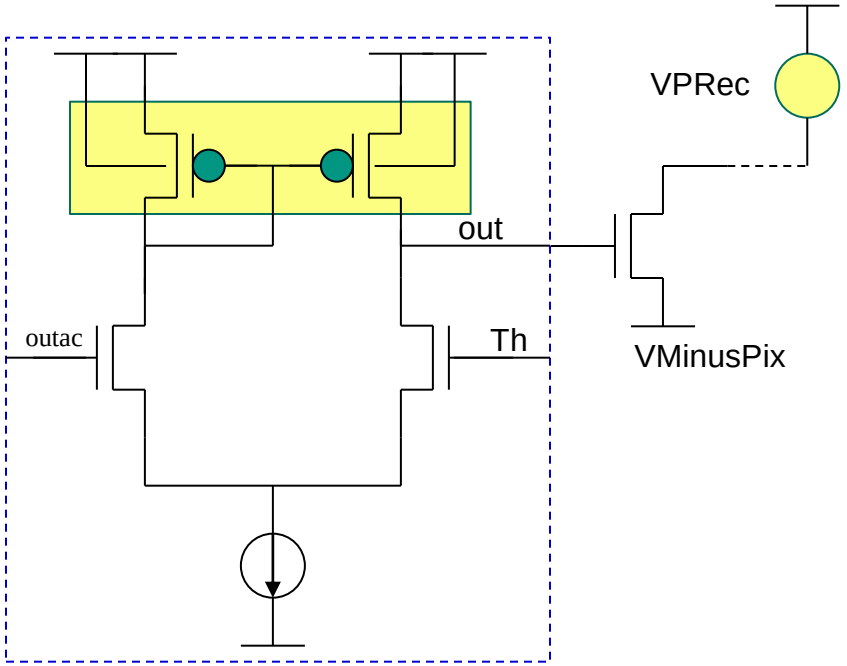
- NMOS comparator
- Standard – does not need deep p-well, used in ATLASPIX3
- Drawback, requires larger DC bias current



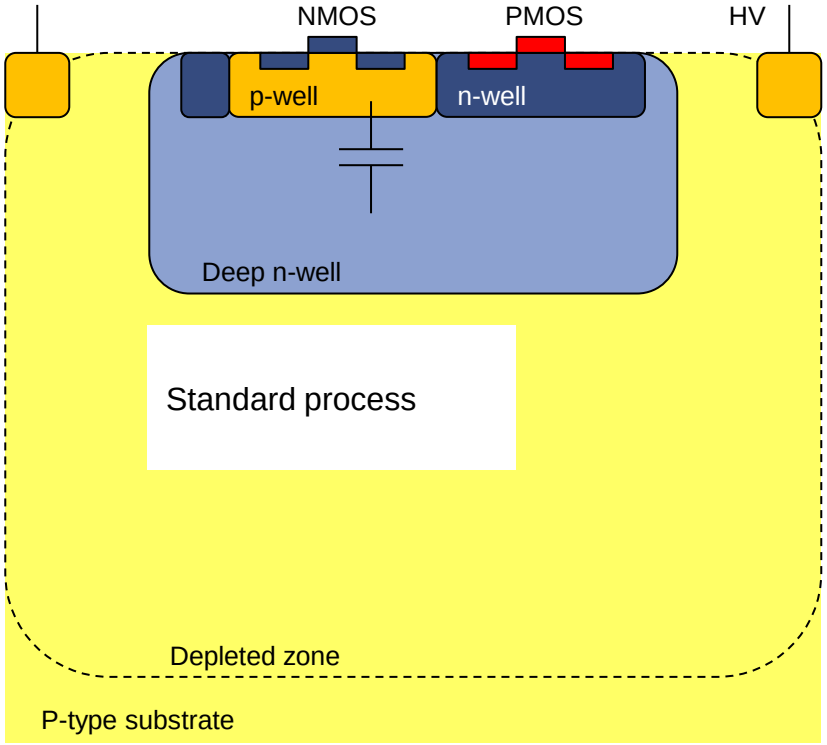


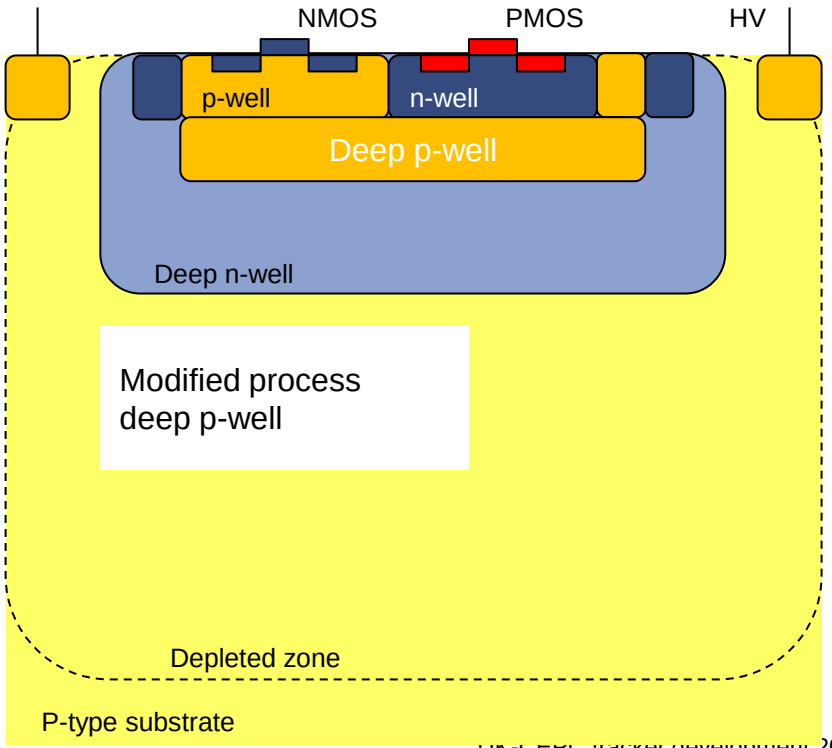
- CMOS comparator
- Needs deep p-well
- Works with smaller bias current



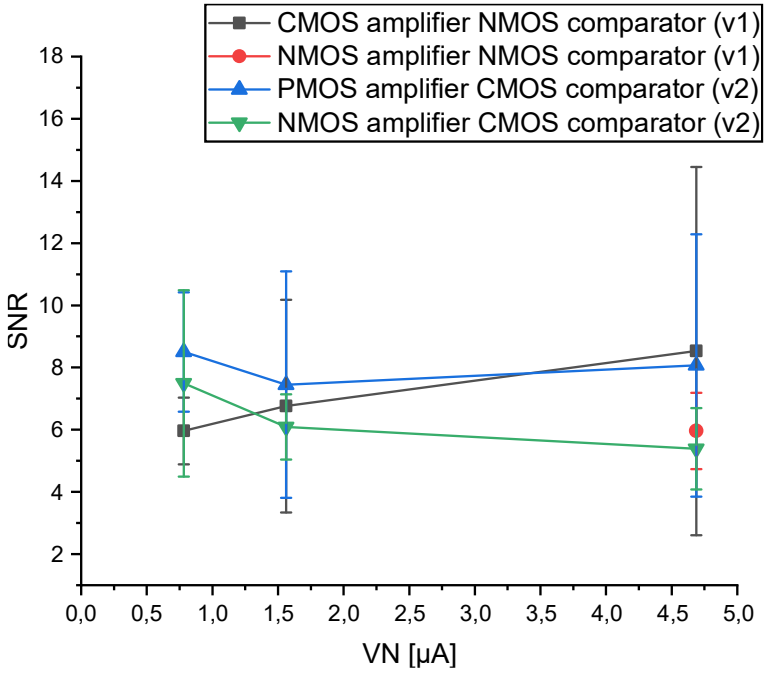


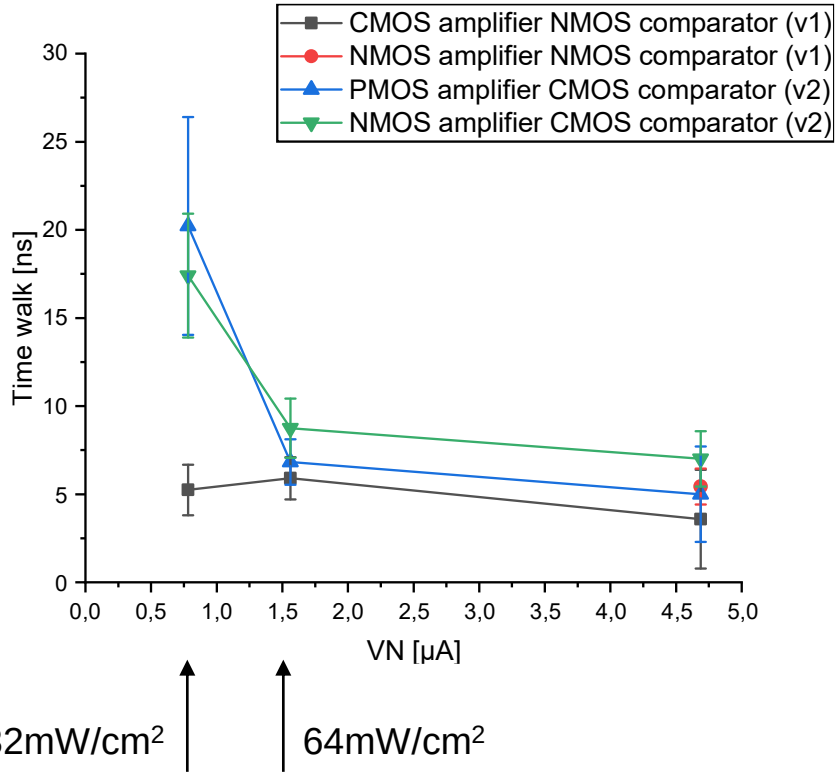
- Deep p-Well was introduced for this sensor





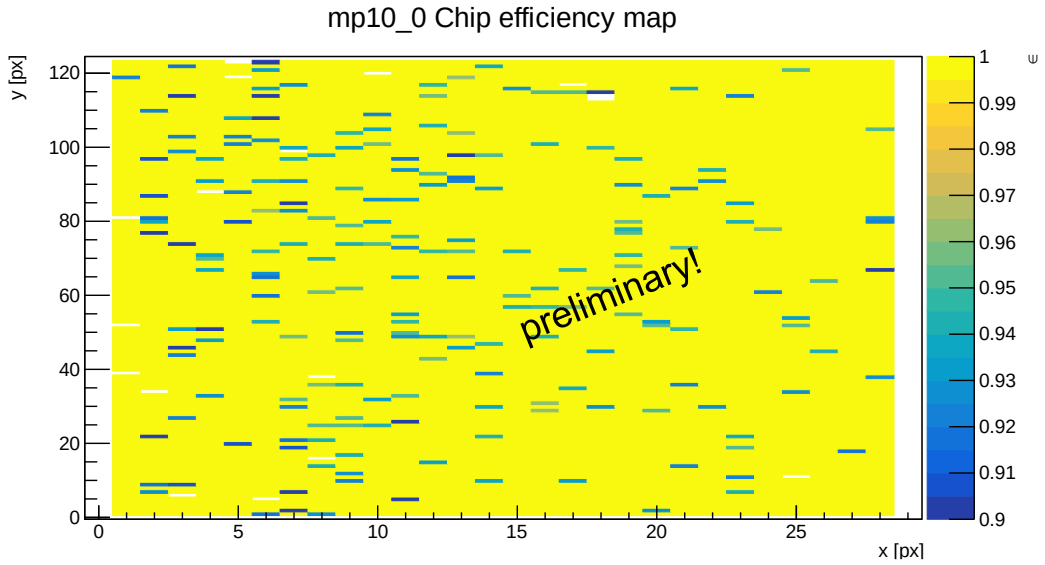
- Pixel matrices with three amplifier types have been operated with smallest possible threshold
- Signal to noise ratio (from ToT) and time walk for signals larger than 3200e have been measured
- CMOS amplifier has smallest time walk
- Low power consumption is possible

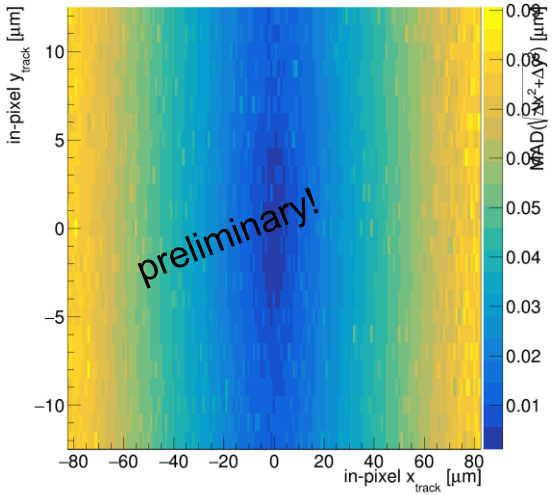


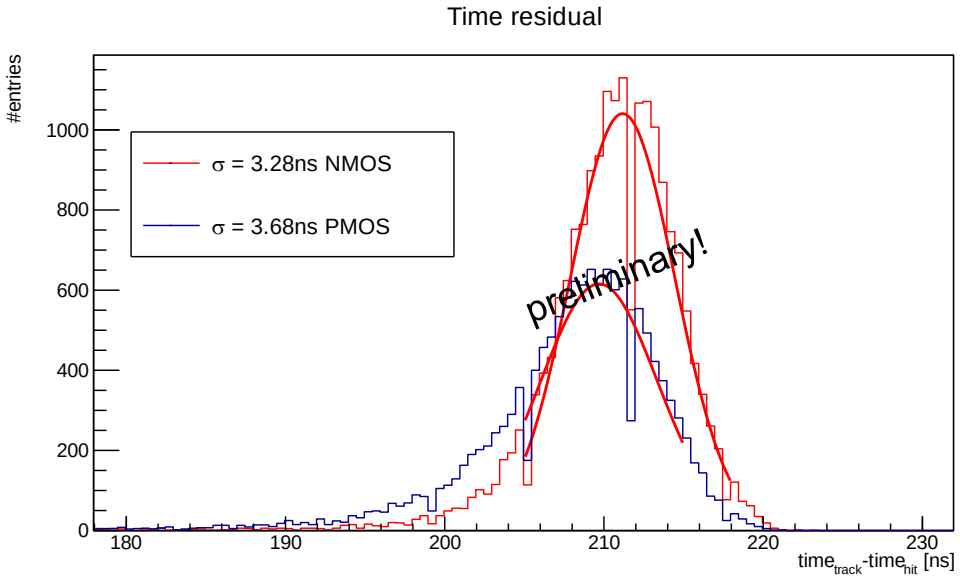


ATLASPIX3: 140mW/cm^2

- Test beam measurement have been performed at DESY (Lennart Huth)





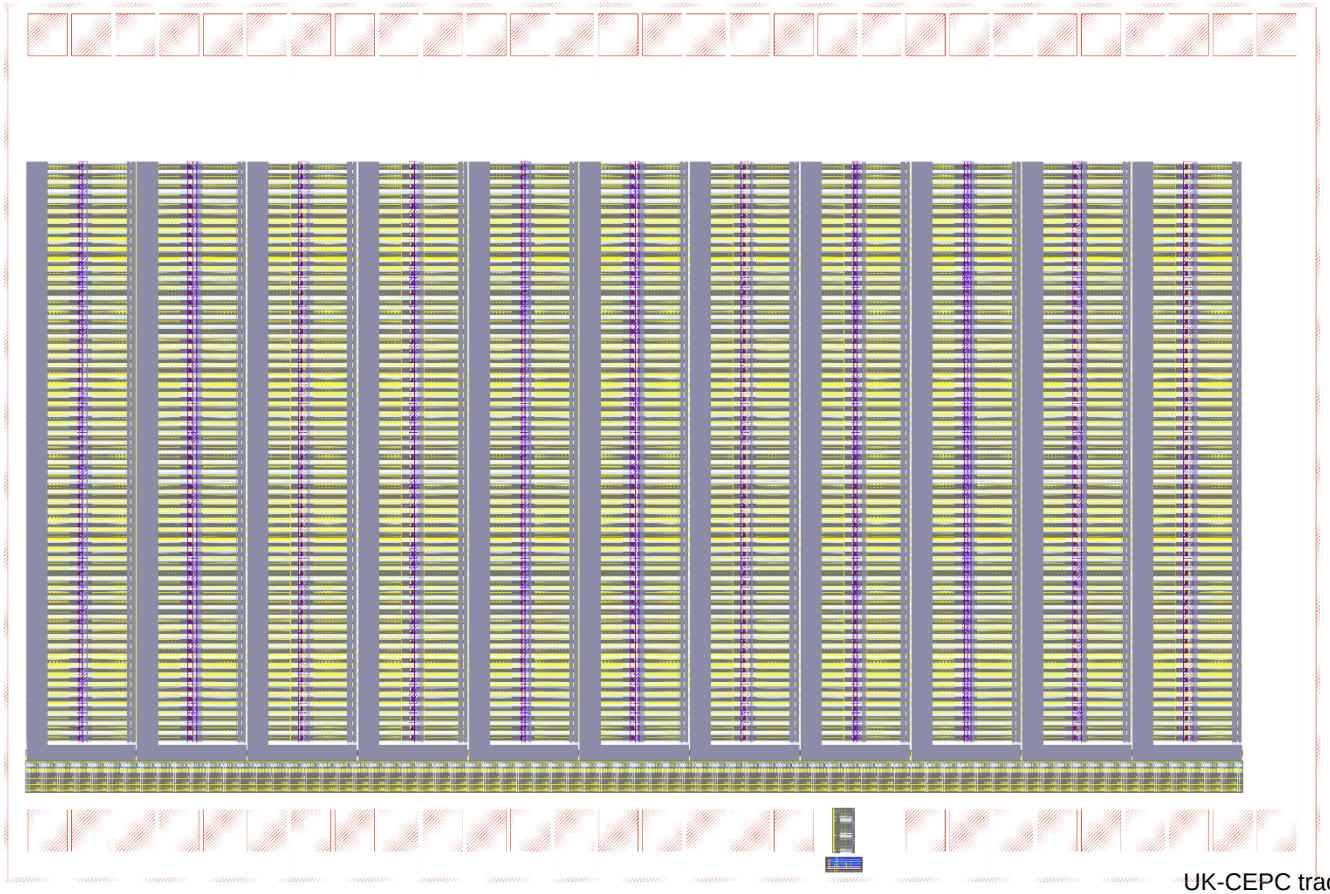


- Y: 165µm pitch -> 47.0µm resolution
- X: 25µm pitch -> 8.2µm resolution
- Resolution along x is below expectation of <7.2µm. Likely due to telescope pointing resolution – needs to be verified

- Time resolution of 3.28ns (RMS) without any correction

HVCMOS Sensor in 55nm Technology

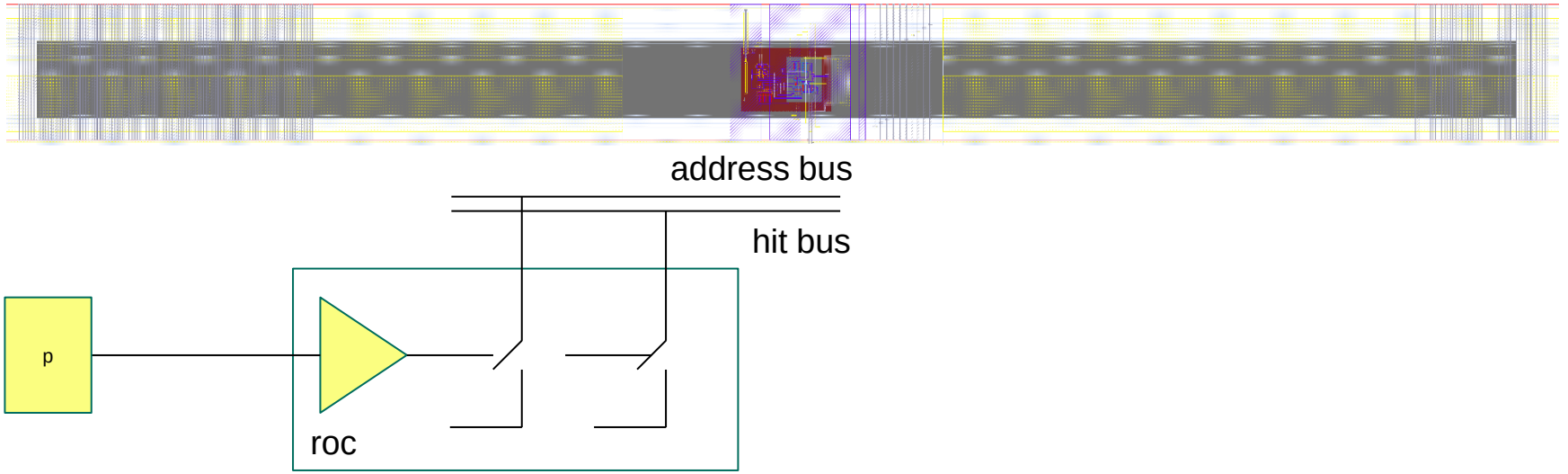
- We have started with design of the dedicated CEPC design in the HLMC 55nm HVCMOS technology
- The test sensor should be submitted within an MPW run
- The run was originally planned for August 2021, it is postponed to March 2022
- An area of 3 x 2 mm is reserved for our design
- The test chip would contain a pixel matrix with 11 x 60 pixels.



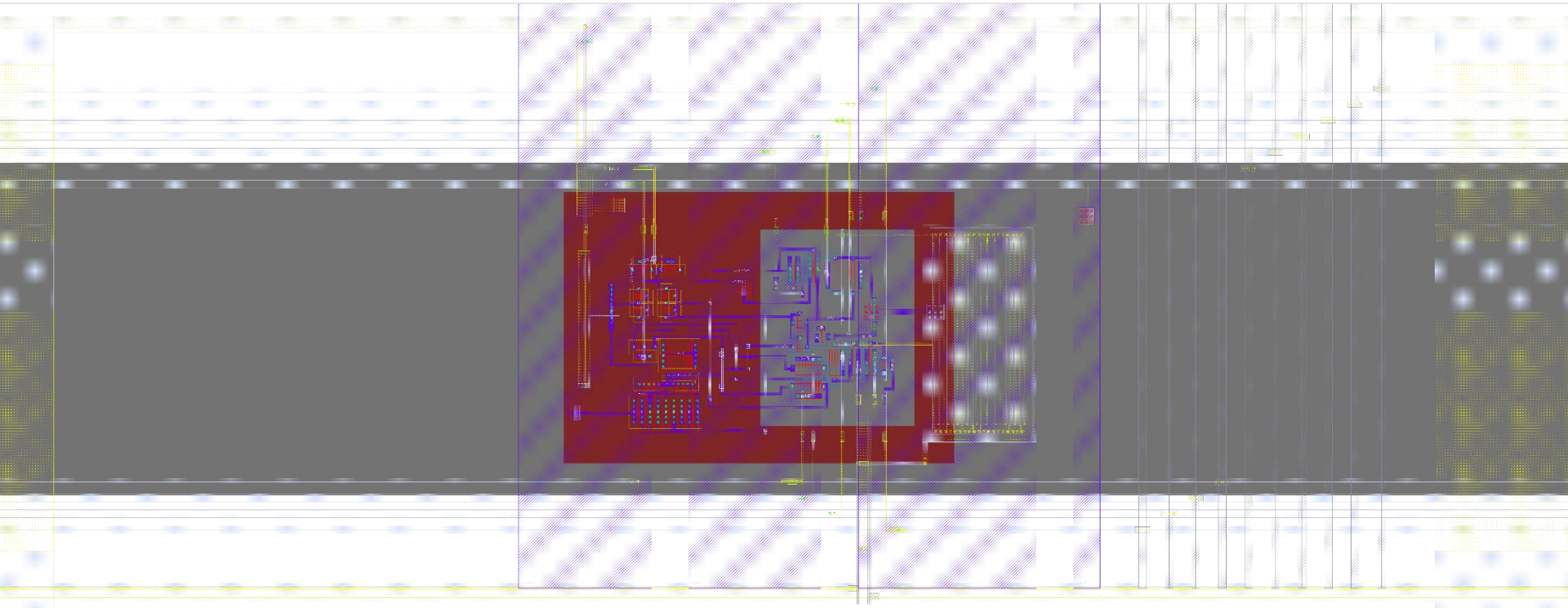
HVCMOS Sensor in 55nm Technology

- HLMC technology offers similar layers as TSI
- Especially important is the floating logic structure with deep n-well
- The maximum voltage for HV transistors is 32V
- Deep n-well to p-substrate should have higher breakdown
- Metal layers 1 – 6 can be used for fine pitch routing
- The realistic pitch is down to 0.2um – relaxed and according to recommendation is 0.3 (in 180nm was 0.6)
- There are tree more thick metal layers, suitable for power
- Low voltage power supply is 1.2V
- There are only hspice models available, we used Mentor Calibre for DRC LVS

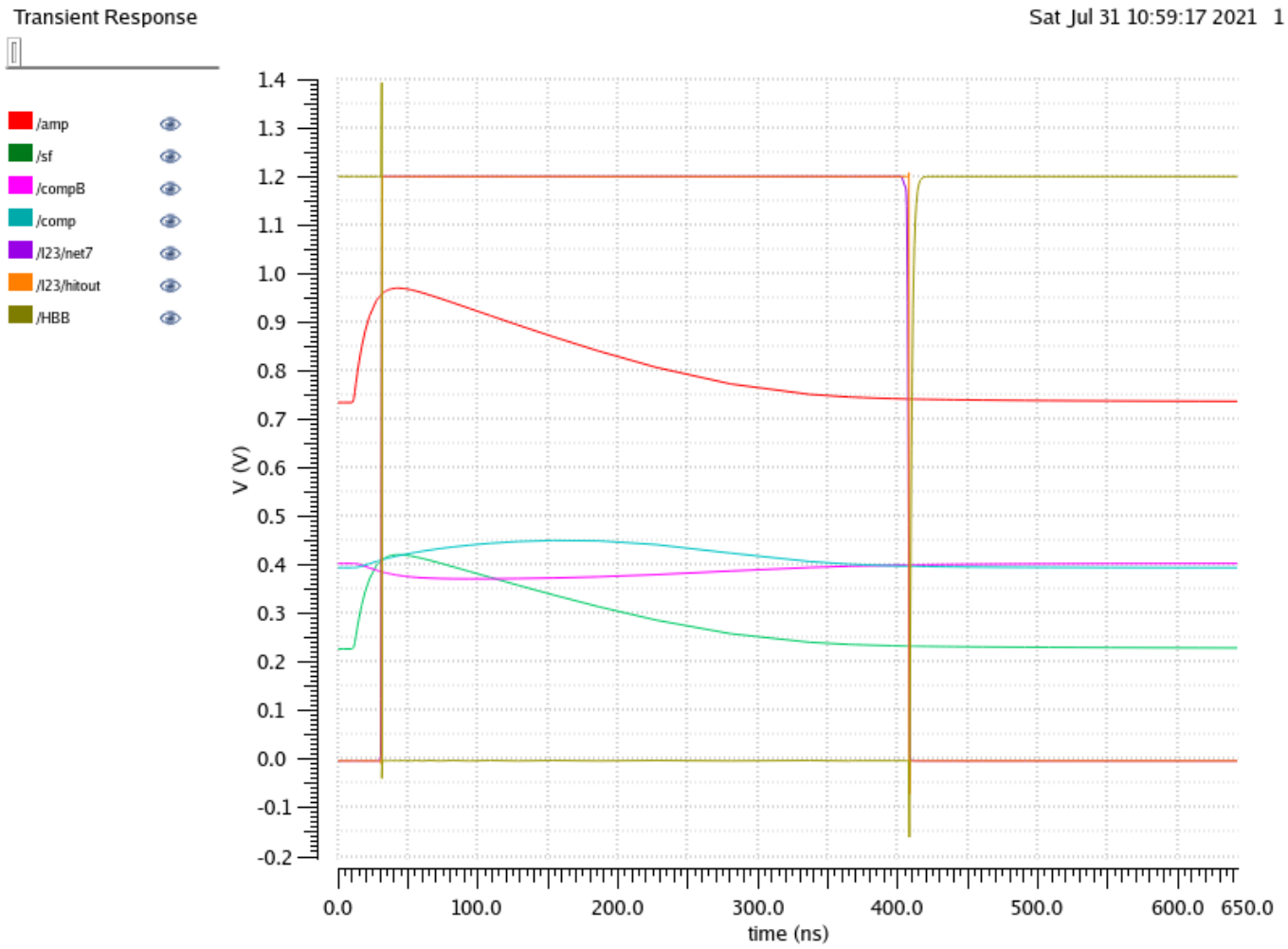
- The pixel site is 252 µm x 22 µm
- The pixel contains CSA, CR filter and differential output driver
- Every pixel has a readout cell placed at the periphery
- One readout cell contains differential receiver – the driver (in pixel) and the receiver form a distributed comparator
- The structure of readout cell is simple, the comparator output is connected to hit bus driver and to address ROM. The ROM cells pass the data to the 10 bit address bus
- The readout cell also contains two bit-register to store comparator enable and injection enable bits
- The size of the readout cell is 4.2µm x 60µm (relaxed layout)



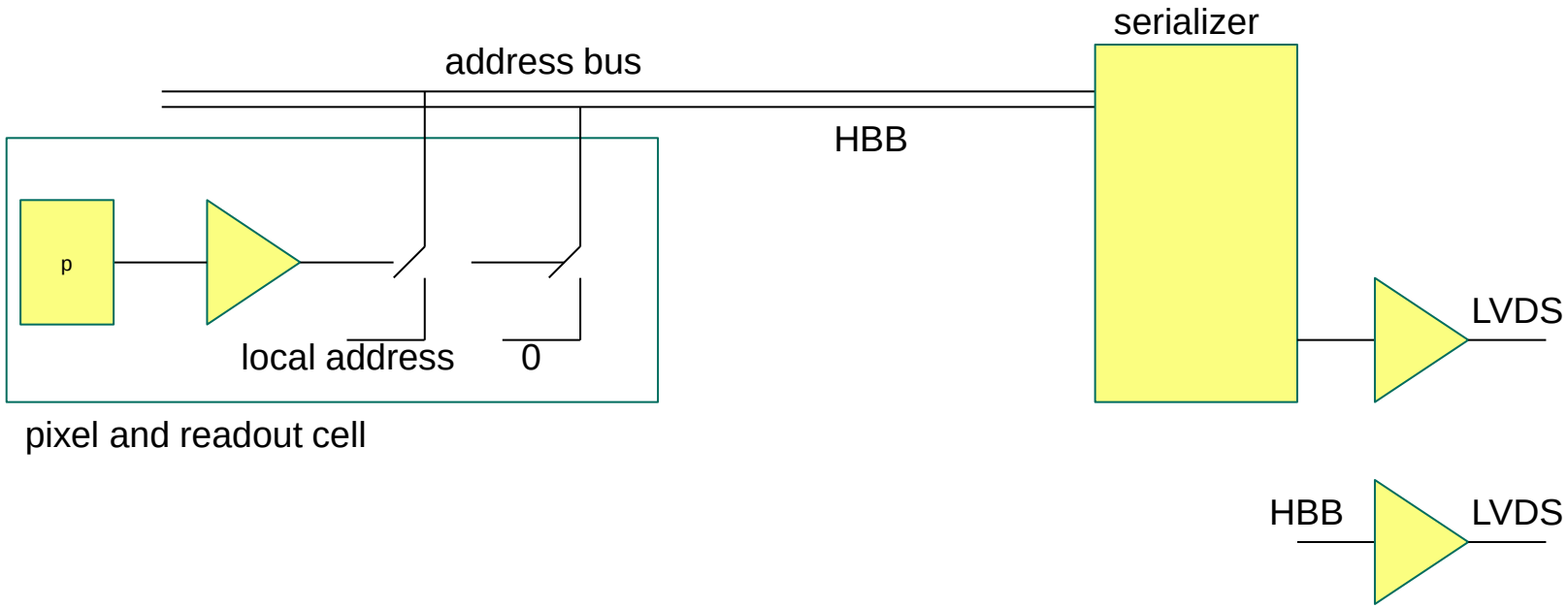
pixel p and readout cell

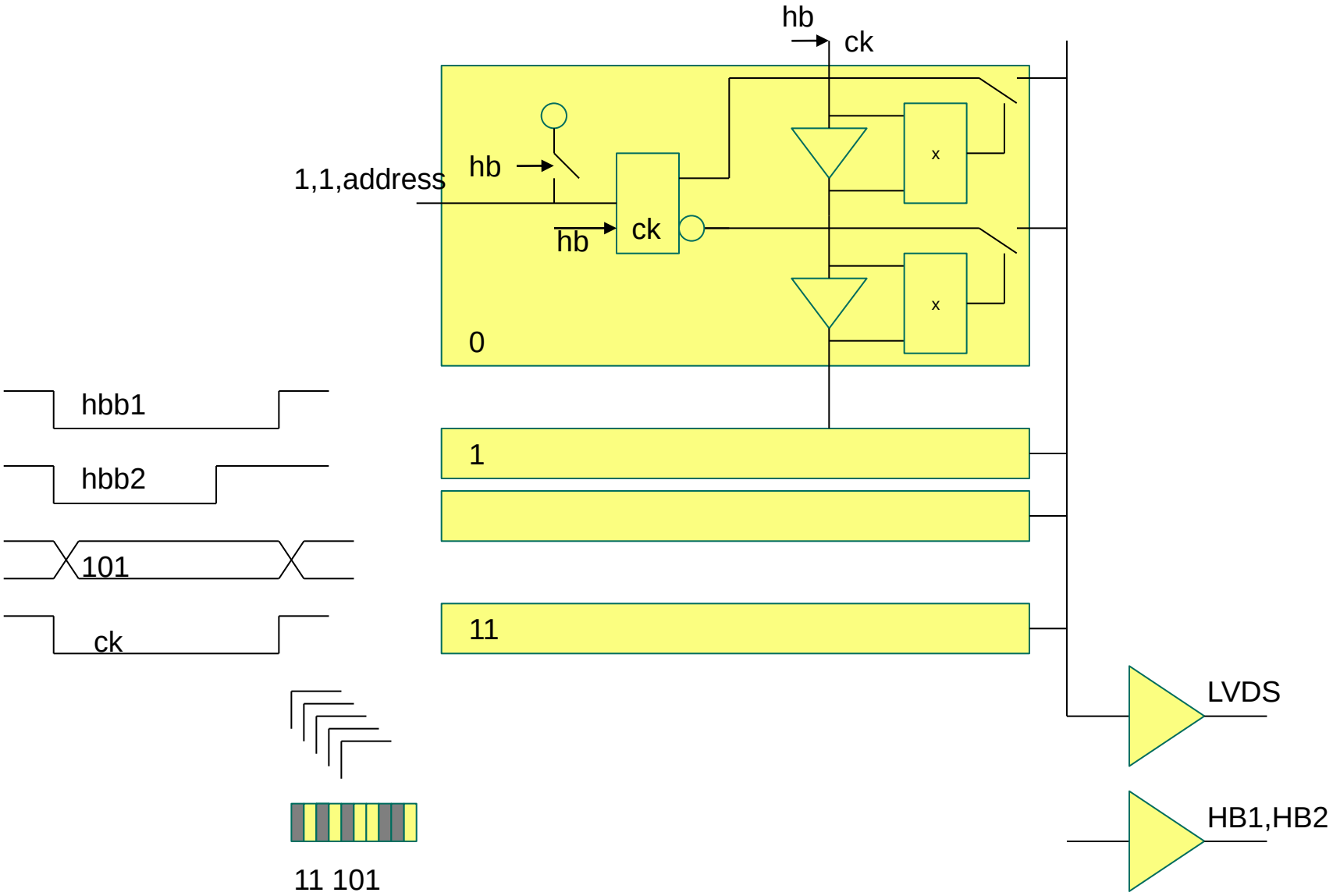


- Pixel and readout cell analog simulation



- Beside the pixels and its readout cells, the chip also contains novel asynchronous serializer
- The serializer receives the 10 address lines (parallel in) and the hit bus signal and sends the serialized address information
- The serializer does not need clock input. The clock for serialization of the address is generated by buffer chain (delay line) that is activated by hitbus
- This scheme is very simple, low power
- The output of the serializer is connected to LVDS output driver
- The hit bus signal is also connected to LVDS driver
- By measuring the hit bus singal length (ToT) off chip, the signal amplitude can be determined




hb
ck
1,1,address
hb
hb
ck
x
x
0
hbb1
hbb2
101
ck
1
11
LVDS
HB1,HB2
11 101

- Since the pixels are long and narrow, we expect 2-pixel clusters
- If we had just one hit bus line, we could not measure the amplitude of both pixels of a cluster
- To allow amplitude measurement of both pixels in a cluster, we foresee two hit bus lines – HB1 and HB2.
- The pixel are connected alternately to HB1 and to HB2.
- The address encoding is done in the way, that if two neighbour pixels are hit, the received code corresponds one of the pixels
- In the case of 2-pixel clusters, by examining the HB1, HB2 and address code we can reconstruct which pixels were hit and their signal amplitudes.

- Sensor modules

ATLASPIX3 quad module B. Raciti, PSD 2021

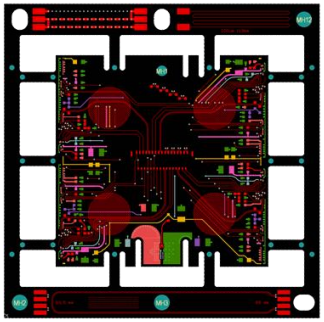


Fig. Scheme of the quad module flex.

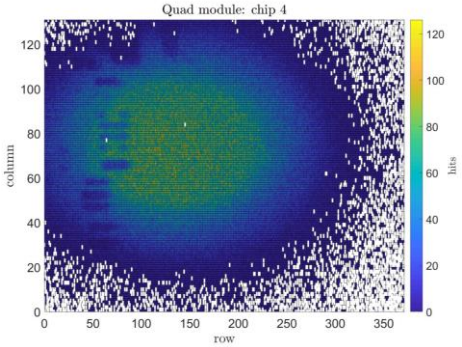


Fig. Hit map of a source run with ^{241}Am on chip 4.

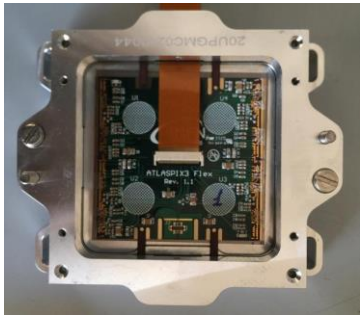
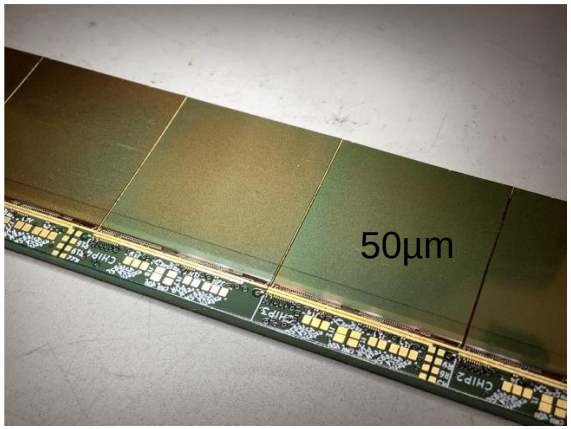


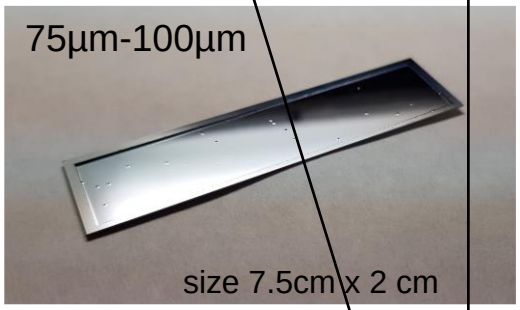
Fig. Image of the quad module.

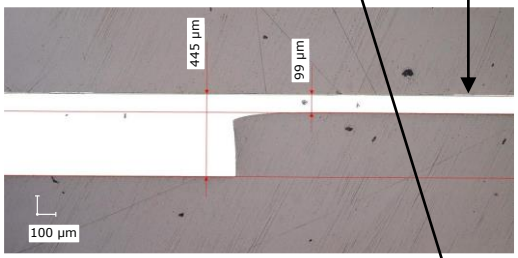
- Mu3e pixel detector will contain four pixel layers with a total sensor area of more than 1.1m^2
- 2844 Chips (sensor area 4cm^2 + periphery) tinned to 50µm will be glued to Al printed flex, and connected by SPTAB. Only Helium cooling will be used. Flex foils will serve as support structure. Only 0.1% of radiation length per layer

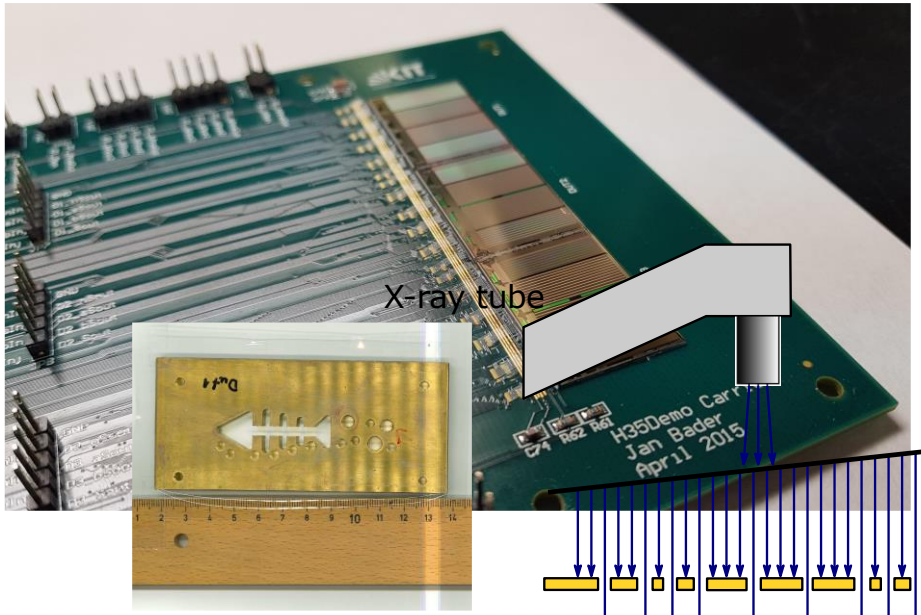


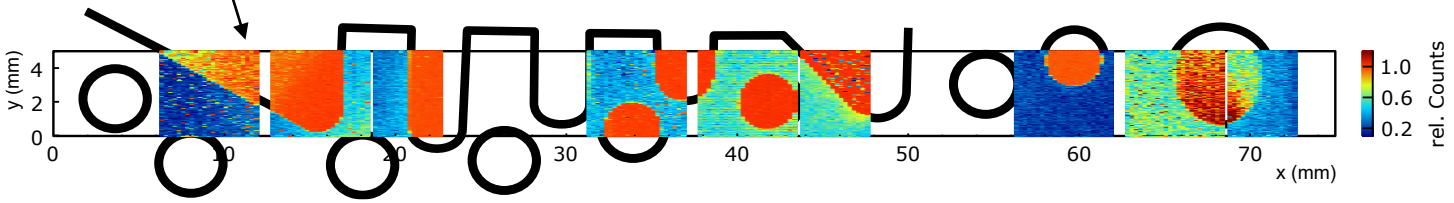
Mu3e ladder

- Another concept would be to use multichip- only silicon modules
- Multichip module with H35DEMO sensors (H35 technology)
- Profile with thin active area and thicker support frame has been done by ion etching (IZM Berlin)
- X-ray image of absorber recorded with thinned H35DEMO module









Summary

- HVCMOS sensors will be used to build thin pixel detector for Mu3e
- Large area sensor ATLASPIX – excellent detection efficiency
  - Foundry TSI semiconductors, process 180nm HVCMOS with high resistivity substrates
- Prototypes with smaller pixels (25µm x 165µm) designed for electron collider trackers and DESY beam telescope
- Preliminary results are promissing
- Design in 55nm HLMC technology almost finished