The FELIX Readout System

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On behalf of the ATLAS TDAQ Collaboration

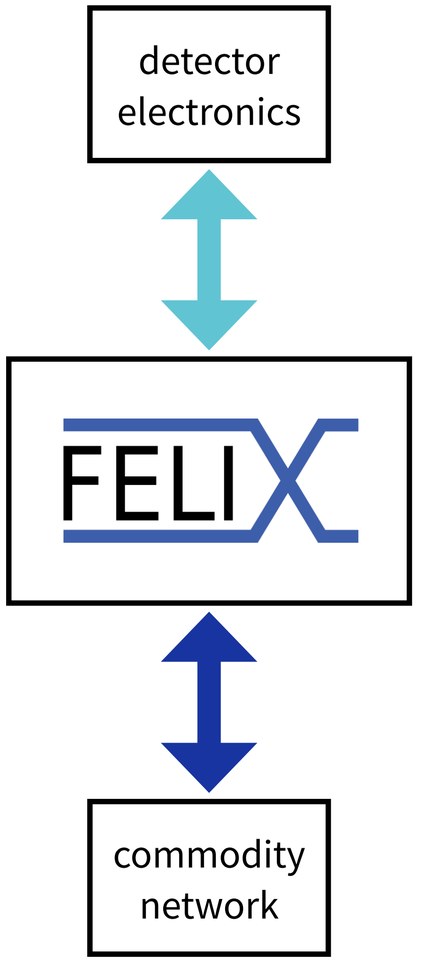
The FELIX readout system

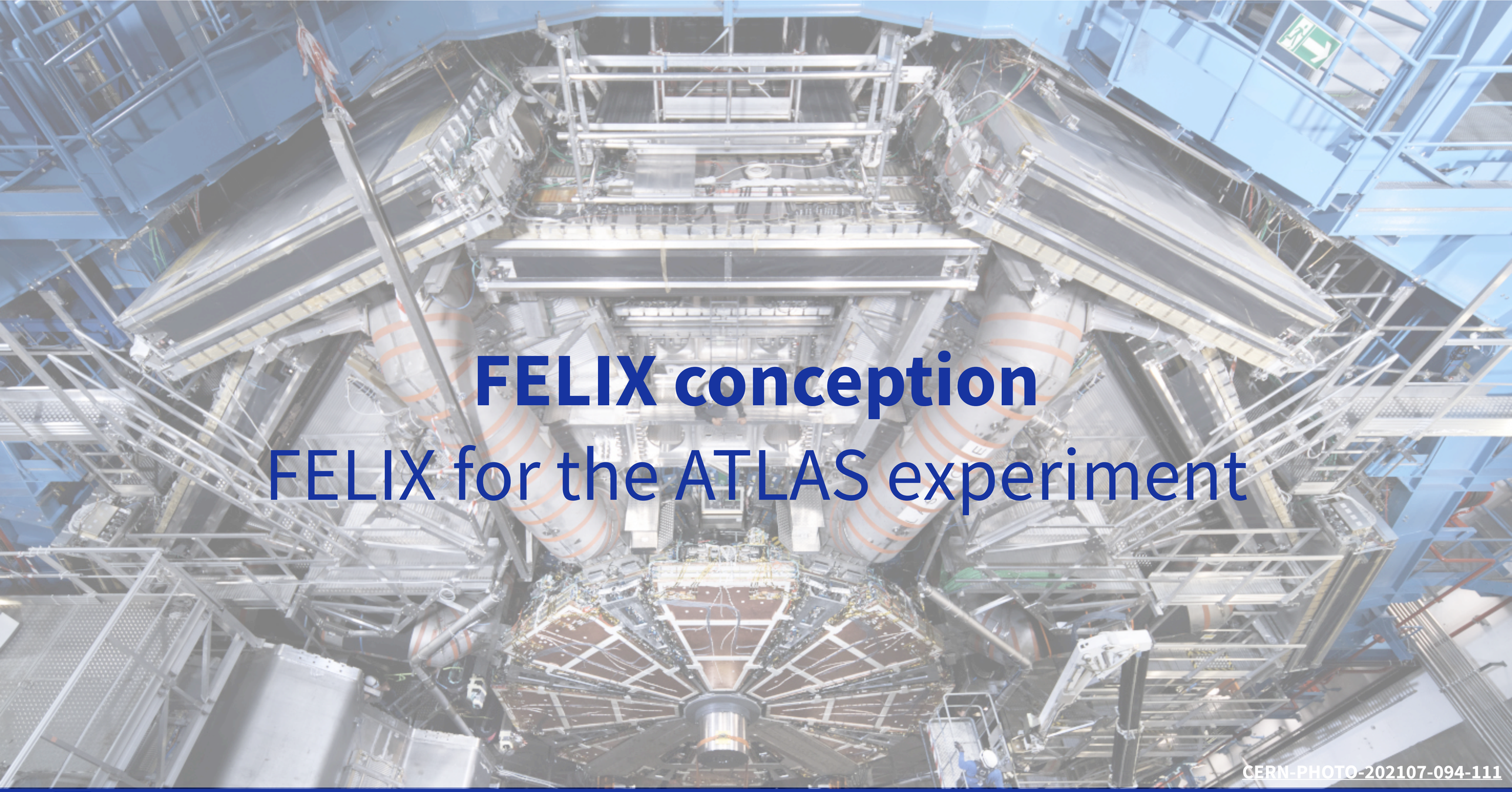
https://atlas-project-felix.web.cern.ch

- A generic detector readout concept, proposed by the ATLAS Collaboration, that connects front-end serial links to a commodity network

- Collaboration of different institutes
  - Open-source firmware and software

- Applications in HEP and Nuclear Physics experiments
  - ATLAS[1], ATLAS Phase-II[2], protoDUNE[3], NA62[4], sPHENIX at RHIC[5], CBM at FAIR[6], HIKE[7], LUXE[8]…





FELIX conception

FELIX for the ATLAS experiment

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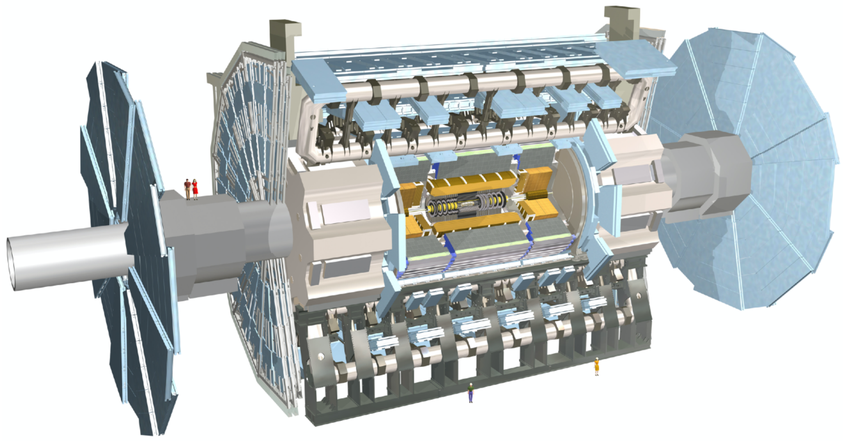
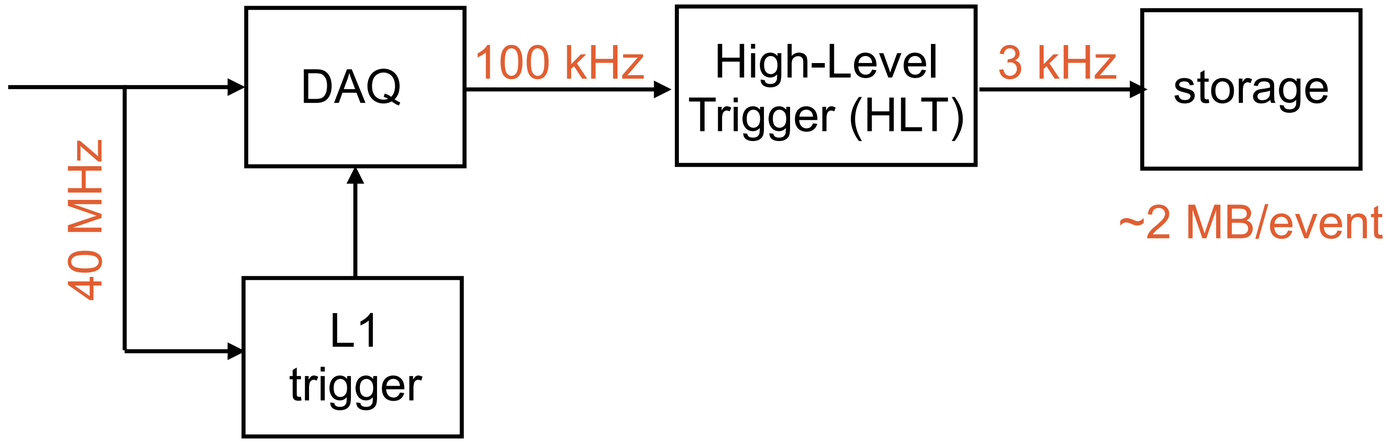
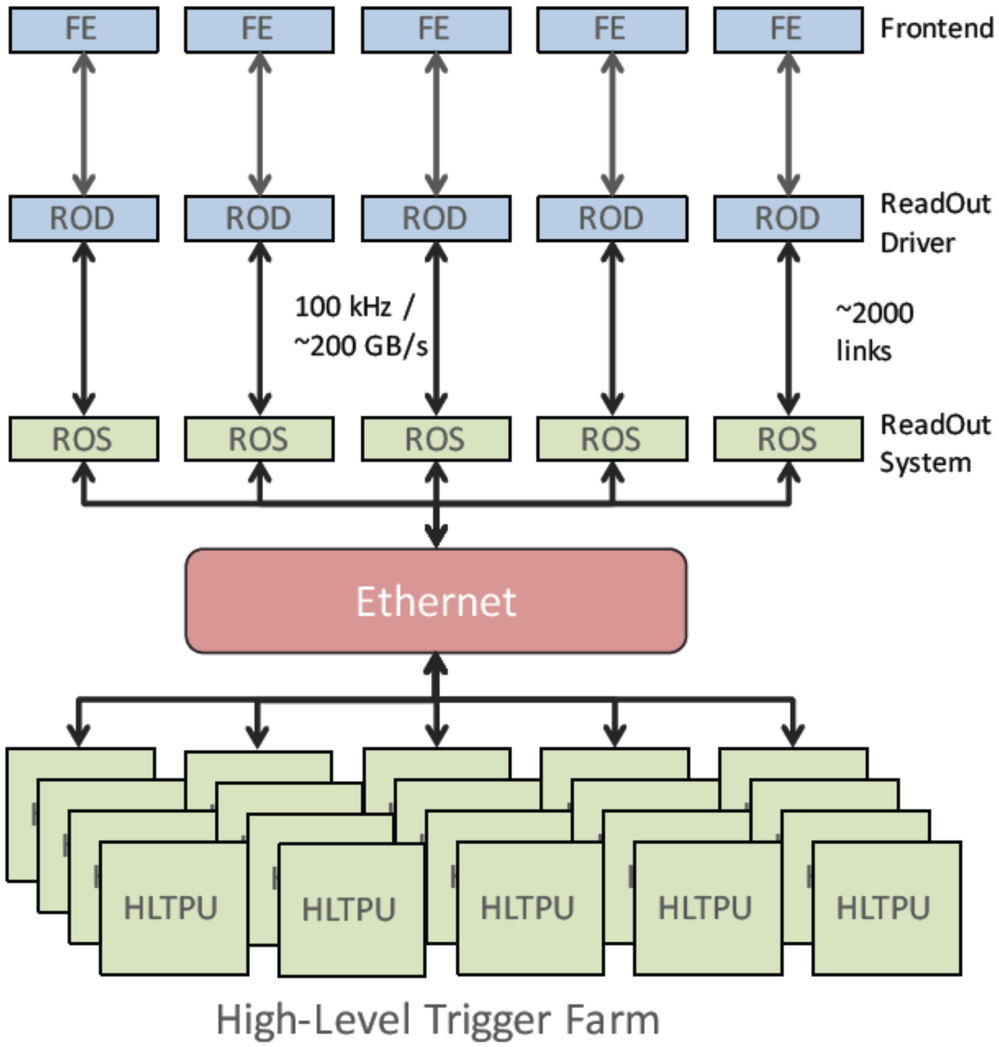
The ATLAS TDAQ architecture

- ATLAS is a general-purpose particle detector at the Large Hadron Collider (LHC)
- LHC collides protons/ions at a 40 MHz rate
- A first level (L1) trigger, implemented in hardware, selects events at maximum rate of 100 kHz
- A “high-level” trigger, implemented in software, selects events at maximum rate of 1-3 kHz





ATLAS Readout in 2015-18



Readout Driver (ROD)

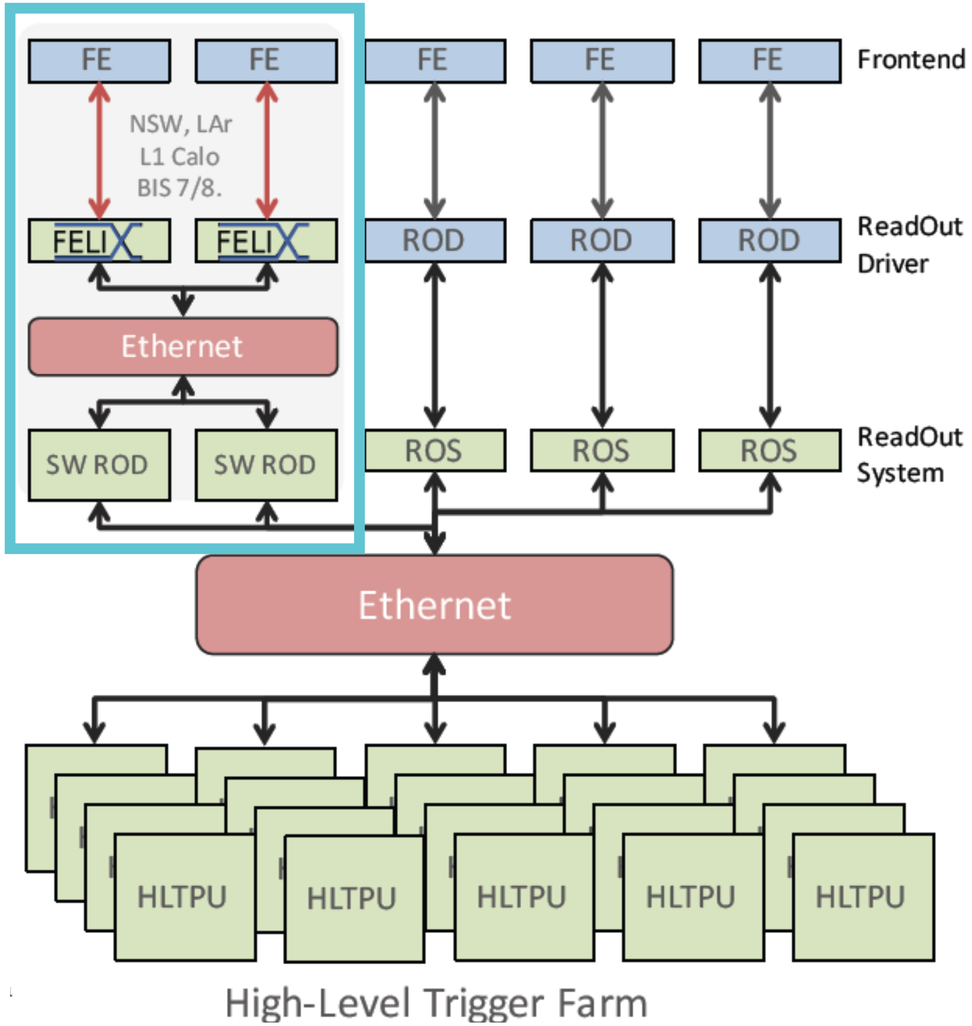
- VME boards, of about a dozen flavours developed and maintained by detectors
- Connected via point-to-point optical link to ROBinNP cards

Readout System (ROS)

- commodity computers hosting the ROBinNPs
- transfers data to the High-Level Trigger farm over the network

ATLAS Readout in 2022-25

New readout chain for upgraded detector and trigger components



FELIX: Front-End Link EXchange

- custom PCIe card hosted on commercial computer
- the interaction with FE includes readout, configuration, trigger & clock distribution, monitoring, BUSY
- about 100 cards, 60 host PCs

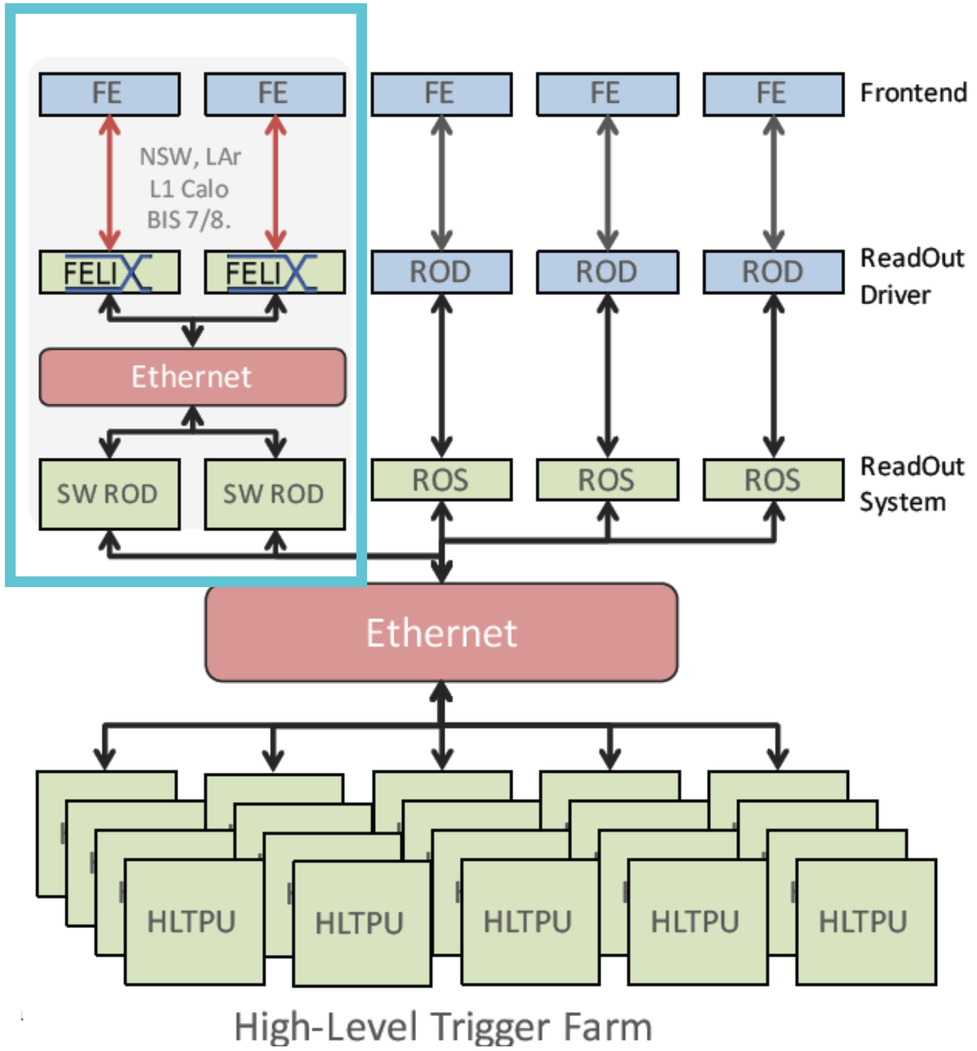
SW ROD: Software Readout Driver

- software running on commercial computer
- builds and aggregates events, detector-specific data processing
- about 30 servers

ATLAS Readout in 2022-25

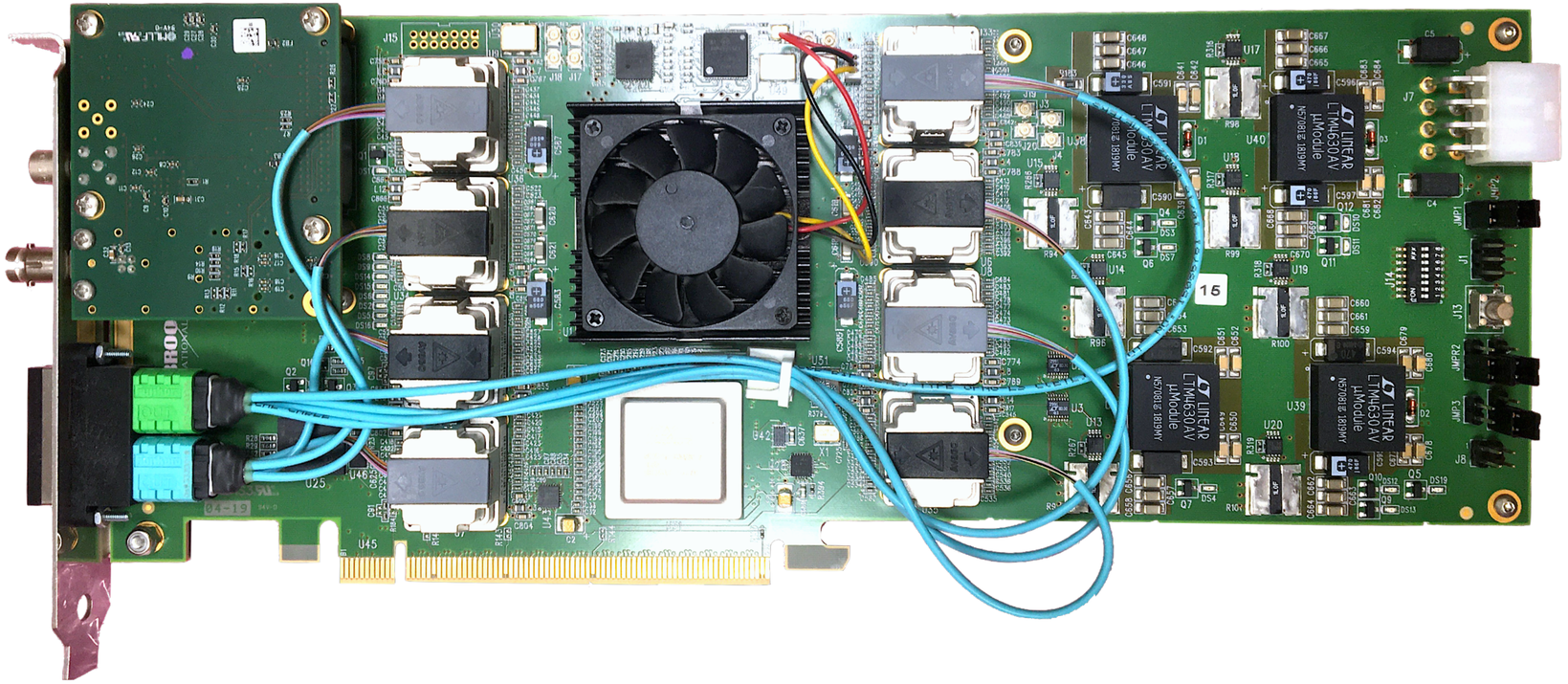
Benefits of the FELIX + SW ROD architecture

1. Less custom components
2. Less hardware and firmware development effort
3. Data transport decoupled from data processing
4. Industry-standard data networks introduced earlier in the readout chain
5. Aggregation of many links into a single higher speed network link



The FLX-712 card

- FPGA: Xilinx Kintex UltraScale XCKU115
- 8 MiniPODs to support up to 48 bidirectional 9.6 Gbps optical links
- 16-lane PCIe Gen3
- interfacing to Timing Trigger and Control (TTC) systems, BUSY output
- About 300 cards produced between 2020 and 2022



Why did ATLAS develop a custom card?

LHC Clock distribution

- During data taking the 40.079 MHz clock signal is provided by the LHC
  - The LHC clock is in synch with bunch crossing
  - All front-end and DAQ components need to be synchronised with the LHC clock
- FELIX needs an interface to the custom ATLAS TTC system to distribute clock and L1 trigger signals to front-ends

Front-end radiation hardness

- FELIX needs to support protocols used by radiation-hard front-ends
  - *GBT* [1], *lpGBT* [2] ASICs and data protocols developed at CERN
  - TCP/IP over Ethernet not an option so far

Availability and cost of commercial solution

- The constraints above strongly limit the selection of commercial products

[1] doi: 10.5170/CERN-2009-006.342
[2] http://lpgbt-fpga.web.cern.ch/doc/html/

FELIX in ATLAS data-taking

Firmware

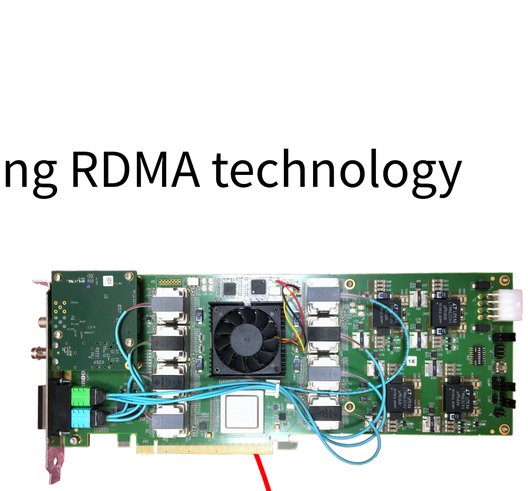
- Decodes incoming data, encodes outgoing data
- Transfers data to and from a buffer in the host computer
- Distributes clock and trigger

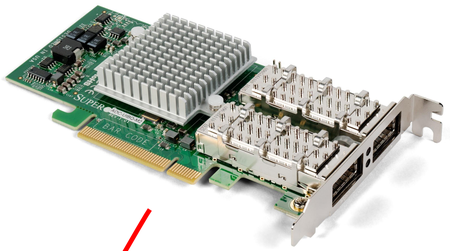
Software

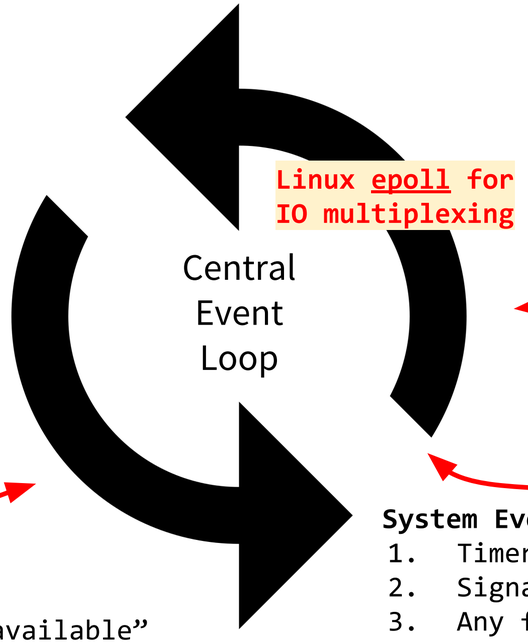
- Transfers data over the network using RDMA technology

Operational experience

- See J. Hoya talk at CHEP2023







FELIX in other experiments

protoDUNE, NA62, sPHENIX

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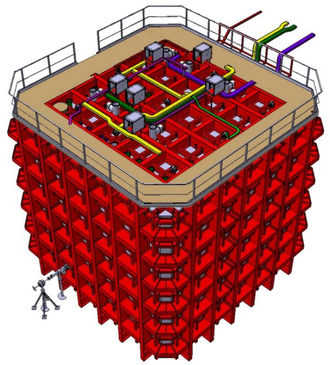
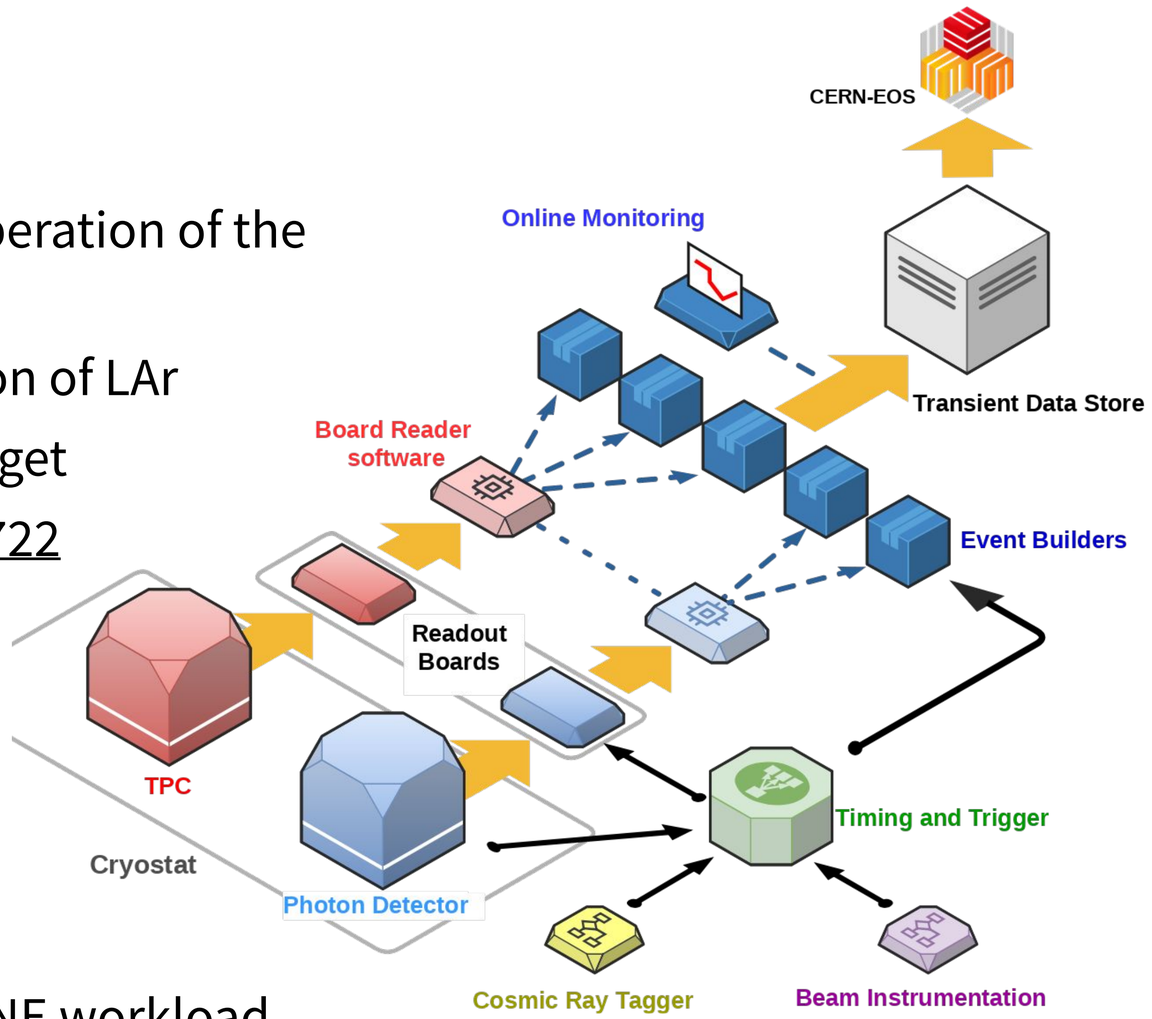
FELIX in protoDUNE-SP



ProtoDUNE single phase

- Demonstrator of design, construction, and operation of the DUNE TPC technologies
- Cryostat dimensions: 10m x 10m x 10m 750 ton of LAr
- Charged particle beam from SPS beam on target
- Test beam results published in arXiv:2007.06722



DAQ system [1, 2]

- Continuous readout of TPC at 2 MHz via FELIX
- 15 360 channels, 55 GB/s throughput
- FELIX firmware enriched with feature to support protoDUNE workload.
- Unlike ATLAS, FELIX host used to store data until requested by a trigger.

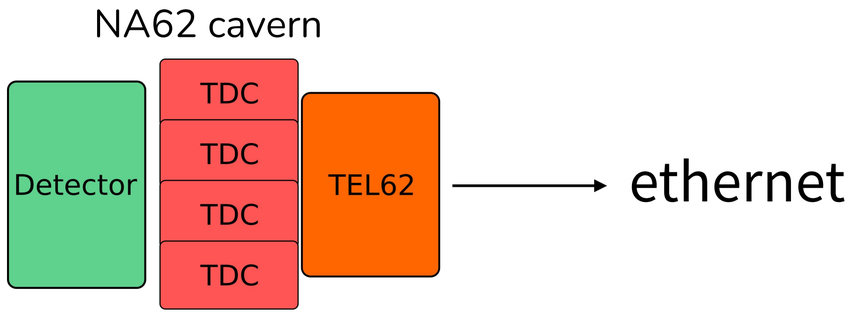
[1] https://doi.org/10.1051/epjconf/201921401013
[2] R. Sipos talk at IX Workshop on Streaming Readout

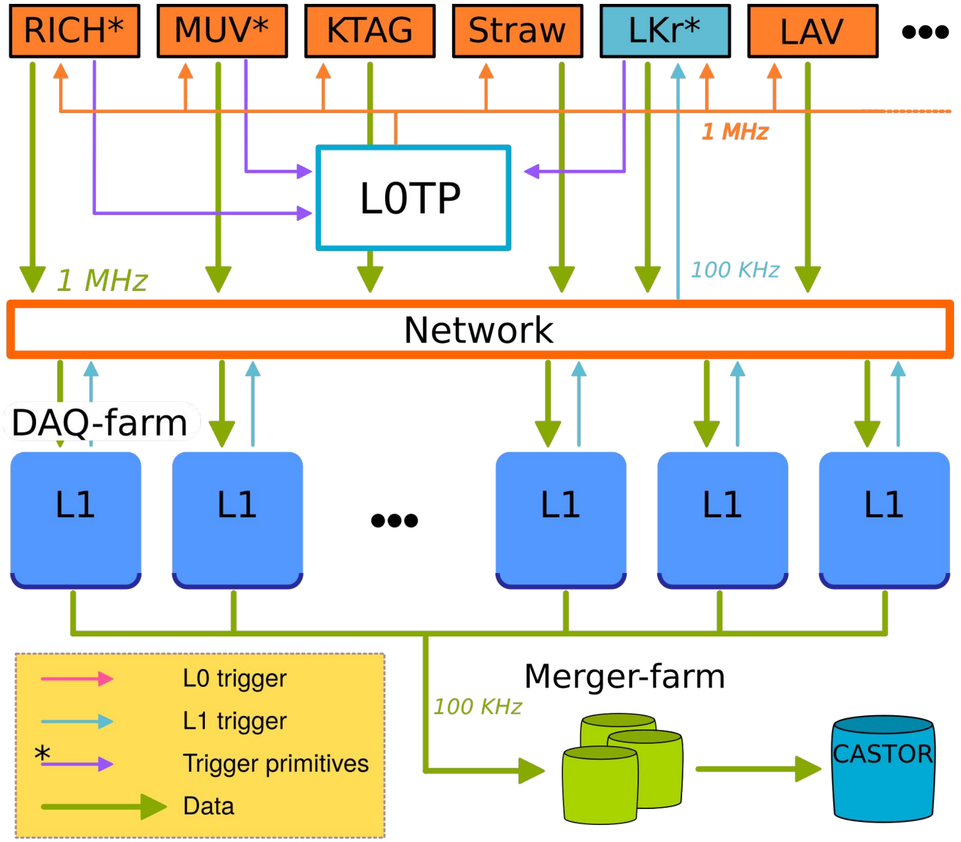
FELIX in NA62

- NA62 is a Kaon physics experiment located in the north area of the CERN SPS
- Kaon decay products detected using a wide range of detectors along a 270m-long beamline.

NA62 DAQ architecture [1]

- L0 trigger in hardware, max event rate 1 MHz
- L1 trigger in DAQ farm reduces event rate to 100 kHz
- “Legacy” readout uses TEL62 board [2]
  - digitises TDC information (TDC as TEL62 mezzanine)
  - buffers data
  - produced trigger primitives



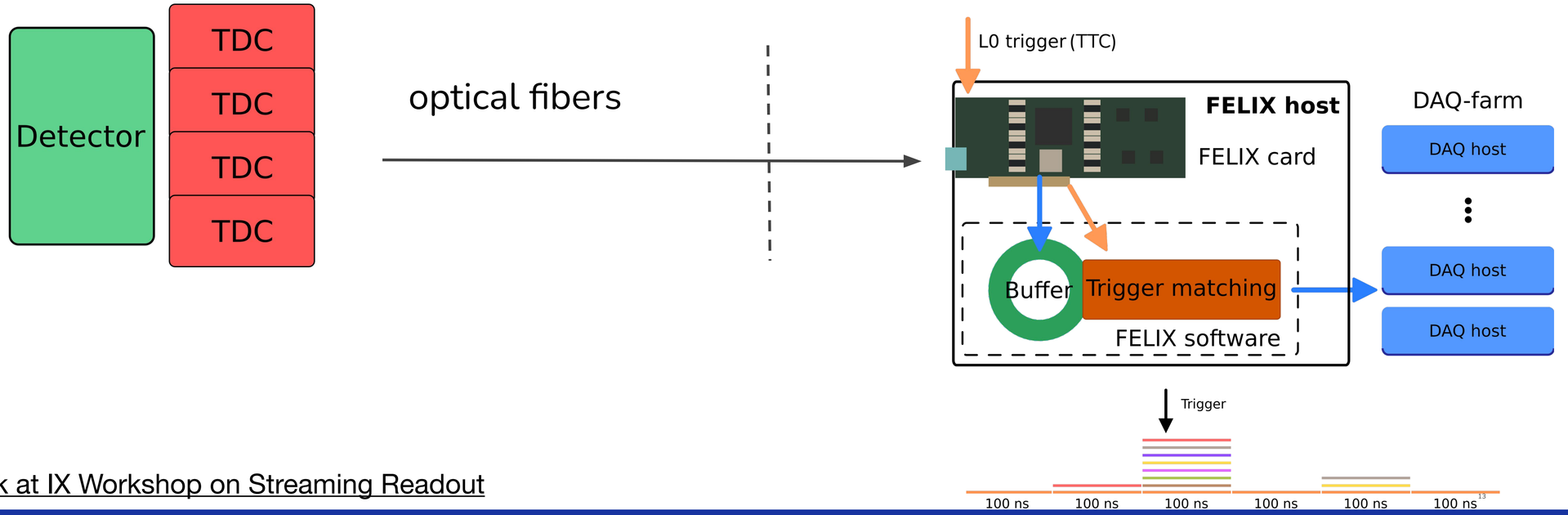


[1] M. Boretto talk at IX Workshop on Streaming Readout
[2] https://doi.org/10.1109/RTC.2014.7097525

FELIX in NA62

NA62 novel readout chain [1]

- New radiation-tolerant TDC boards with 10 Gbps transceivers
- FELIX used to
  - buffer data: hits are indexed and trigger matching extracts relevant hits
  - distribute clock
  - manage synchronous communication for control and configuration



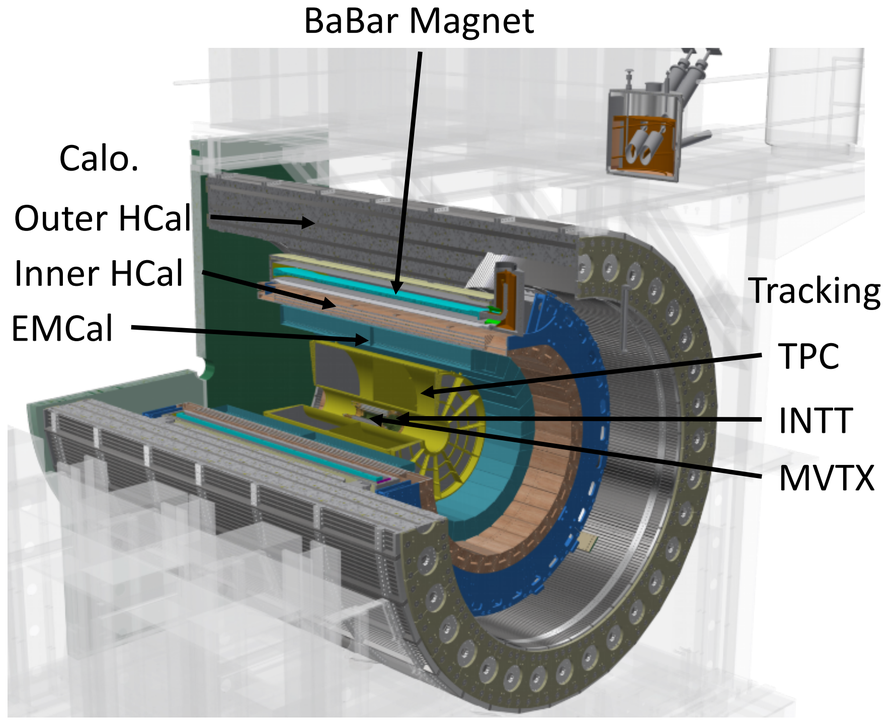
[1] M. Boretto talk at IX Workshop on Streaming Readout

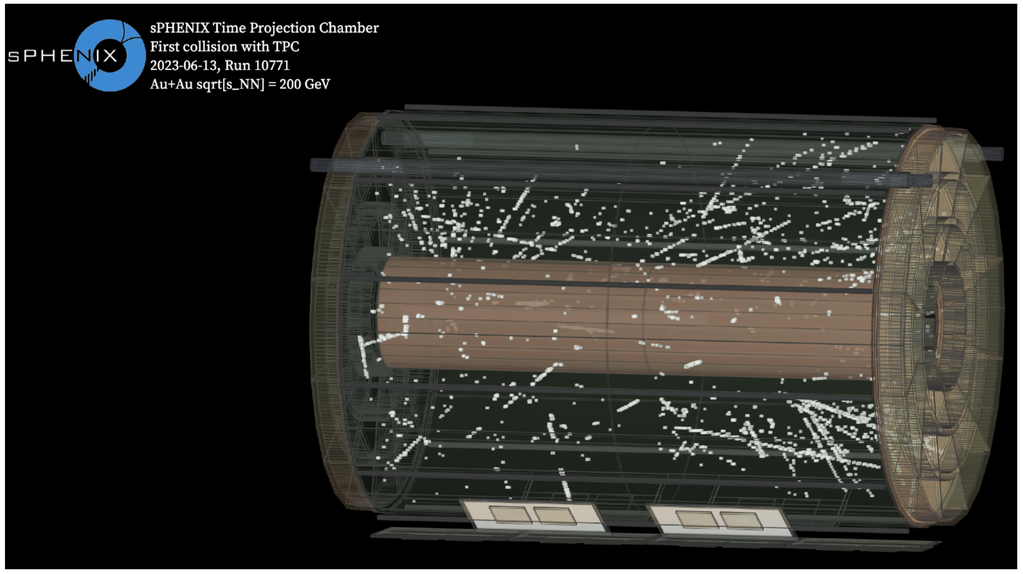
FELIX in sPHENIX

- Located at RHIC, sPHENIX is dedicated to the study of QCD and QGP at different energies scales using p+p or Au+Au collisions

- Three sub-detectors read with FELIX [1] in both triggered and streaming mode
  - Pixel Vertex Detector built with ALPIDE MAPS (~20 Gb/s)
  - Intermediate Silicon Strip Tracker (~7 Gb/s)
  - Compact Time Projection Chamber (~100 Gbps)

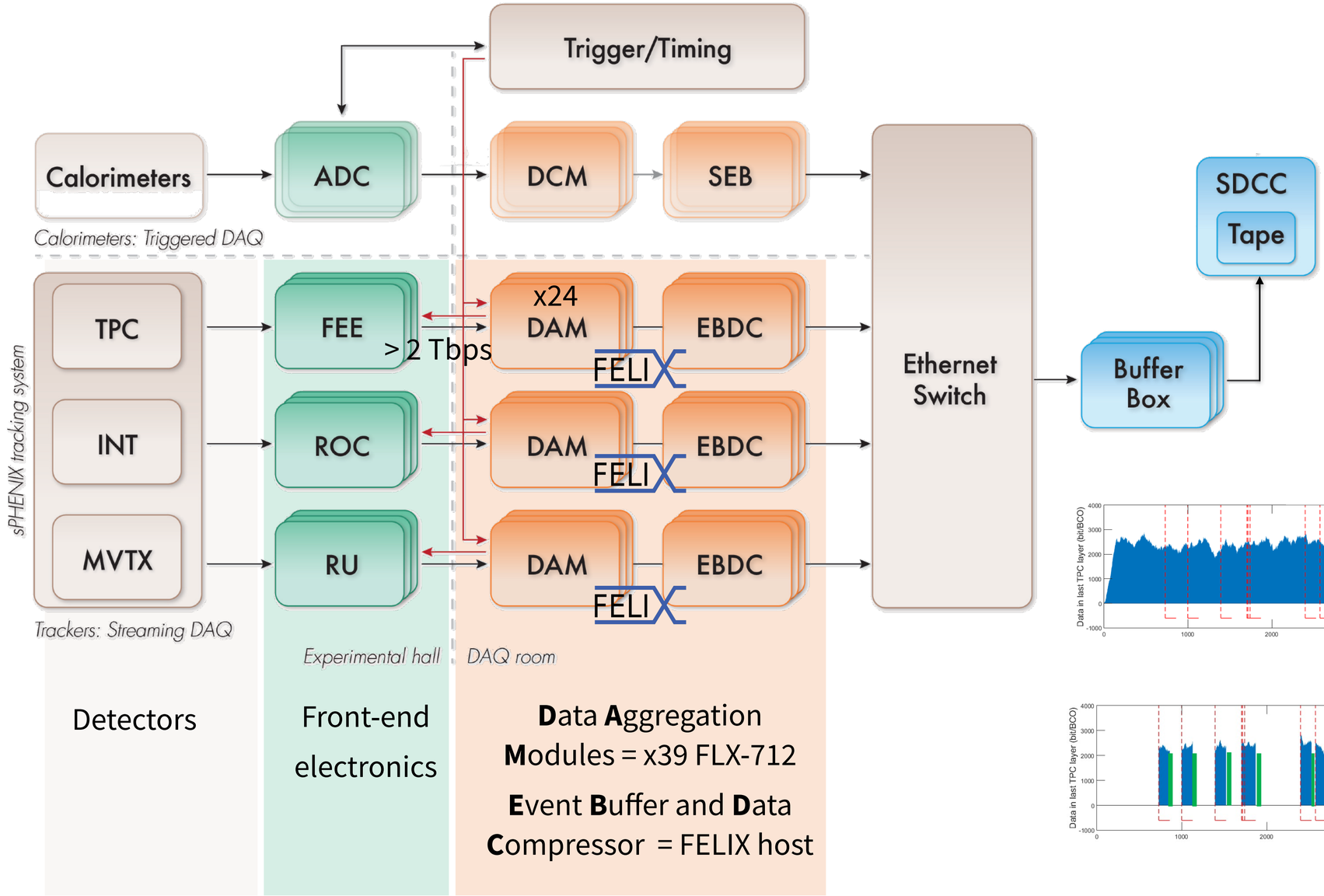
- Detector commissioning ongoing, data-taking starting soon



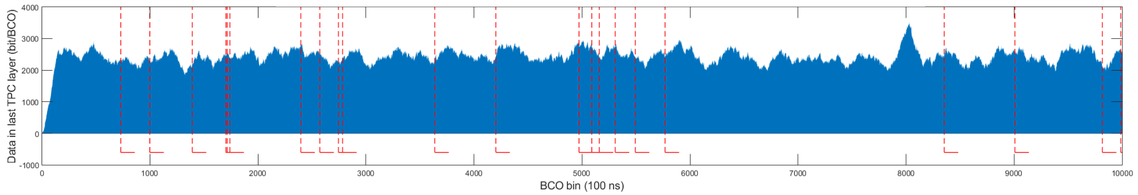


[1] M. Purschke, The sPHENIX DAQ System, IEEE-RT 2020

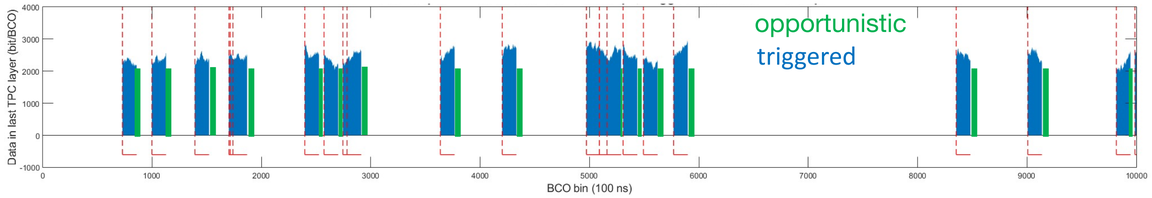
sPHENIX readout



FEE data input to DAM



DAM data output



M. Purschke, VIII workshop on Streaming Readout

Ongoing and future development

ATLAS Readout in ≥2029

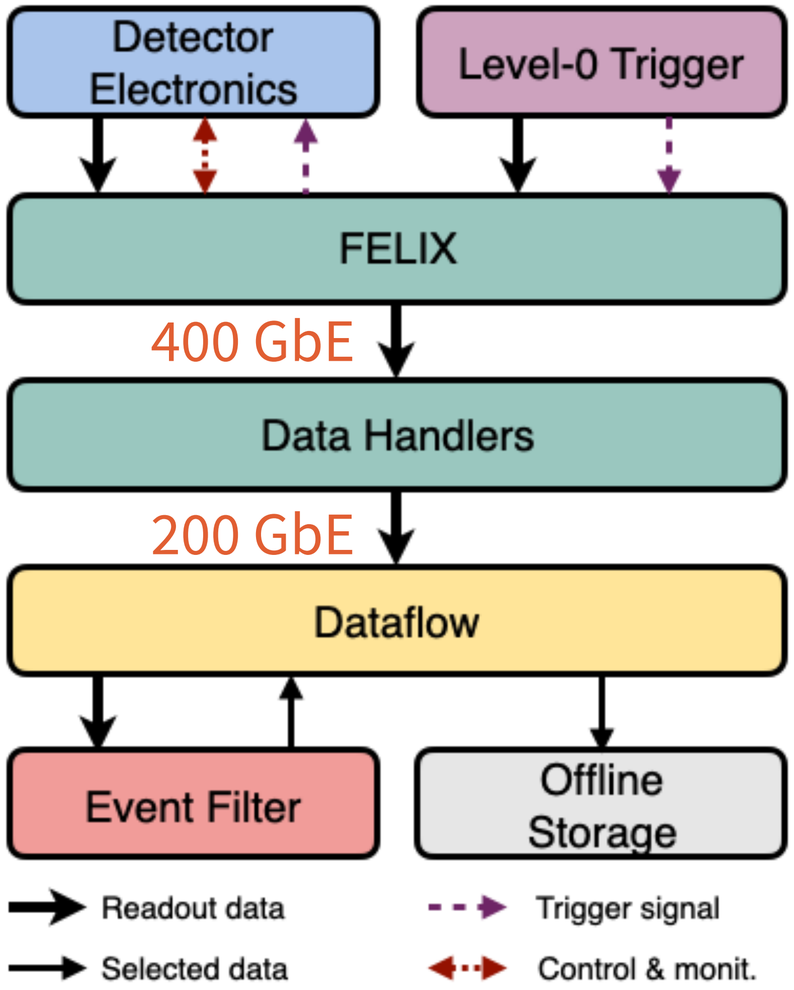
Architecture

- Similar architecture as in current data taking period
  - SW ROD renamed Data Handler

Workload & requirements

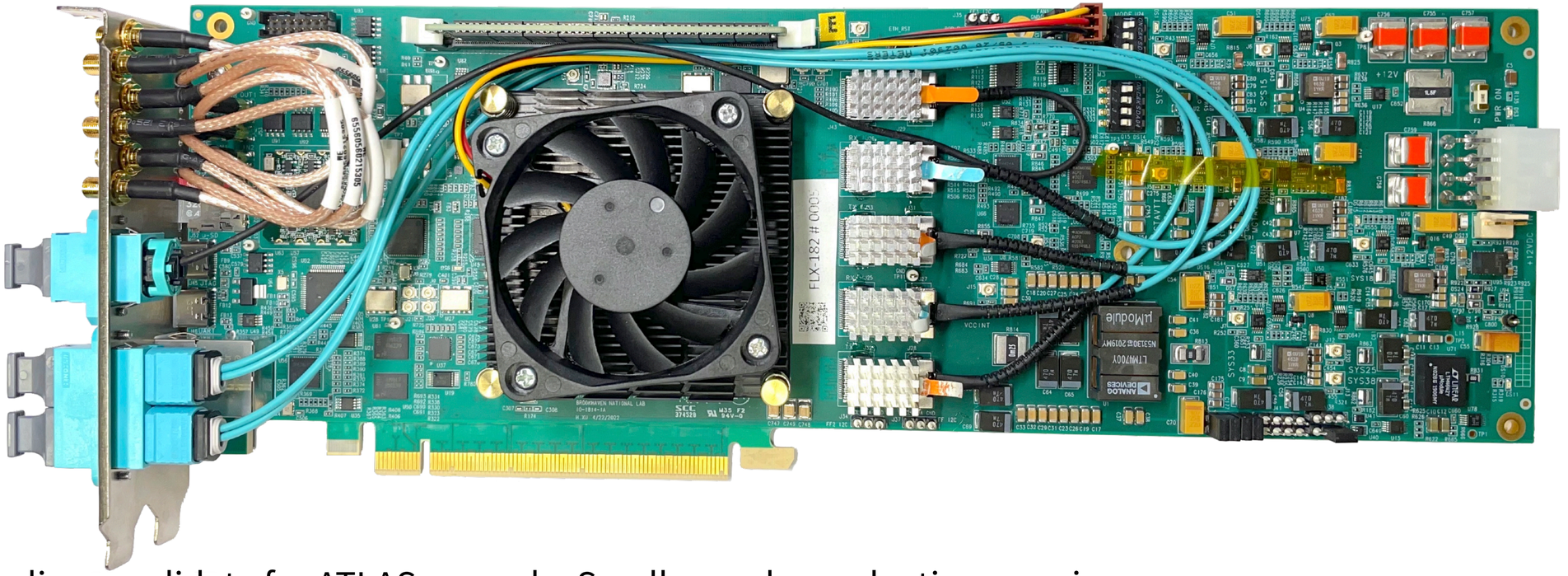
- Readout of all ATLAS sub-detectors
- 4.6 TB/s total data throughput (×20)
- 1 MHz data rate (×10)
- Support for additional protocols and 25 Gbps data links

- New FELIX hardware, firmware and software under development.



FLX-182 prototype board

- AMD Versal Prime VM1802 System-on-Chip
- x4 Firefly transceivers to support up to x24 duplex 25 Gbps data links
- x1 Firefly transceiver to support TTC interface / 100 Gbps Ethernet / 4 more 25 Gbps data links
- 16-lane PCIe Gen4



- Current baseline candidate for ATLAS upgrade. Small sample production ongoing.

Further developments

Firmware

- Firmware to support future ATLAS workload available for FLX-182
  - support for various data protocols & enconding including Intelaken for 25 Gbps links

Software

- Developments ongoing to scale up current architecture
- Retaining RDMA technology to fully use the 400 Gbps network bandwidth

Hardware

- Ongoing design of FLX card with
  - AMD VP1552 SoC with support for PCIe Gen5
  - up to 48 duplex data links at 25 Gbps
  - TTC interface or 400 GbE

Summary

- FELIX is a versatile data acquisition platform
  - particularly useful for experiments exposed to radiation

- The first FELIX implementation used in production
  - successful data taking with protoDUNE-SP
  - stable readout in ongoing ATLAS data taking
  - sPHENIX data taking starting soon

- An evolution of FELIX for the High-Luminosity LHC Phase of ATLAS is under development