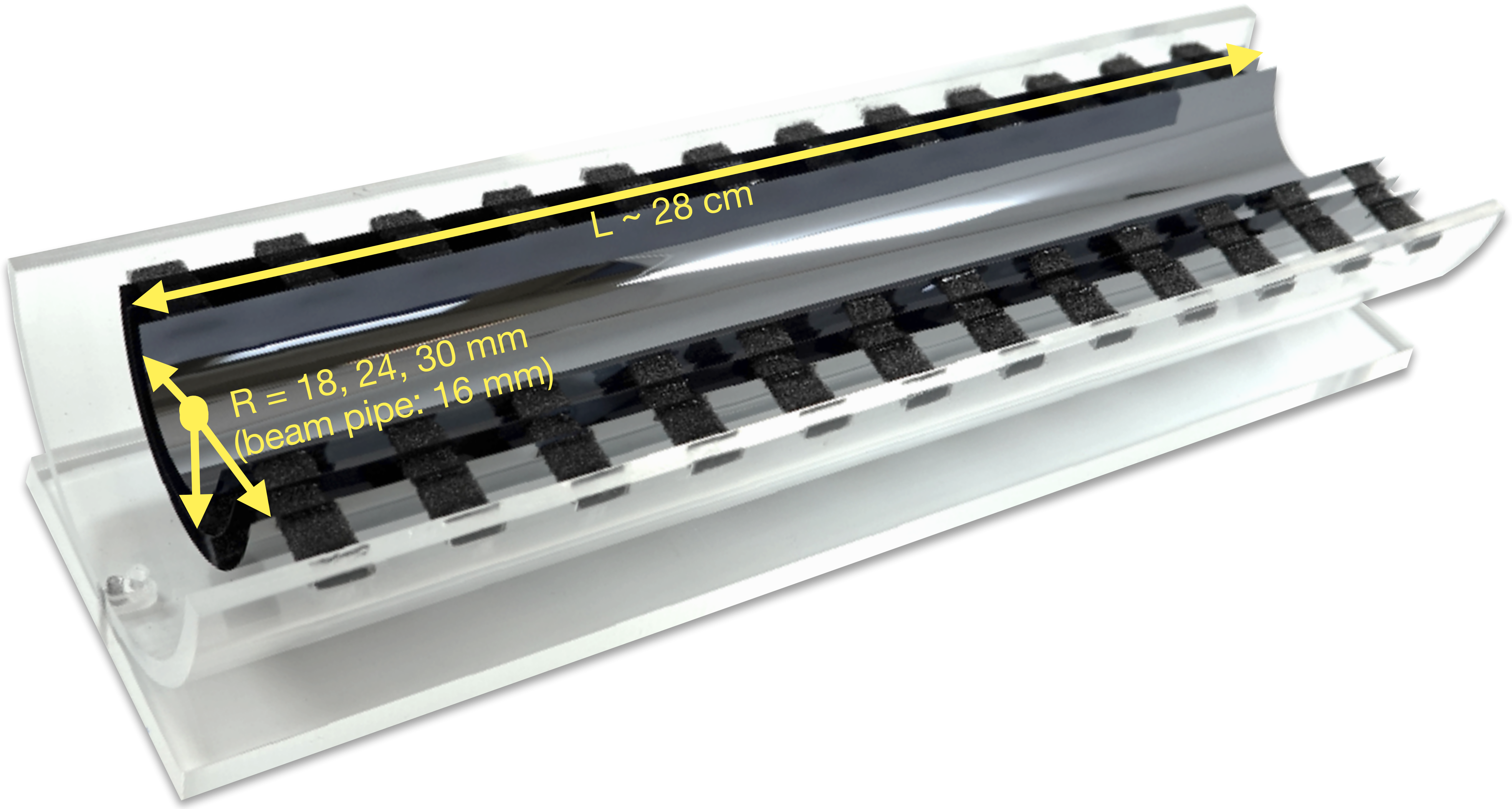
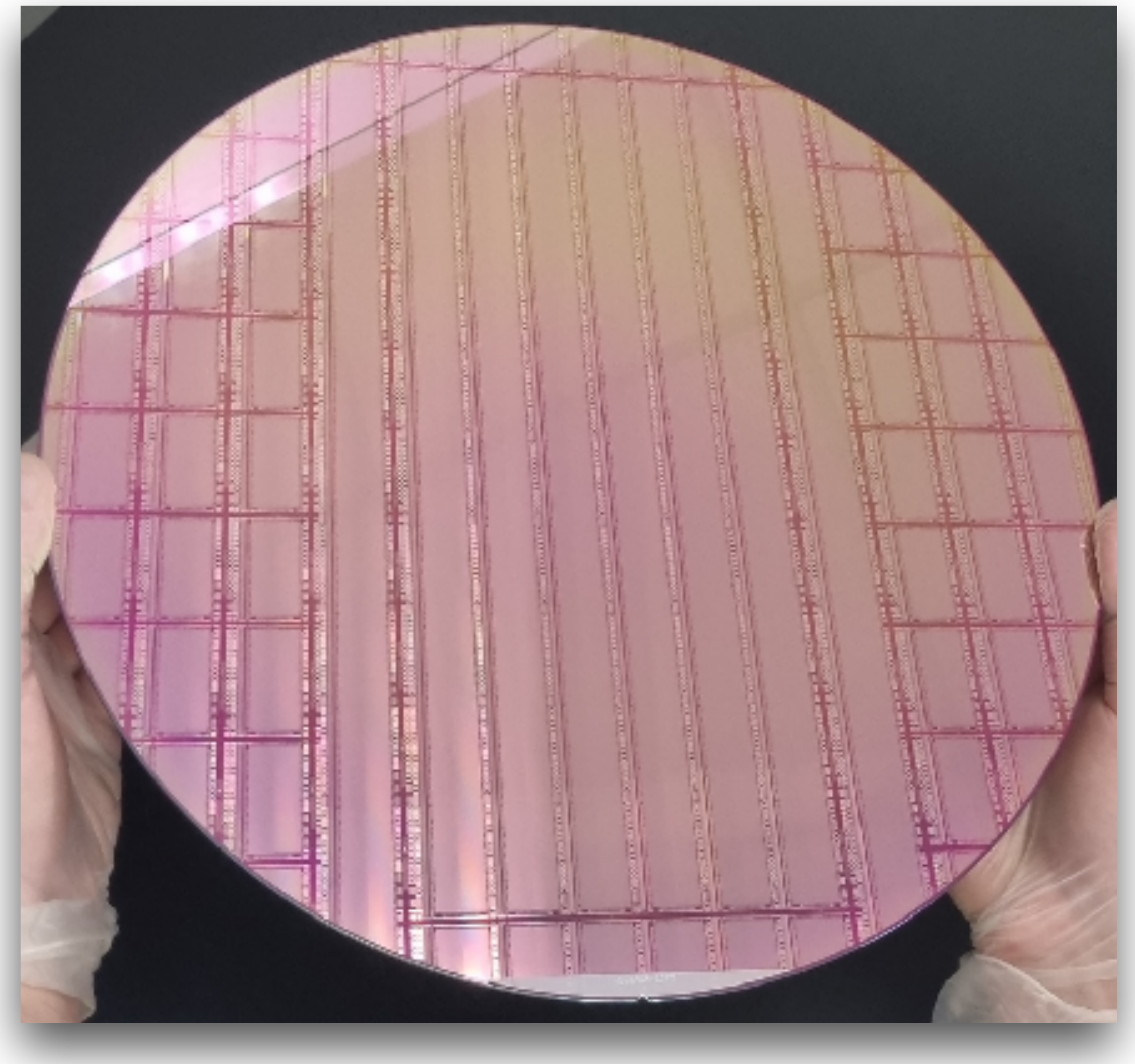
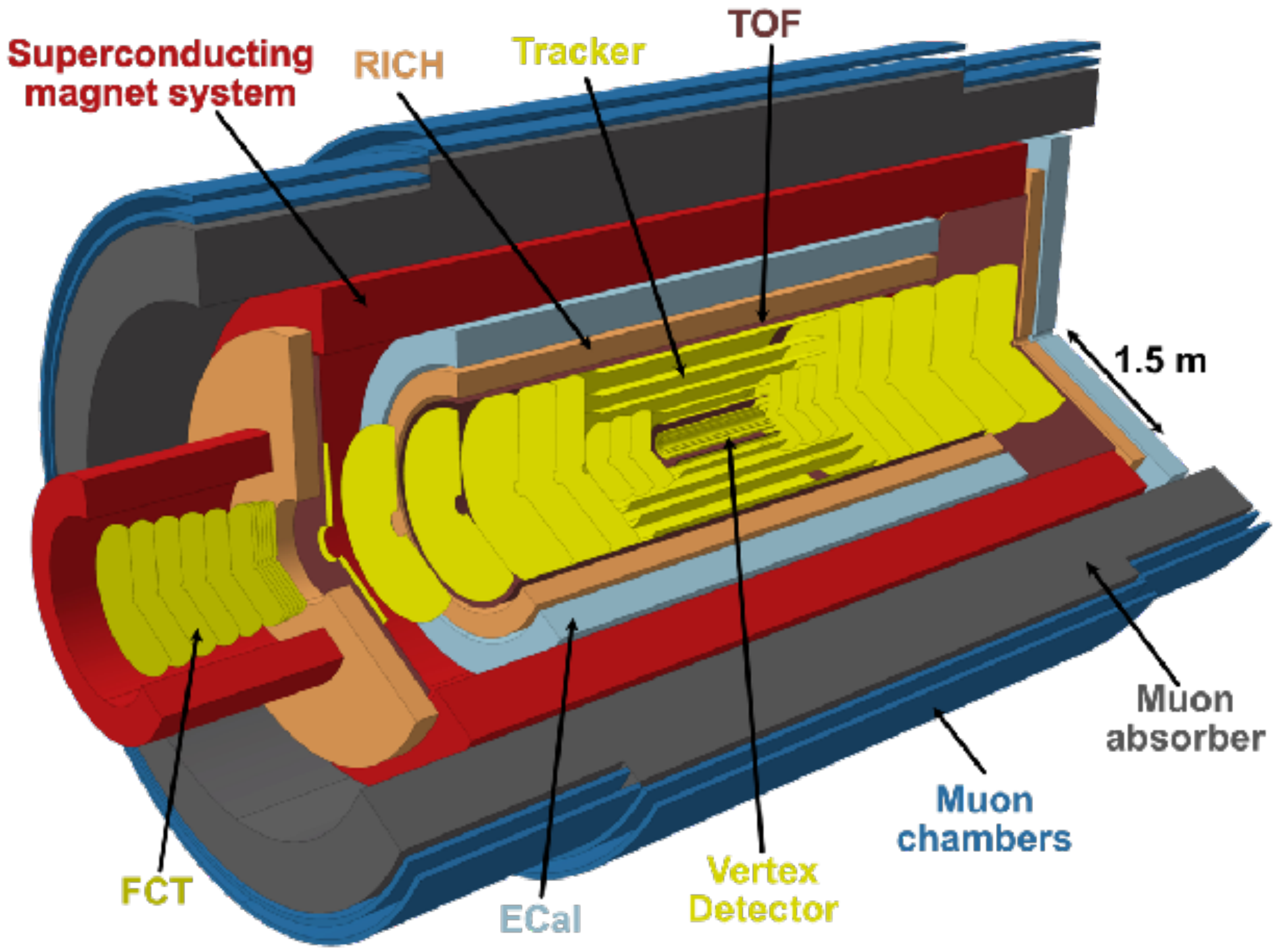
CMOS sensor R&D for next-generation vertex detector

Magnus Mager (CERN) ***on behalf of the ALICE collaboration***

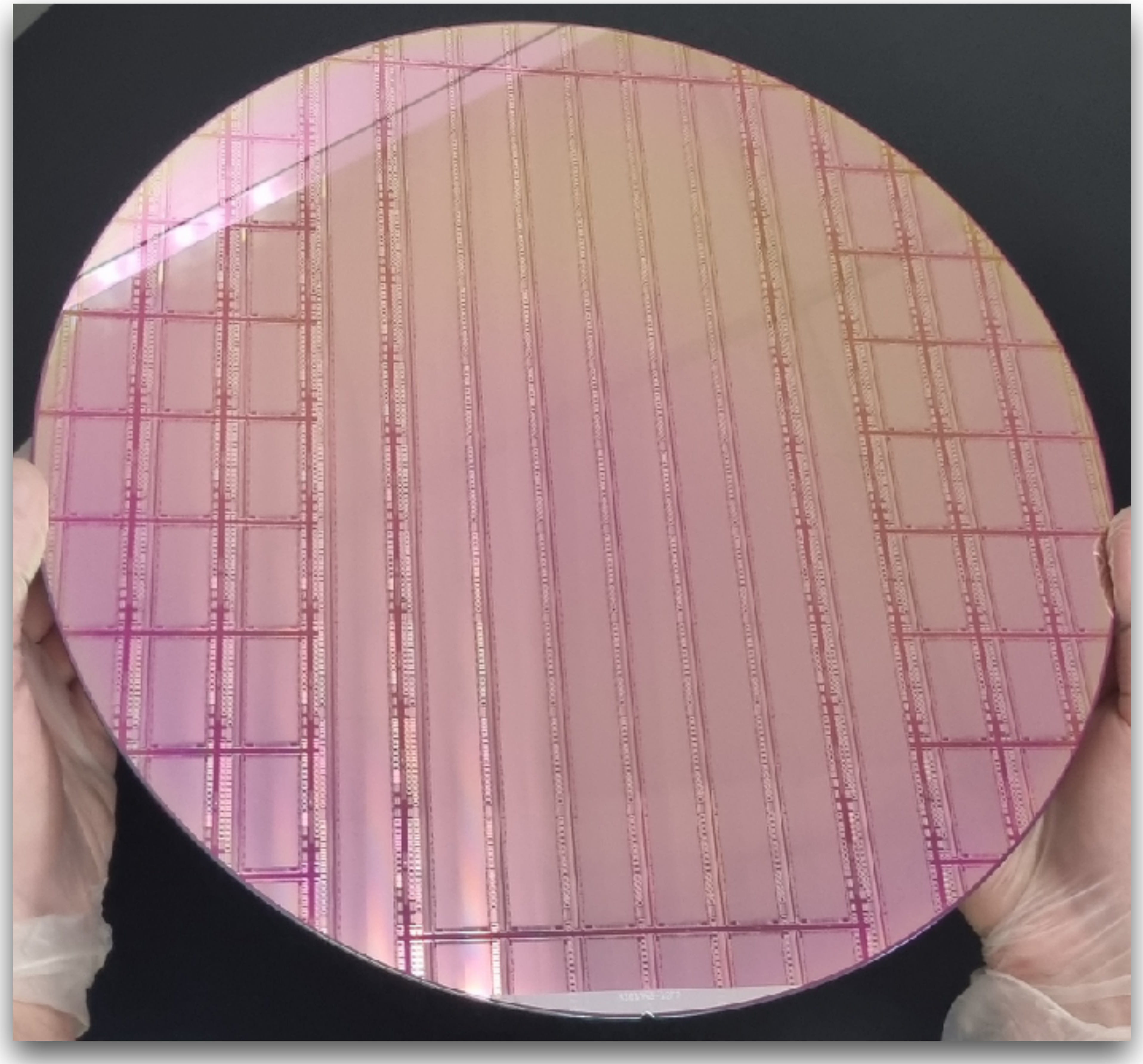
03.07.2023







Overview



[300 mm wafer with wafer-scale MAPS in 65 nm technology]

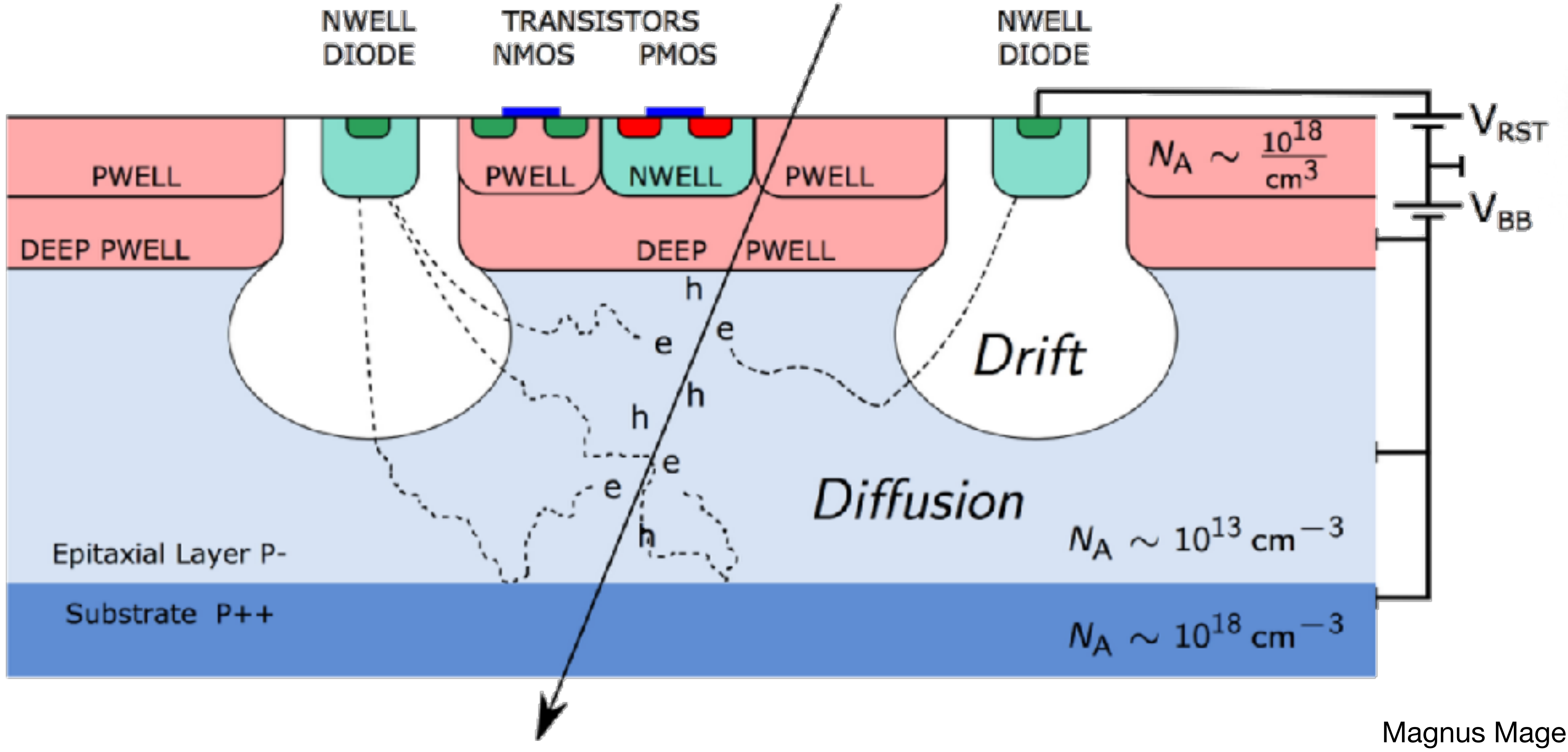
- **Intro**
  - monolithic Active Pixel Sensors (MAPS)
  - ALPIDE / ALICE ITS2
- **180 nm → 65 nm technology**
  - qualification of the technology
  - development of wafer-scale sensors
- **future ALICE applications**
  - ITS3
  - ALICE 3
- **Summary**

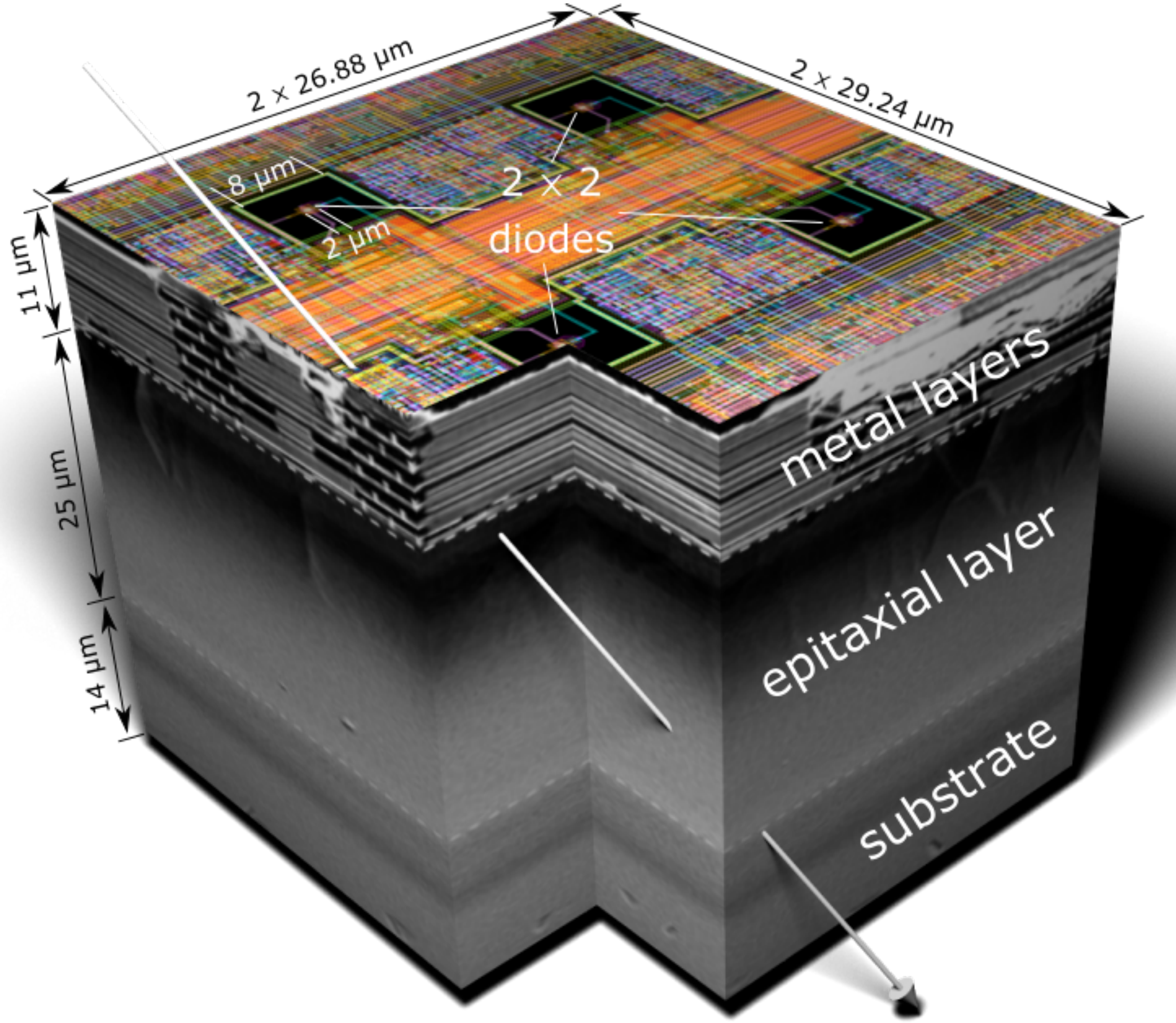
Monolithic Active Pixel Sensors (MAPS)

in a nutshell

- Single silicon chip contains both the detection volume and the readout electronics
  - as opposed to hybrid pixel sensors, which use two chips that need to be interconnected

- Advantages:
  - small pixel pitches: O(10-30 µm)
  - very low capacitances = low power O(10-100 mW/cm^2)
  - thin: <50 µm (0.05% X_0)
  - commercial process





ITS2: ALPIDE

> 70k chips produced and tested

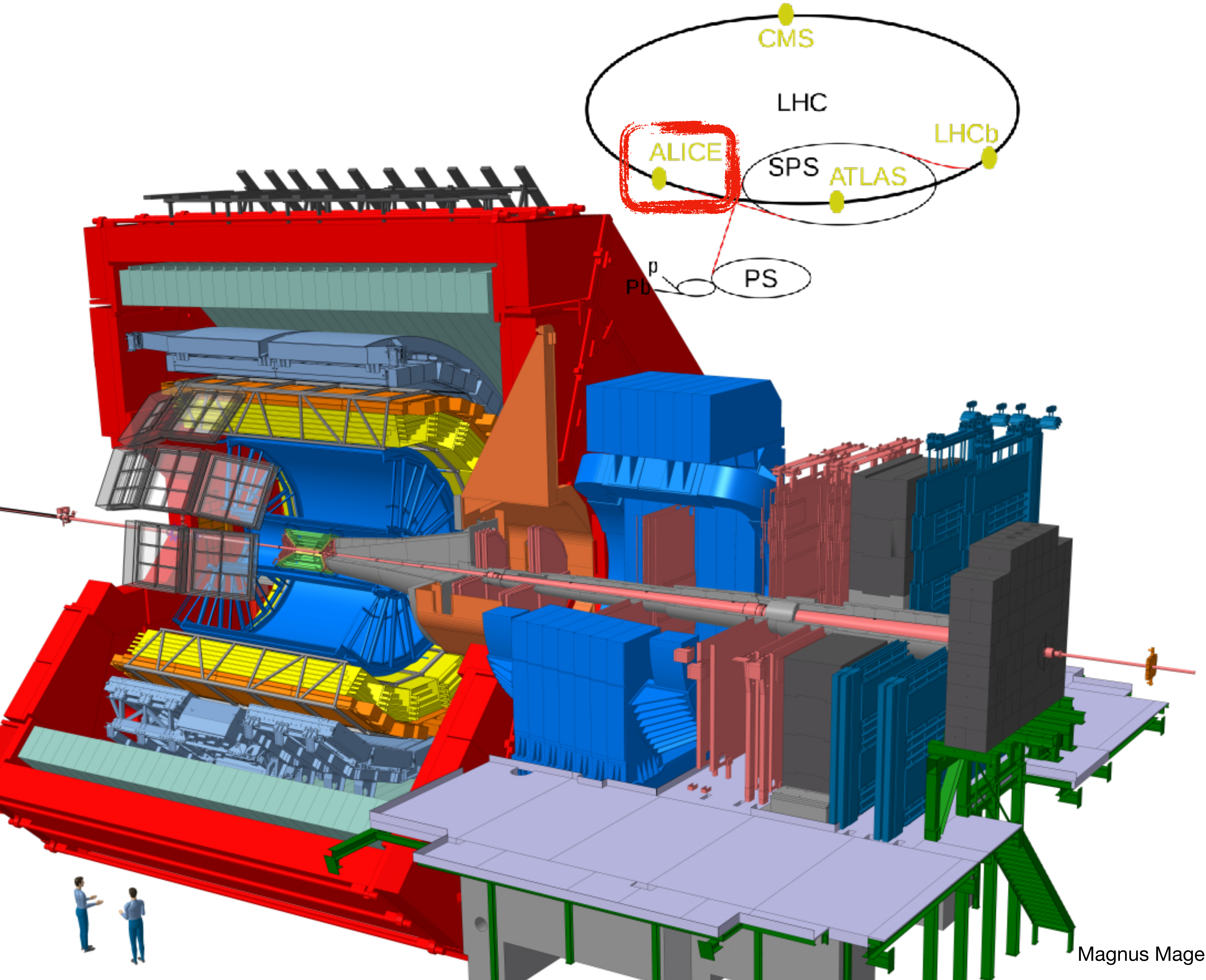
24k in continuous operation on ITS2

+ several other applications

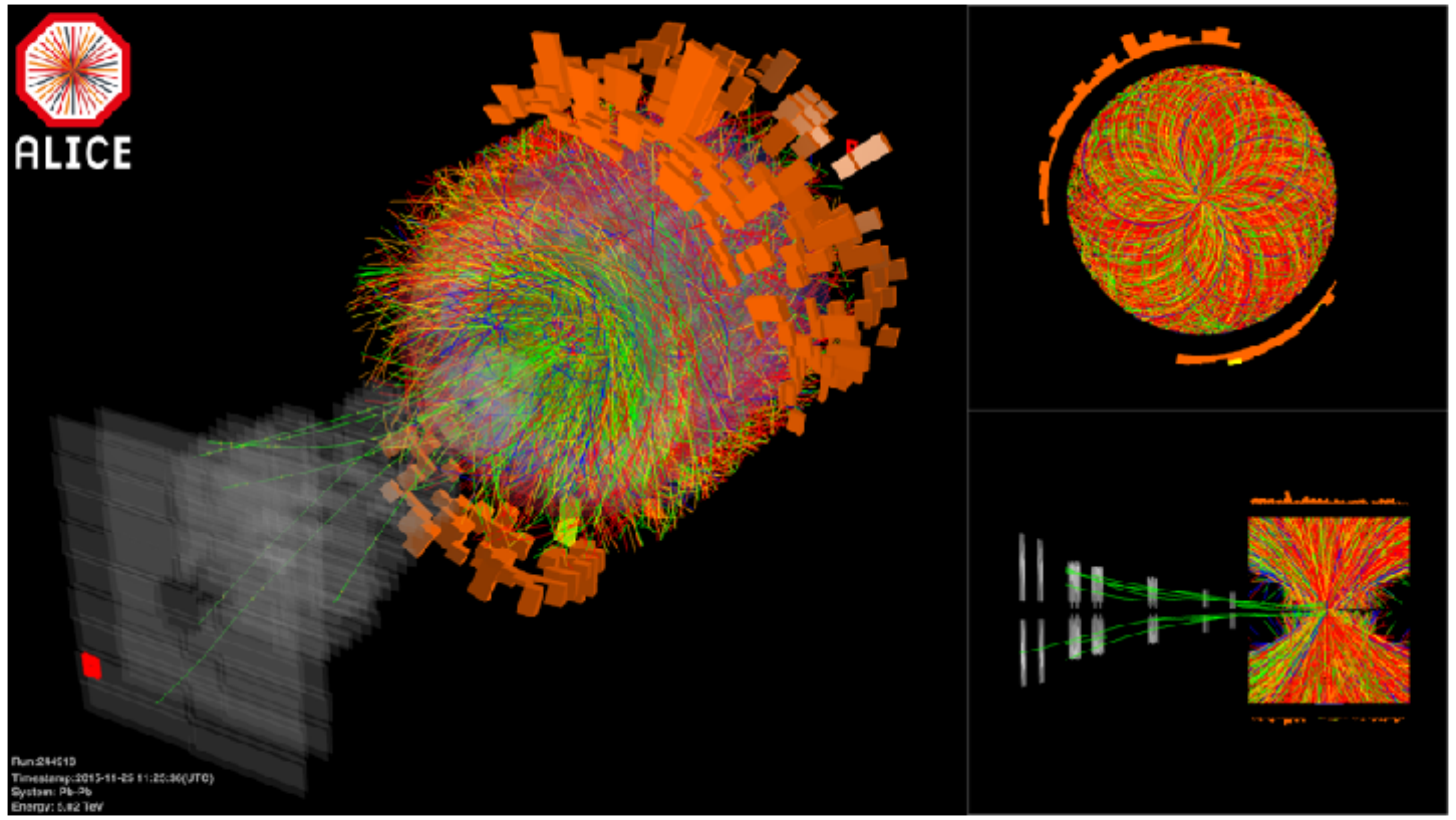
Parameter	Req.	ALPIDE
Spatial resolution (µm)	≈ 5	≈ 5
Integration time (µs)	< 30	< 10
Fake-hit rate (/pixel/event)	$< 10^{-6}$	$\ll 10^{-6}$
Detection efficiency	> 99%	>>99%
Power density (mW/cm^2)	< 100	< 40
TID (krad)	> 270 (IB)	OK
NIEL (1 MeV n_{eq} / cm^2)	$> 1.7\times10^{12}$	OK

ALICE

Detector and main goals

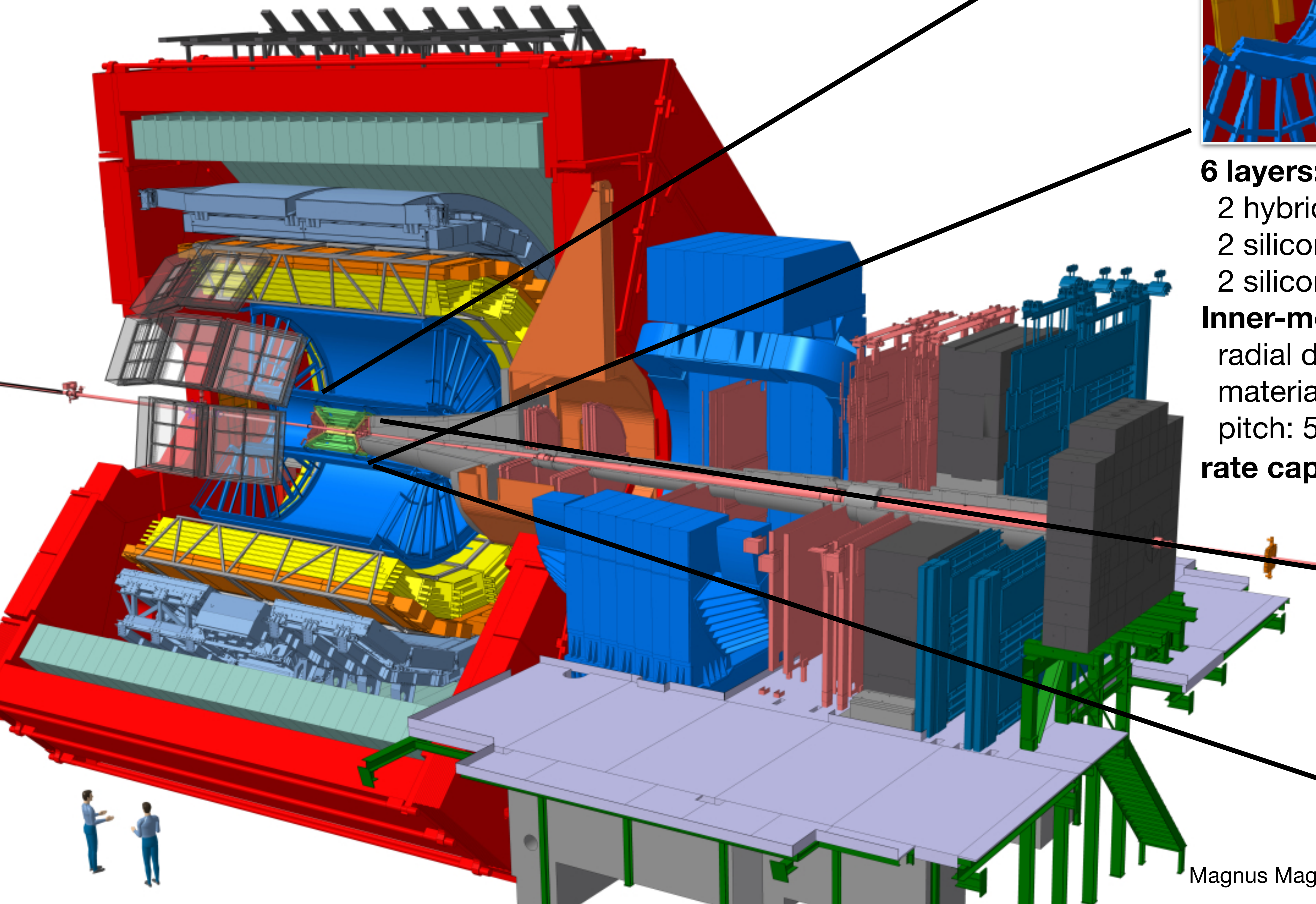


- Study of QGP in heavy-ion collisions at LHC
  - i.e. up to O(10k) particles to be tracked in a single event
- Reconstruction of charm and beauty hadrons
- Interest in low momentum (≲1 GeV/c) particle reconstruction

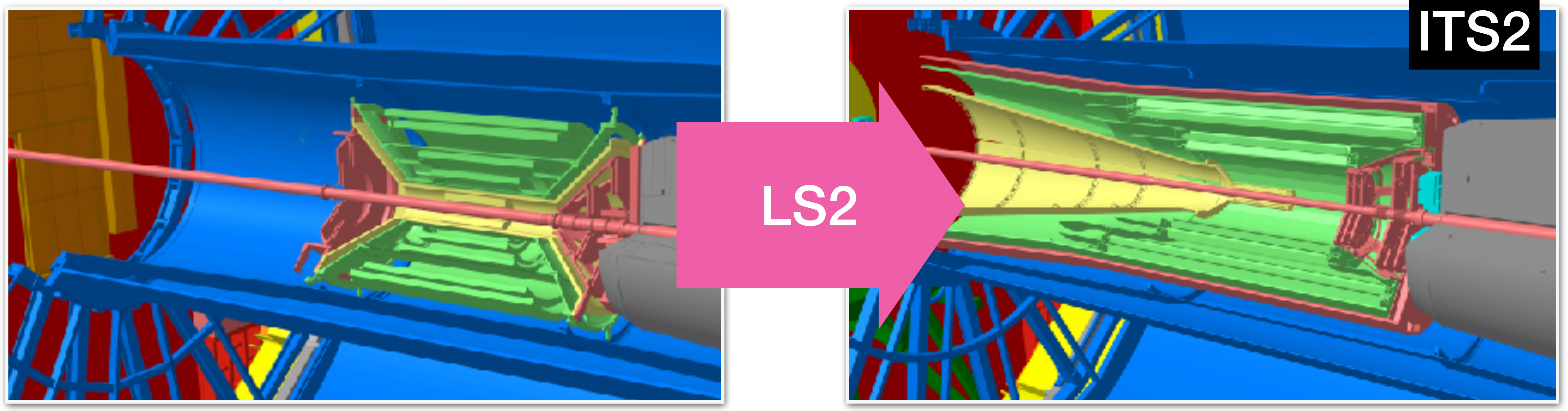


ALICE ITS2 + MFT

LS2 upgrades with Monolithic Active Pixel Sensors (MAPS)



Inner Tracking System



6 layers:
- 2 hybrid silicon pixel
- 2 silicon drift
- 2 silicon strip

Inner-most layer:
- radial distance: 39 mm
- material: $X/X_0 = 1.14\%$
- pitch: $50 \times 425\ \mu m^2$

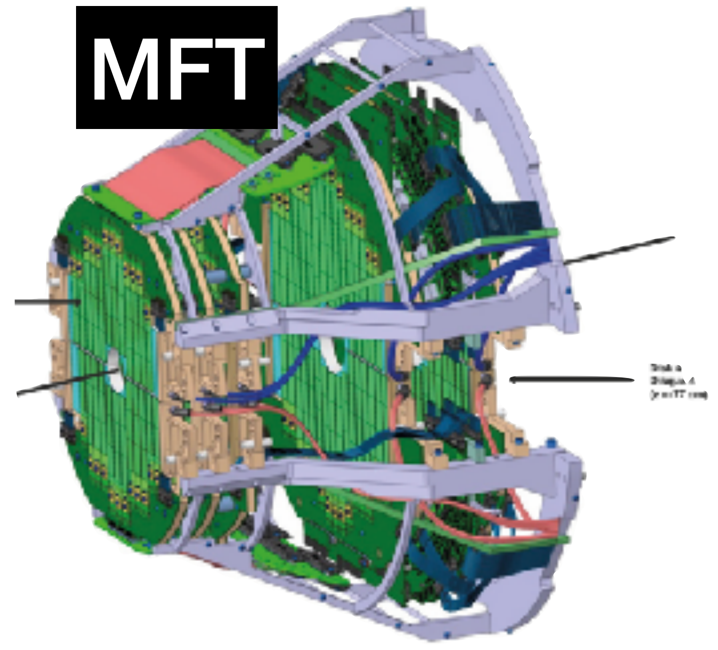
rate capability: 1 kHz

7 layers:
- all MAPS
- 10 m^2, 24k chips, 12.5 Giga-Pixels

Inner-most layer:
- radial distance: 23 mm
- material: $X/X_0 = 0.35\%$
- pitch: $29 \times 27\ \mu m^2$

rate capability: 100 kHz (Pb-Pb)

Muon Forward Tracker



new detector

5 discs, double sided:
- based on same technology as ITS2

ALICE ITS2 + MFT

LS2 upgr … ctive Pixel

CERN-LHCC-2012-013
(LHCC-P-005)
ALICE-UG-002
September 12, 2012

ALICE
Conceptual Design Report

Upgrade of the
Inner Tracking Sy
Conceptual

ALICE
Technical Design Report

CERN-LHCC-2013-024
ALICE-TDR-017
December 2, 2013

Upgrade of the
Inner Tracking System
Technical Design Report

CERNCOURIER
July/August 2021 cerncourier.com
Reporting on international high-energy physics

PIXEL
PERFECT

Exploring the Hubble tension
A CERN for climate change
Medical technologies

ALICE ITS2:

- 7 layers
- 10 m² MAPS
- 12.5 GPixel
- installed in Mar-May’21 (LHC LS2)

Pb-Pb 5.36 TeV
LHC22s period
18th November 2022
16:52:47.893

ITS2 offspring

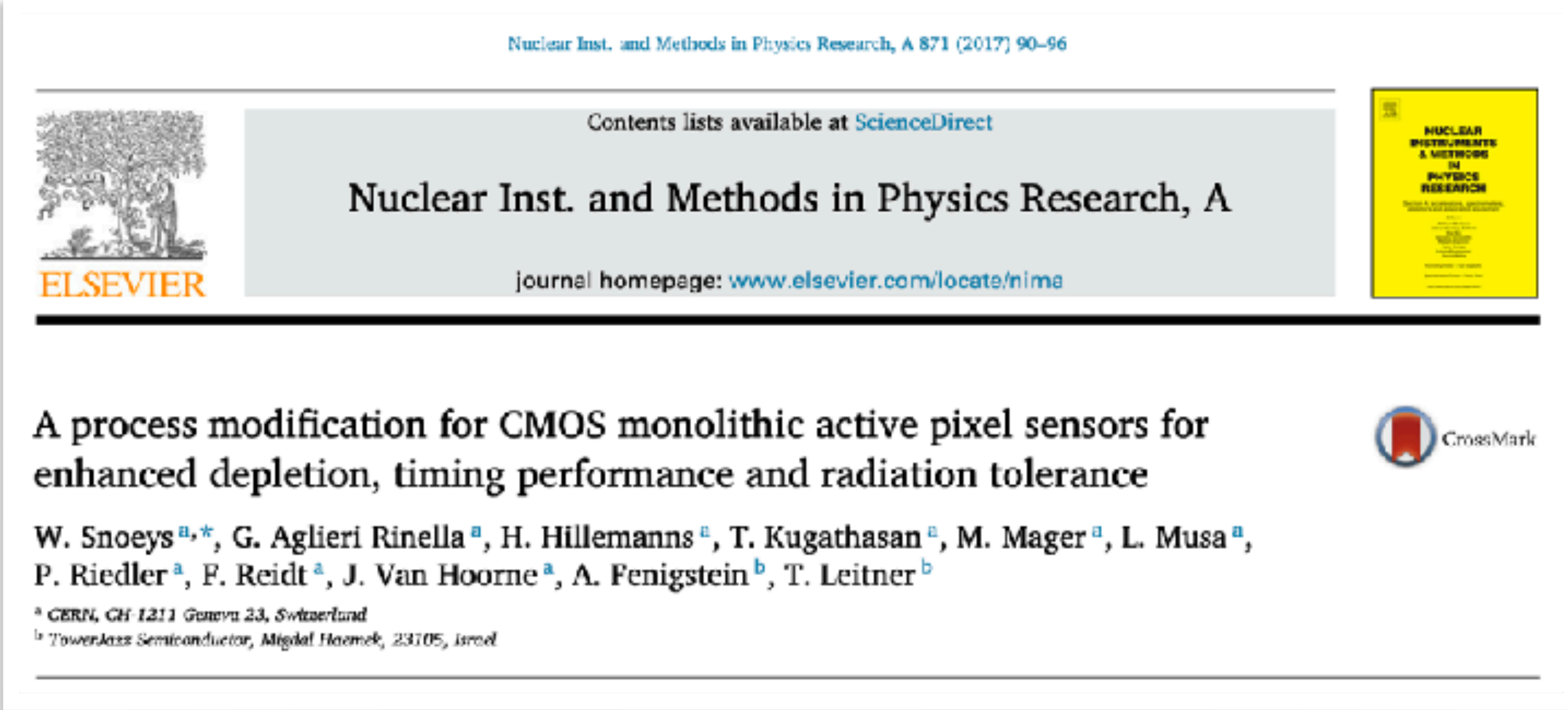
example: sPHENIX

replica of ITS2 Inner Barrel (3 layers) – installed in Mar’23

ITS2 R&D: process modification

full depletion as “side development”

- Addition of a **low-dose n-implant**
  - developed together with foundry
- Opens up new applications
  - higher radiation hardness
  - faster charge collection
- Now crucial for the 65 nm development (it paid off also for ALICE!)



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journal homepage: www.elsevier.com/locate/nima

ELSEVIER

A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance

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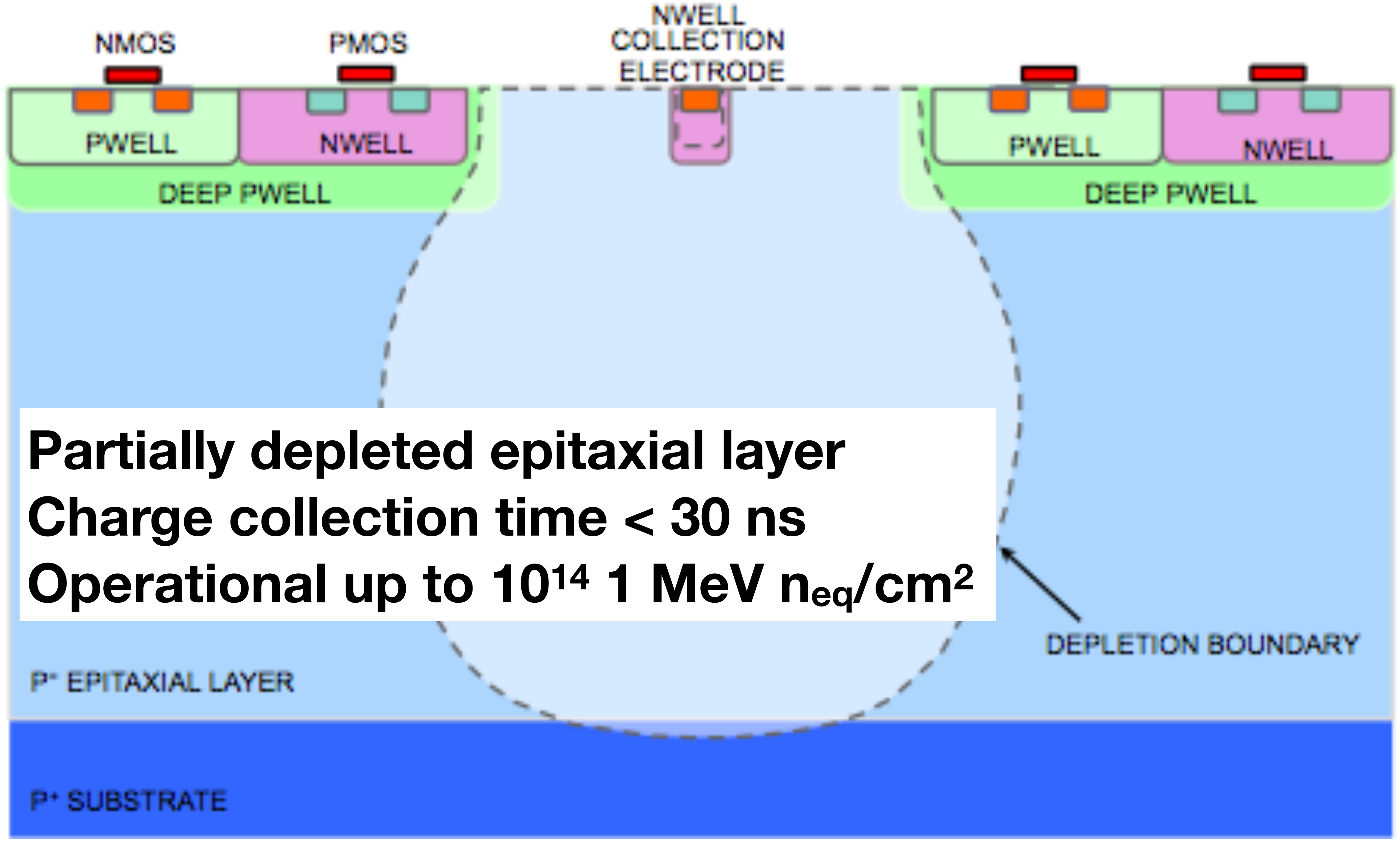
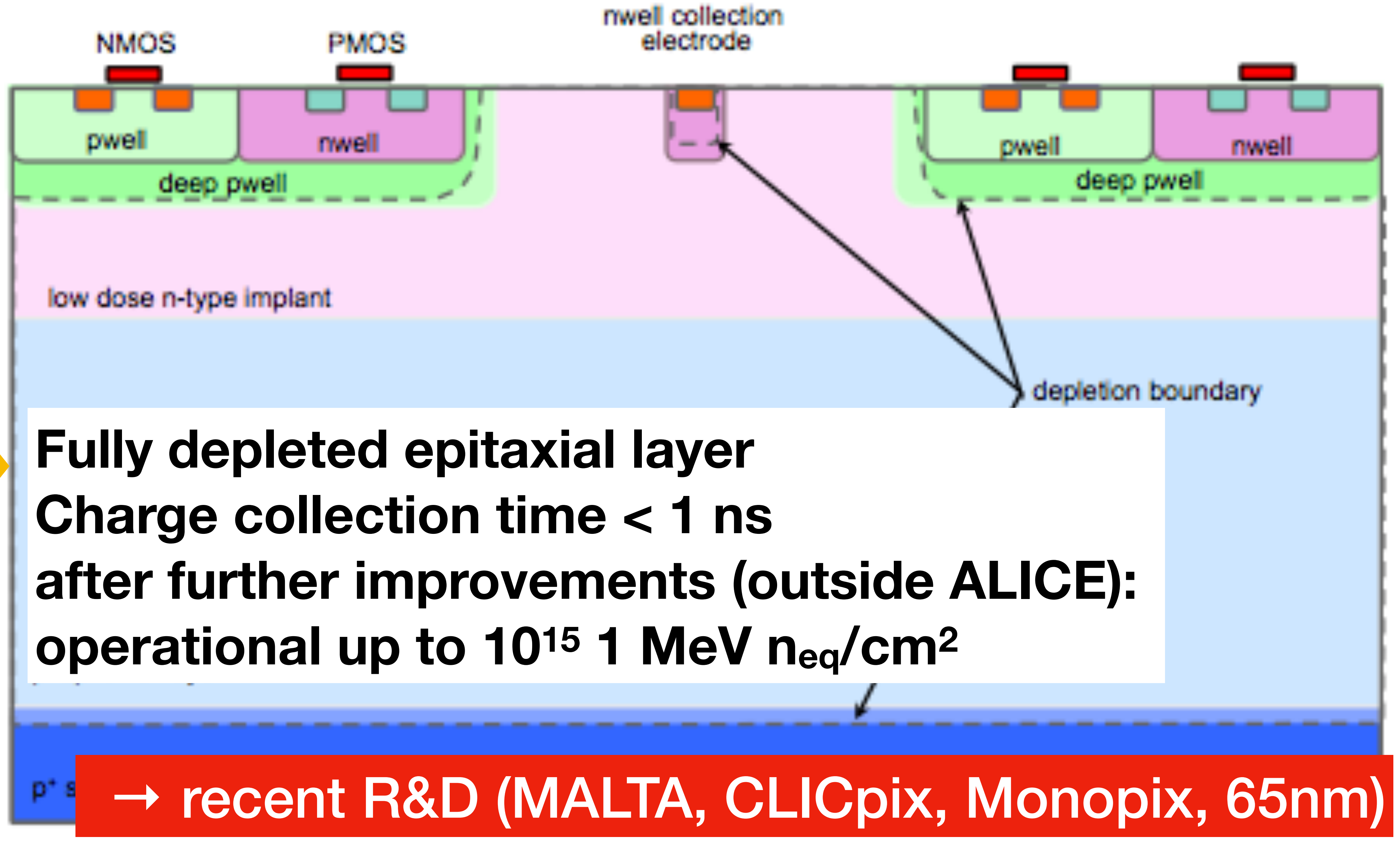
[doi:10.3390/s8095336]



Partially depleted epitaxial layer
Charge collection time < 30 ns
Operational up to 10^{14} 1 MeV n_{eq}/cm^2

Developed and prototyped within ALPIDE R&D



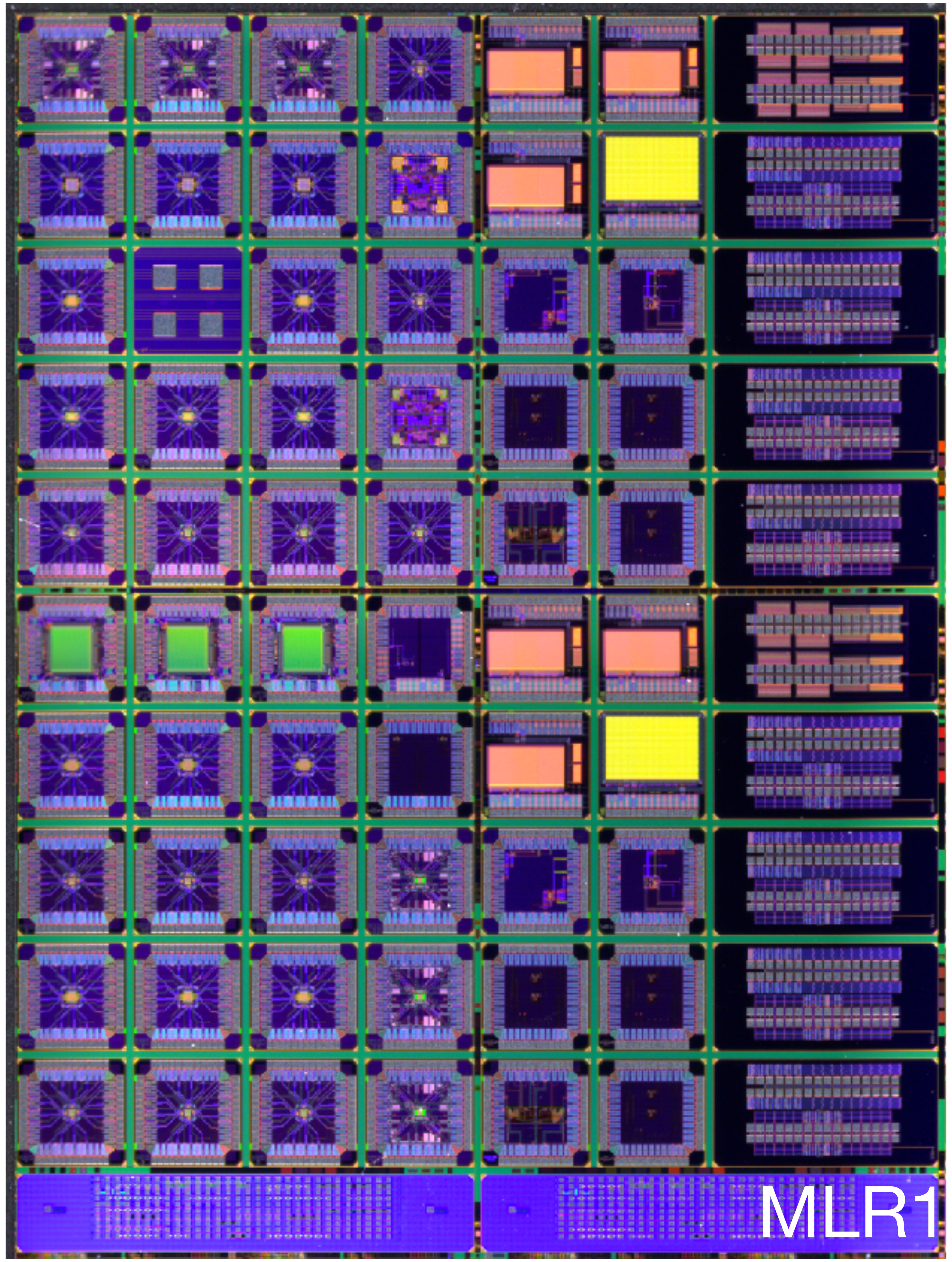
Fully depleted epitaxial layer
Charge collection time < 1 ns
after further improvements (outside ALICE):
operational up to 10^{15} 1 MeV n_{eq}/cm^2

→ recent R&D (MALTA, CLICpix, Monopix, 65nm)

Current R&D: 180 nm → 65 nm CMOS

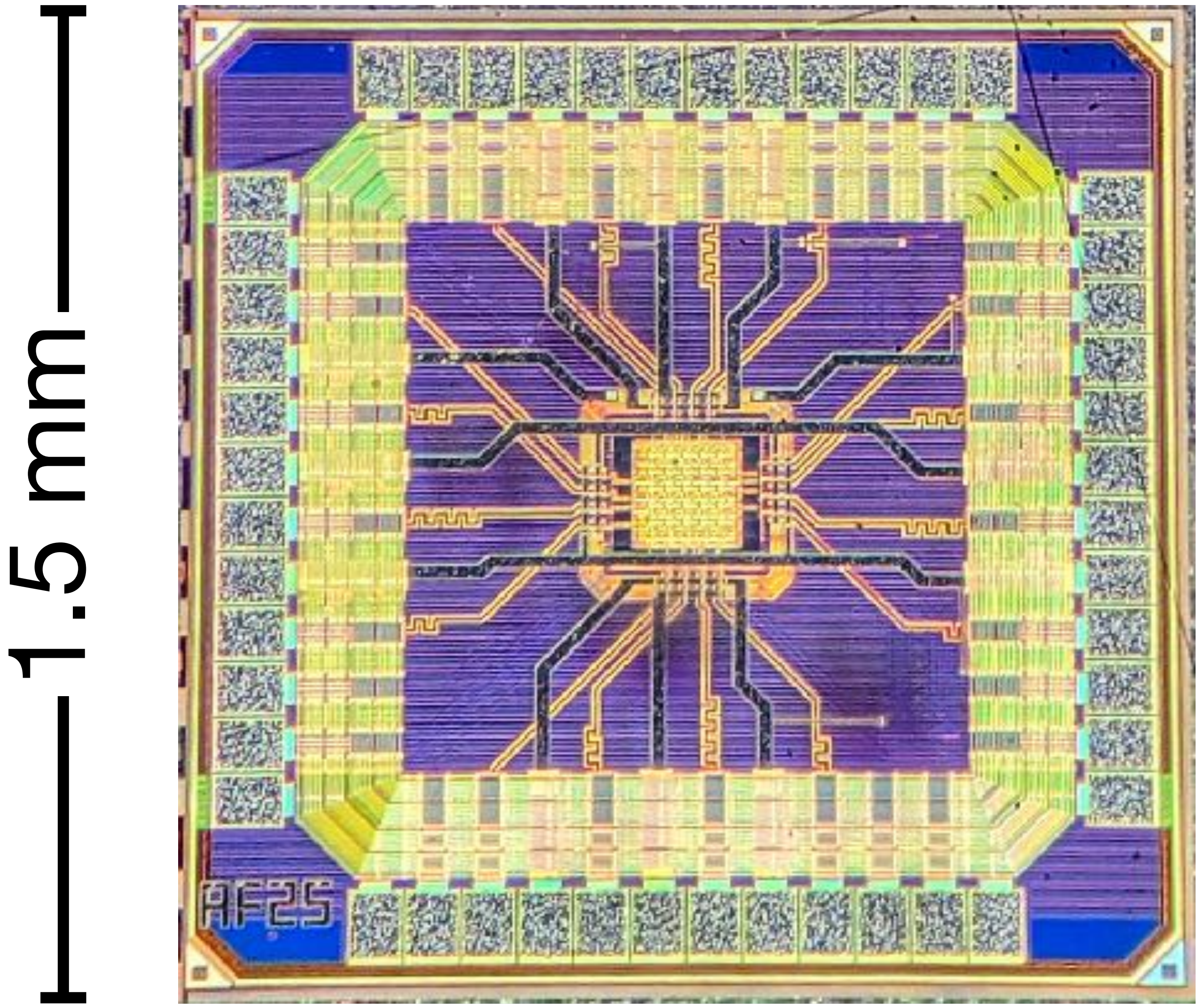
qualifying the TPSCo 65 nm CMOS imaging technology

- Concentrated effort **ALICE ITS3** together with **CERN EP R&D**
- **Key benefits**
  - smaller features/transistors: higher integration density
  - smaller pitches
  - lower power consumption
  - **larger wafers** (200→300 mm)
- **MLR1:**
  - comprehensive *first* submission: **55** prototype chips
  - goal: qualify the technology (achieved)
- **ER1:**
  - goal: first test of stitching aka **wafer-scale chips**
  - chips are back and testing has starded



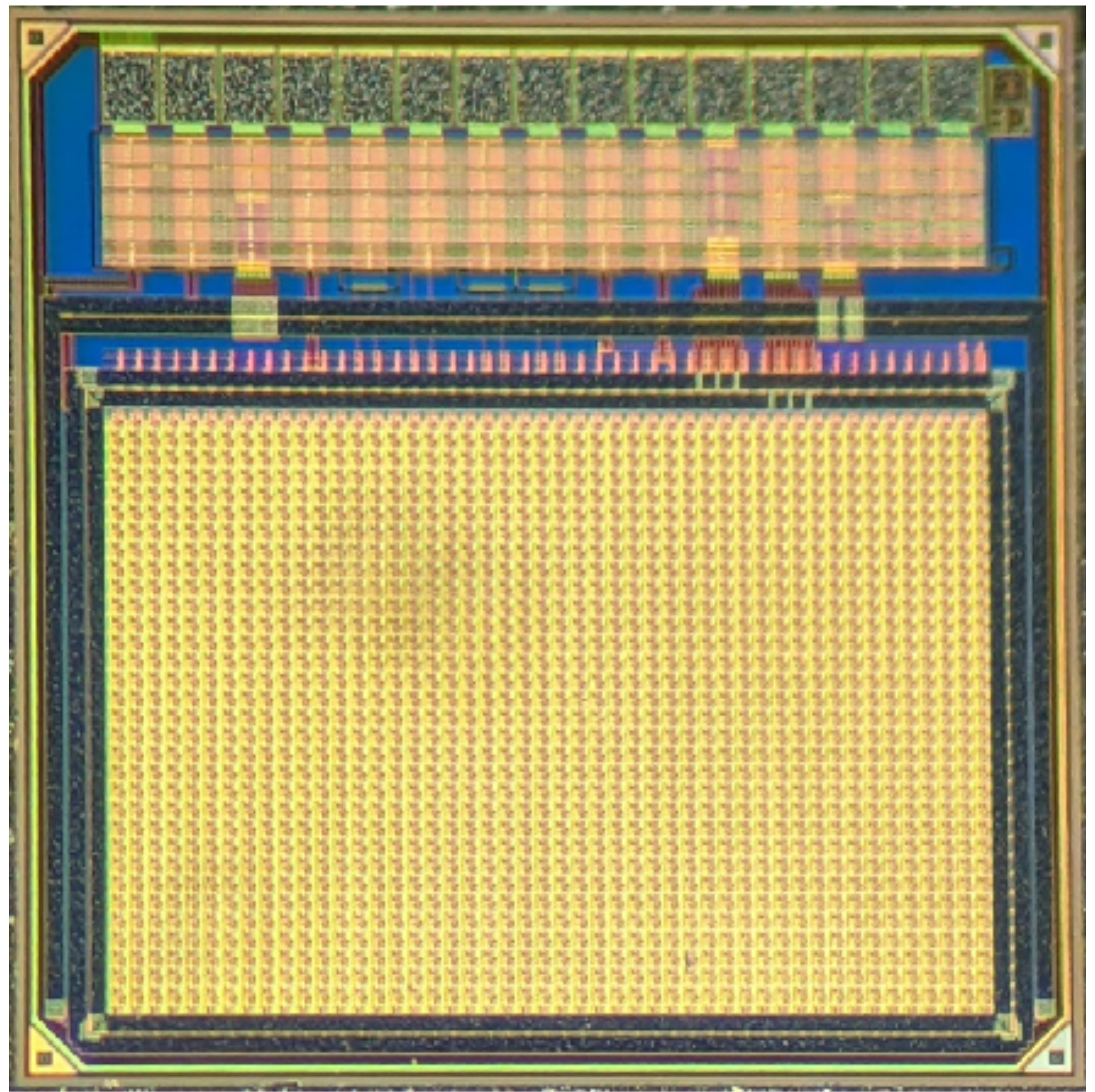
ITS3: pixel prototype chips (selection)

APTS



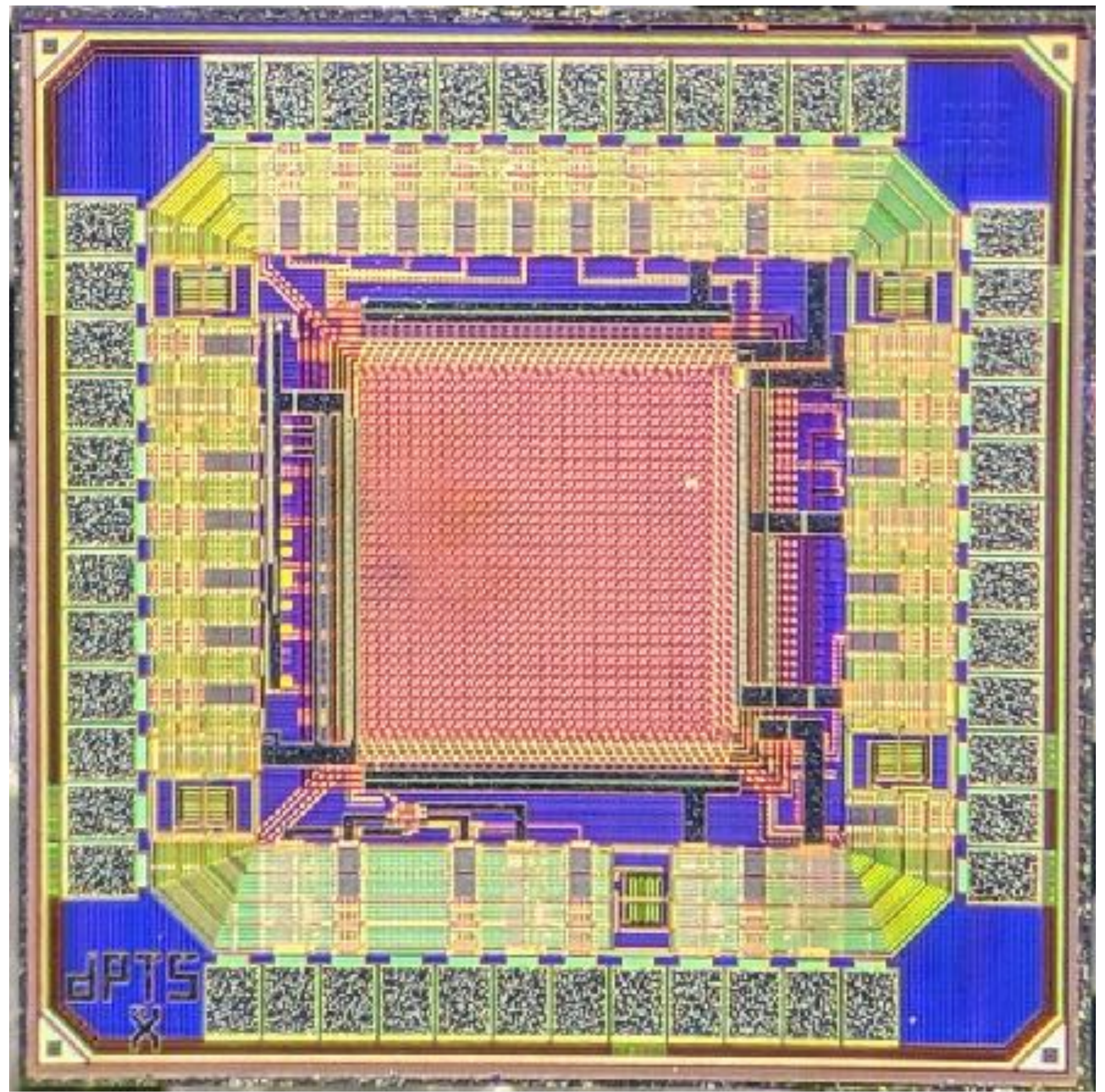
- **matrix:** 6x6 pixels
- **readout:** direct analog readout of central 4x4
- **pitch:** 10, 15, 20, 25 µm
- **total:** 34 dies

CE65



- **matrix:** 64x32, 48x32 pixels
- **readout:** rolling shutter analog
- **pitch:** 15, 25 µm
- **total:** 4 dies

DPTS

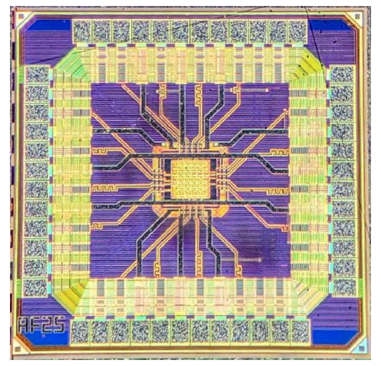


- **matrix:** 32x32 pixels
- **readout:** async. digital with ToT
- **pitch:** 15 µm
- **total:** 3 dies

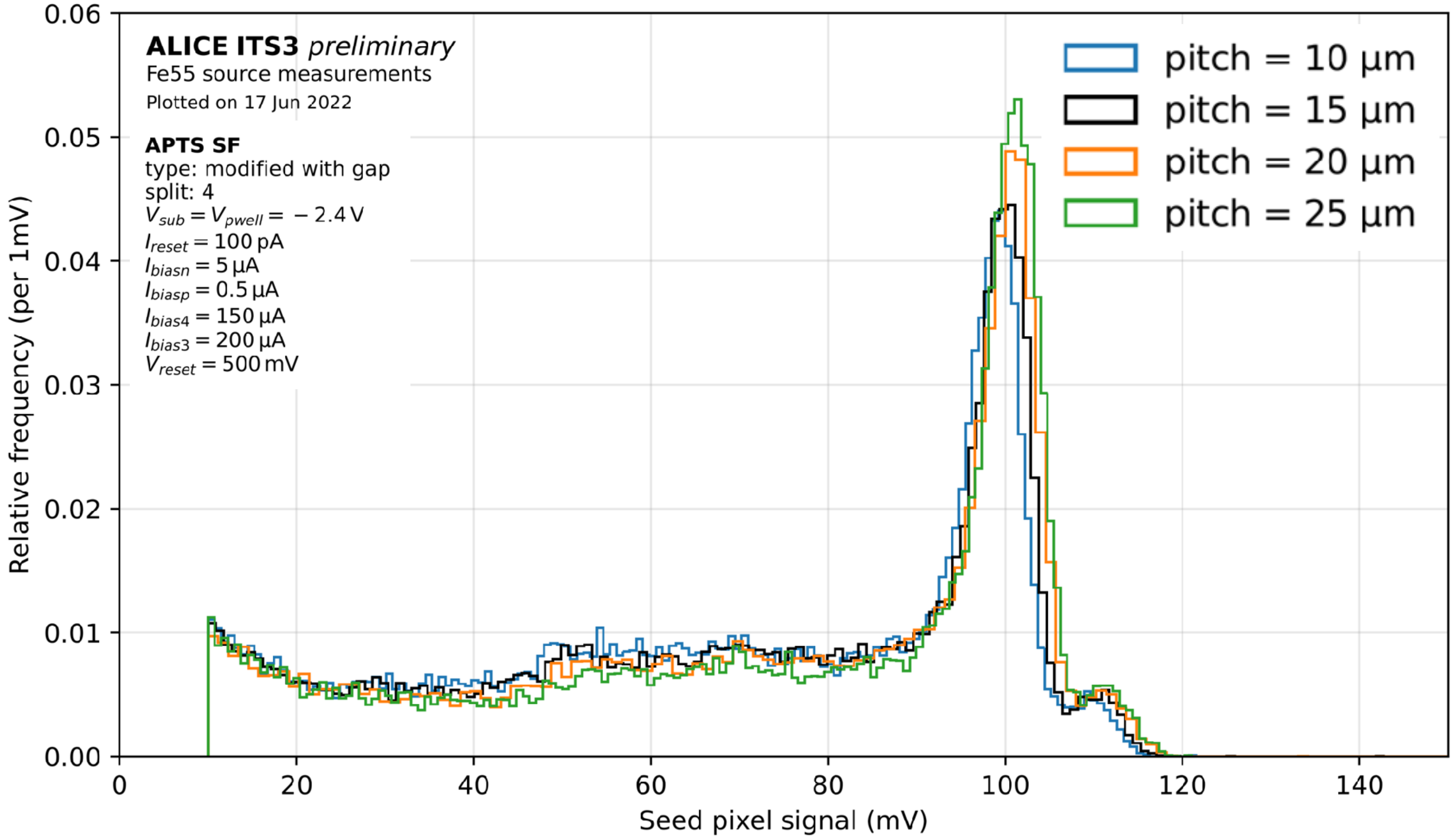
Comprehensive set of (small) prototypes and variants to explore the technology for particle detection

APTS – Fe-55 lab tests

comparison of pitches



- Process modification was introduced:
  - full depletion of sensors
  - electric field pointing to collection electrodes
- Pixels of pitches of 10-25 µm show similar results
  - indicates that the charge collection is very efficient
- Allows to *choose* optimal pitch for the final sensor

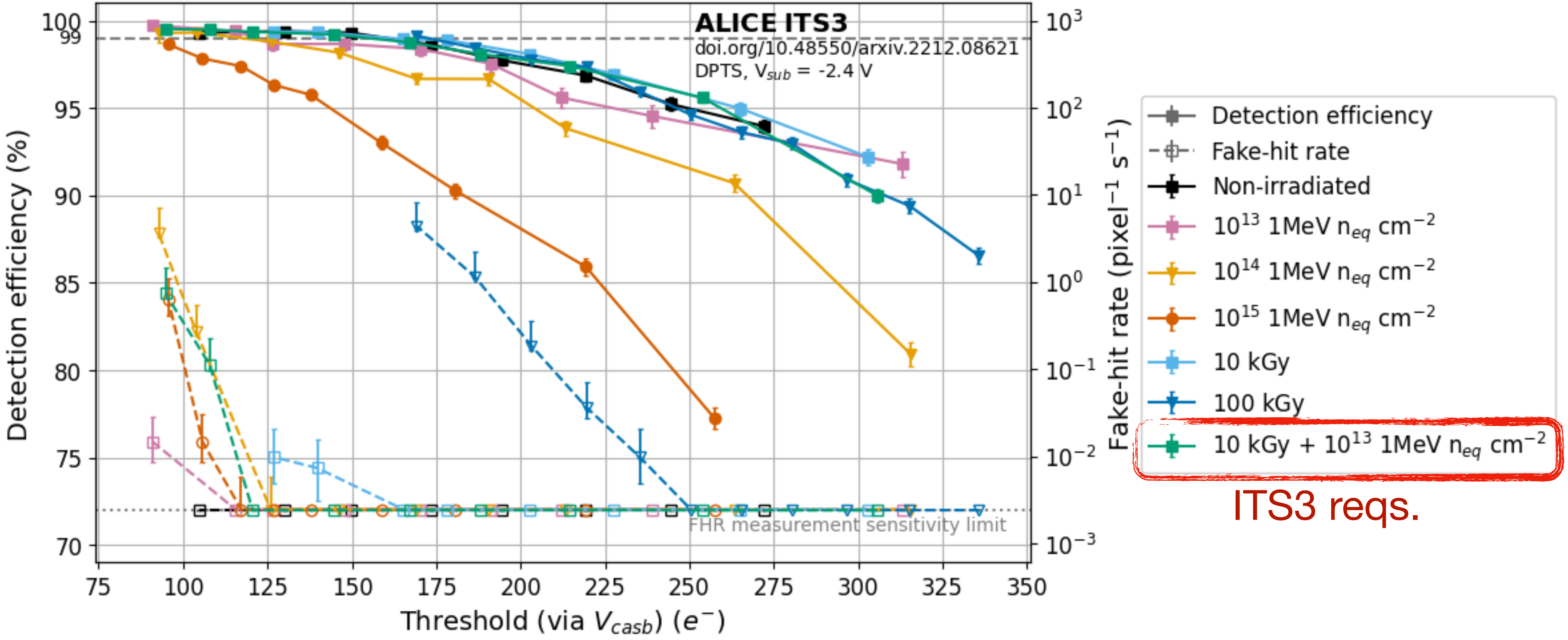


This is a remarkable result — showing that we have very efficient charge collection

Detection efficiency

Digital pixel test chip (“DPTS”)

[doi:10.48550/arXiv.2212.08621]



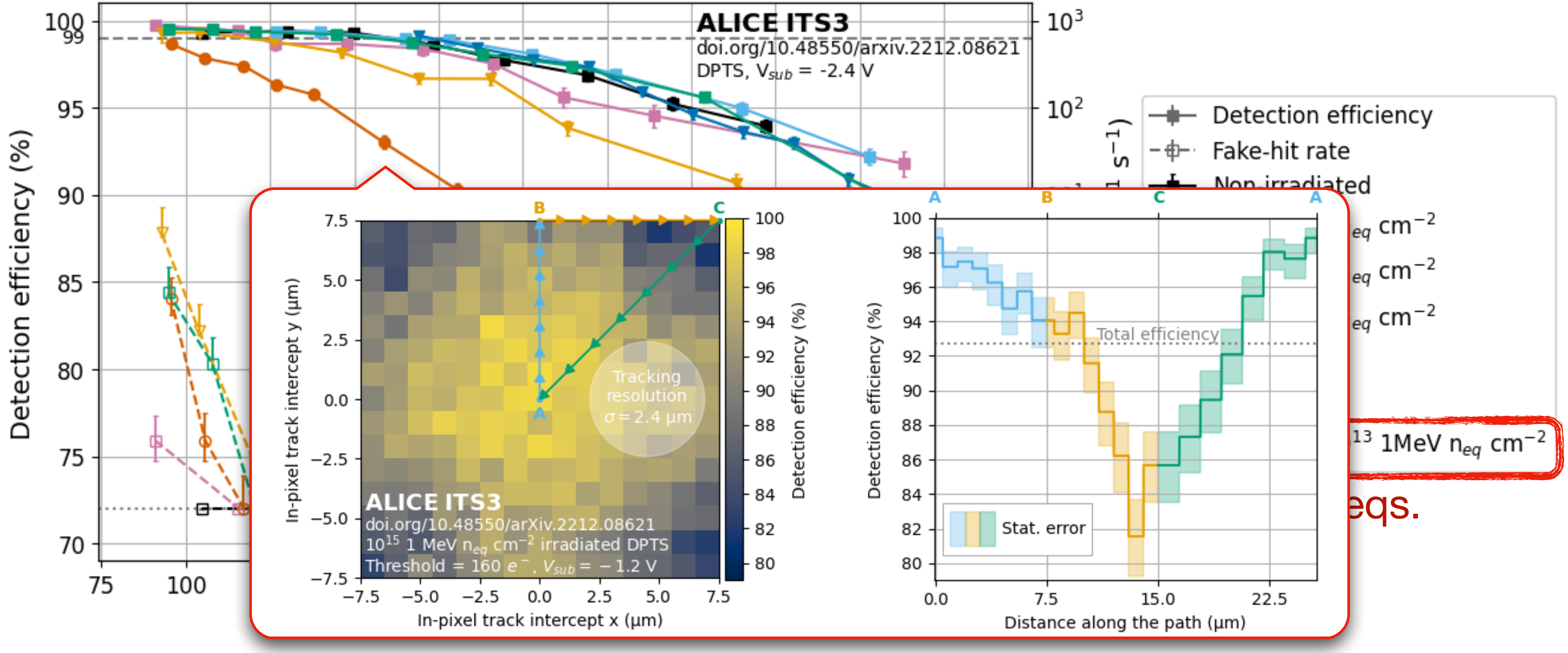
ITS3 reqs.

First comprehensive paper on 65 nm — summarises 1 year of measurements

Detection efficiency

Digital pixel test chip ("DPTS")

[doi:10.48550/arXiv.2212.08621]

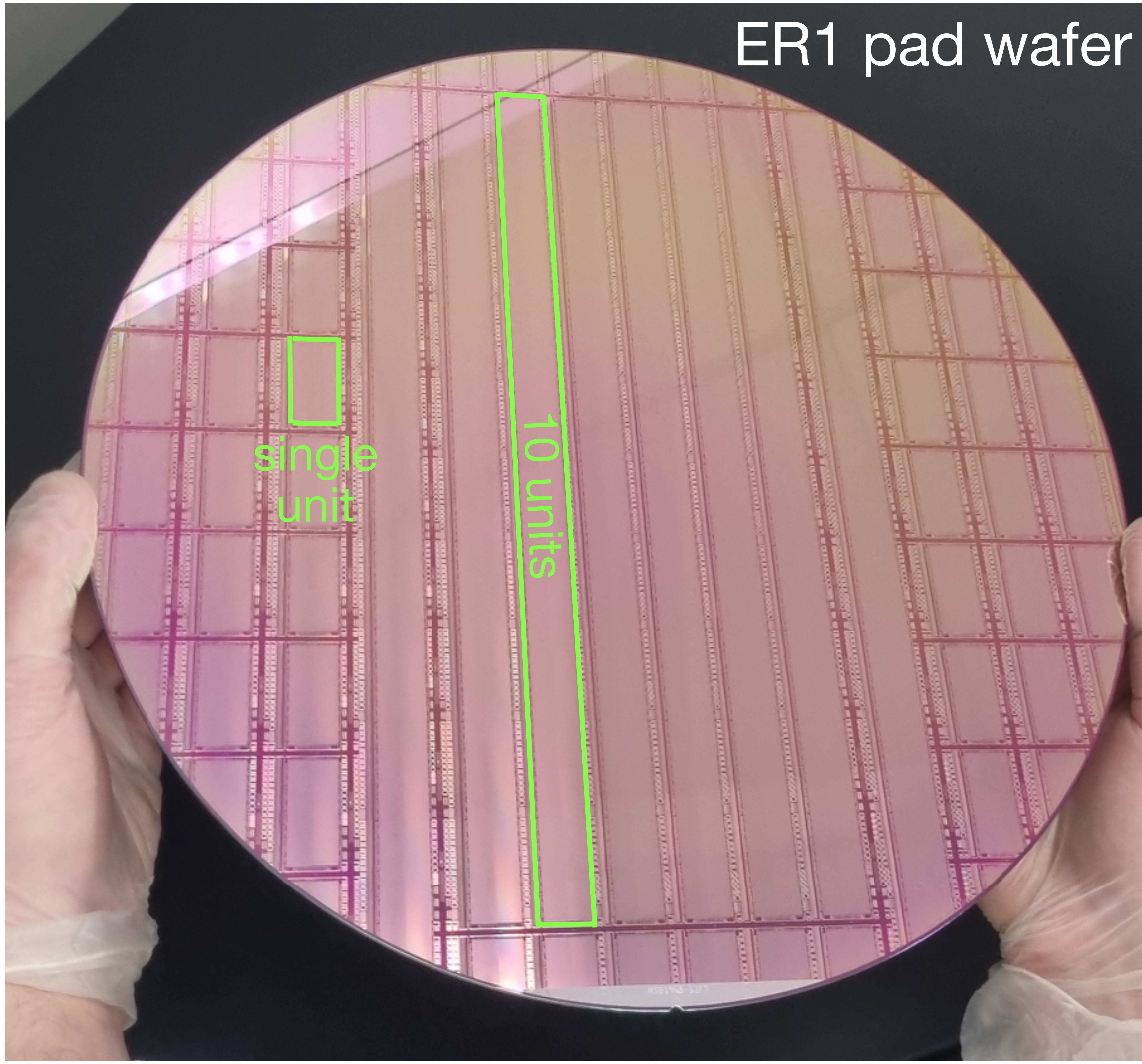


First comprehensive paper on 65 nm — summarises 1 year of measurements

ITS3: Wafer-scale sensors

Engineering Run 1 (ER1)

- First MAPS for HEP using stitching
  - one order of magnitude larger than previous chips
- "**MOSS**": 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 μm²)
  - conservative design, different pitches
- "**MOST**": 2.5 x 259 mm, 0.9 MPixel (18 x 18 μm²)
  - more dense design
- Plenty of small chips (like MLR1)



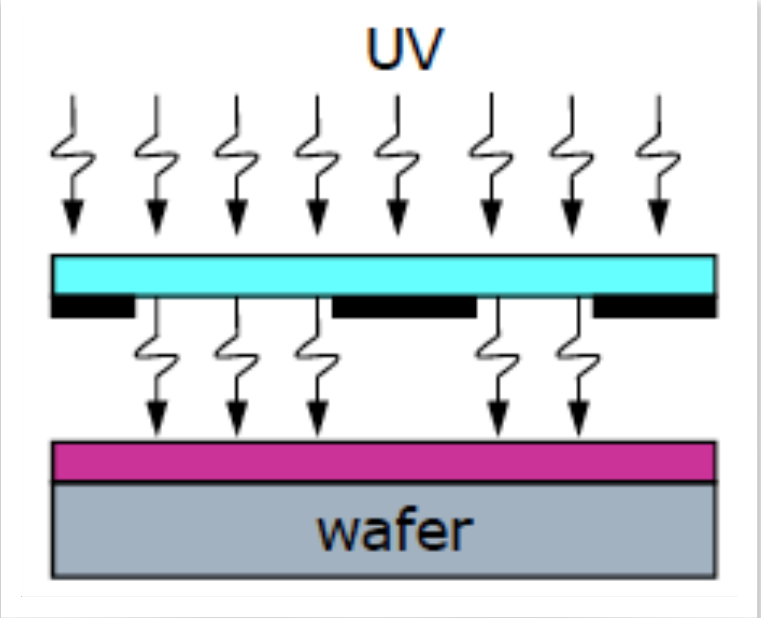
Wafer-scale sensors

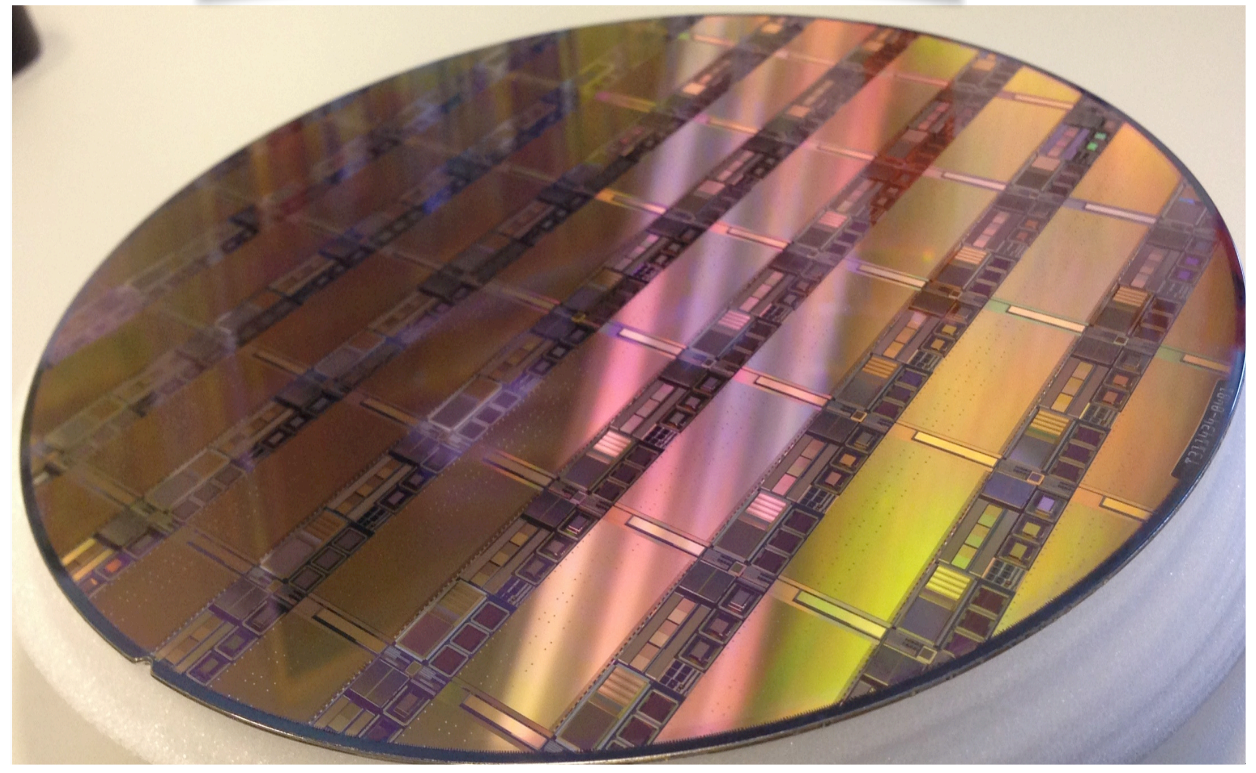
benefits and challenges

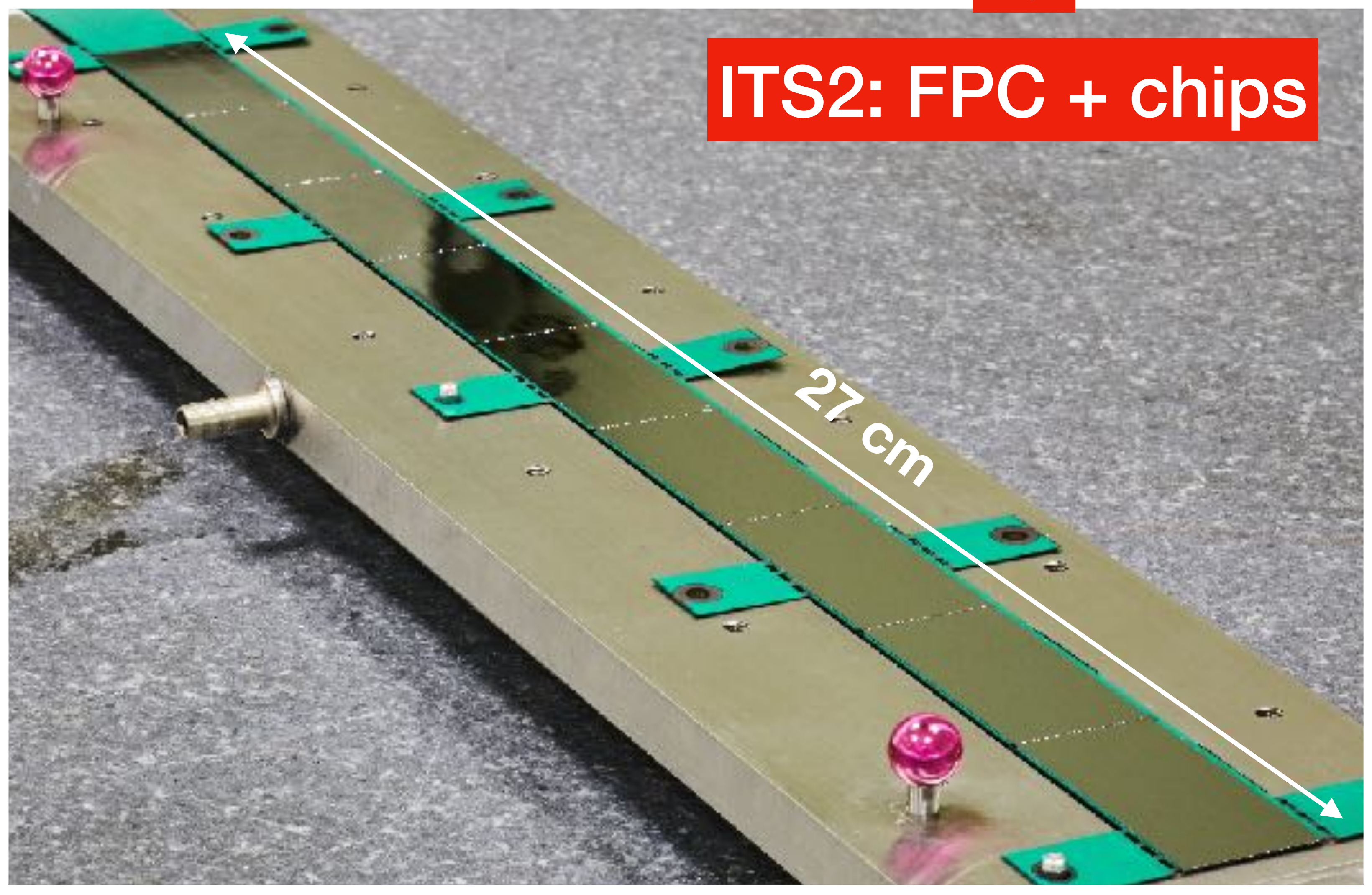
- **Previous** chip sizes are O(1-3 by 1-3 cm^2)
  - dictated by mask size
  - masks are exposed once for each chip
- Chips diced out and qualified/selected
- Interconnection on circuit boards (“modules”)

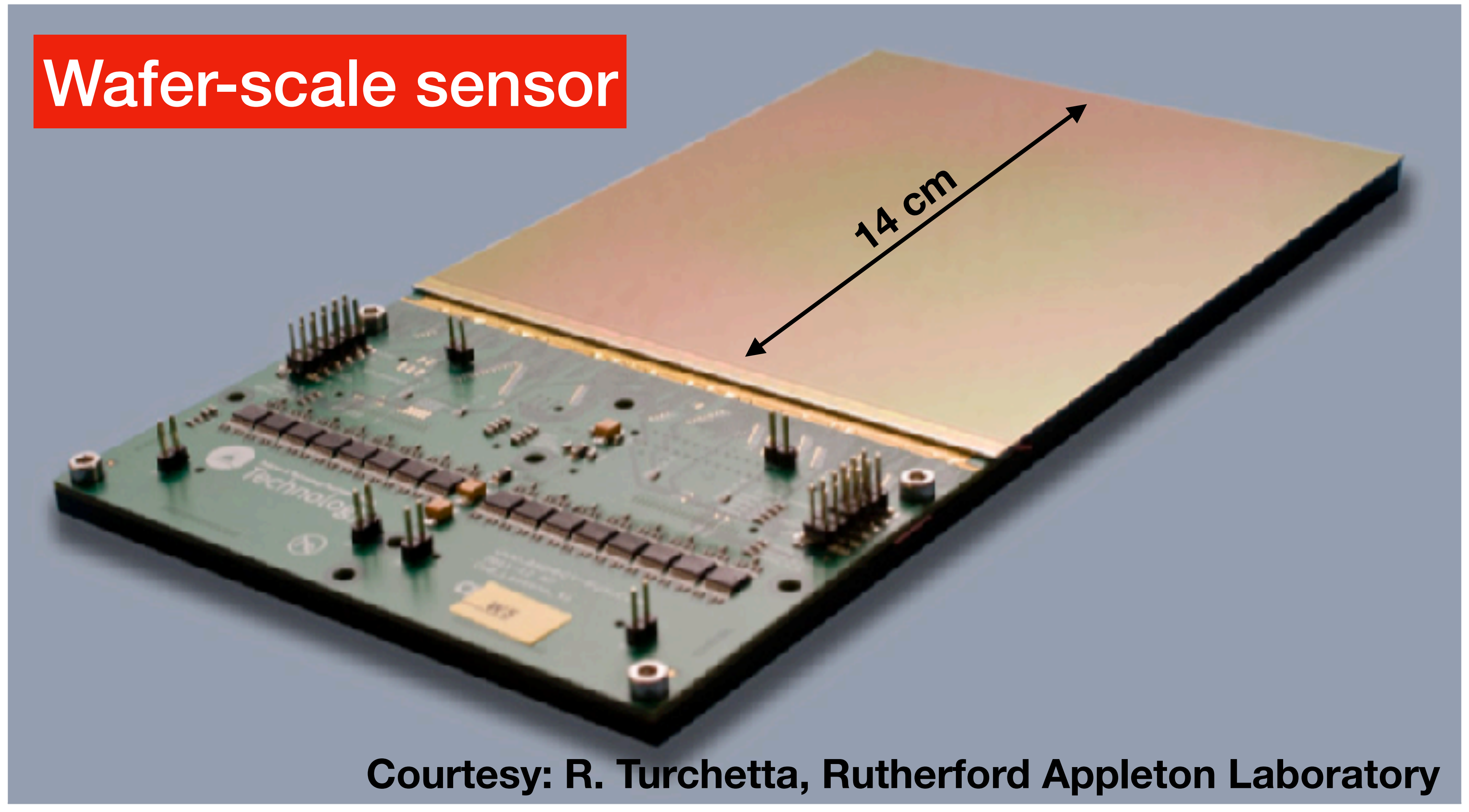
dedicated desing effort

- **Wafer-scale** “chips”/sensors: stitching of exposures
  - same mask exposed in a precisely aligned fashion
  - design is made periodic (metal lines stitch together)
  - *(edges and corners need attention)*
- Monolithic entity: more sensitive to manufacturing defects (yield)
- All interconnection is done on the wafer: denser, but also less conductive







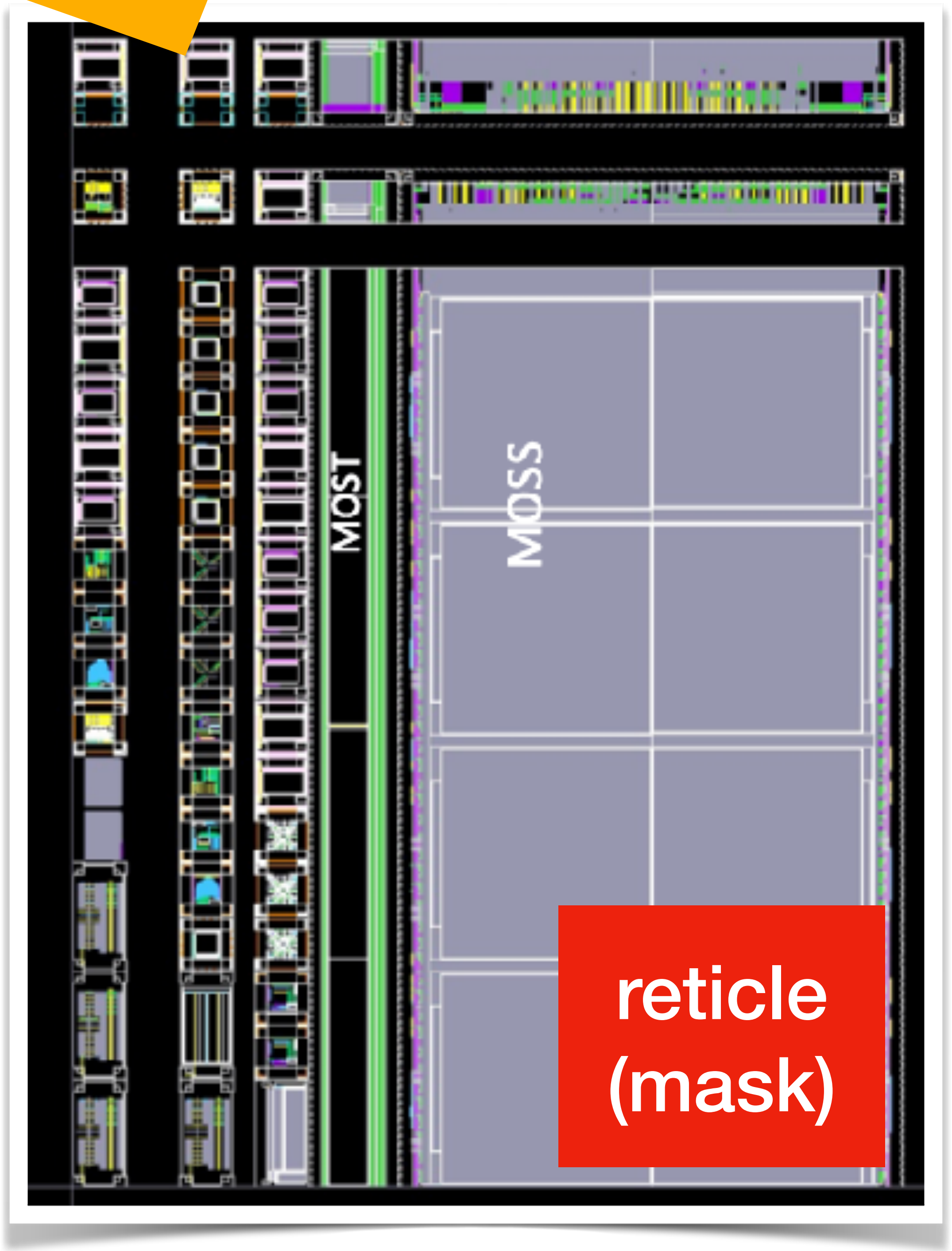


Courtesy: R. Turchetta, Rutherford Appleton Laboratory

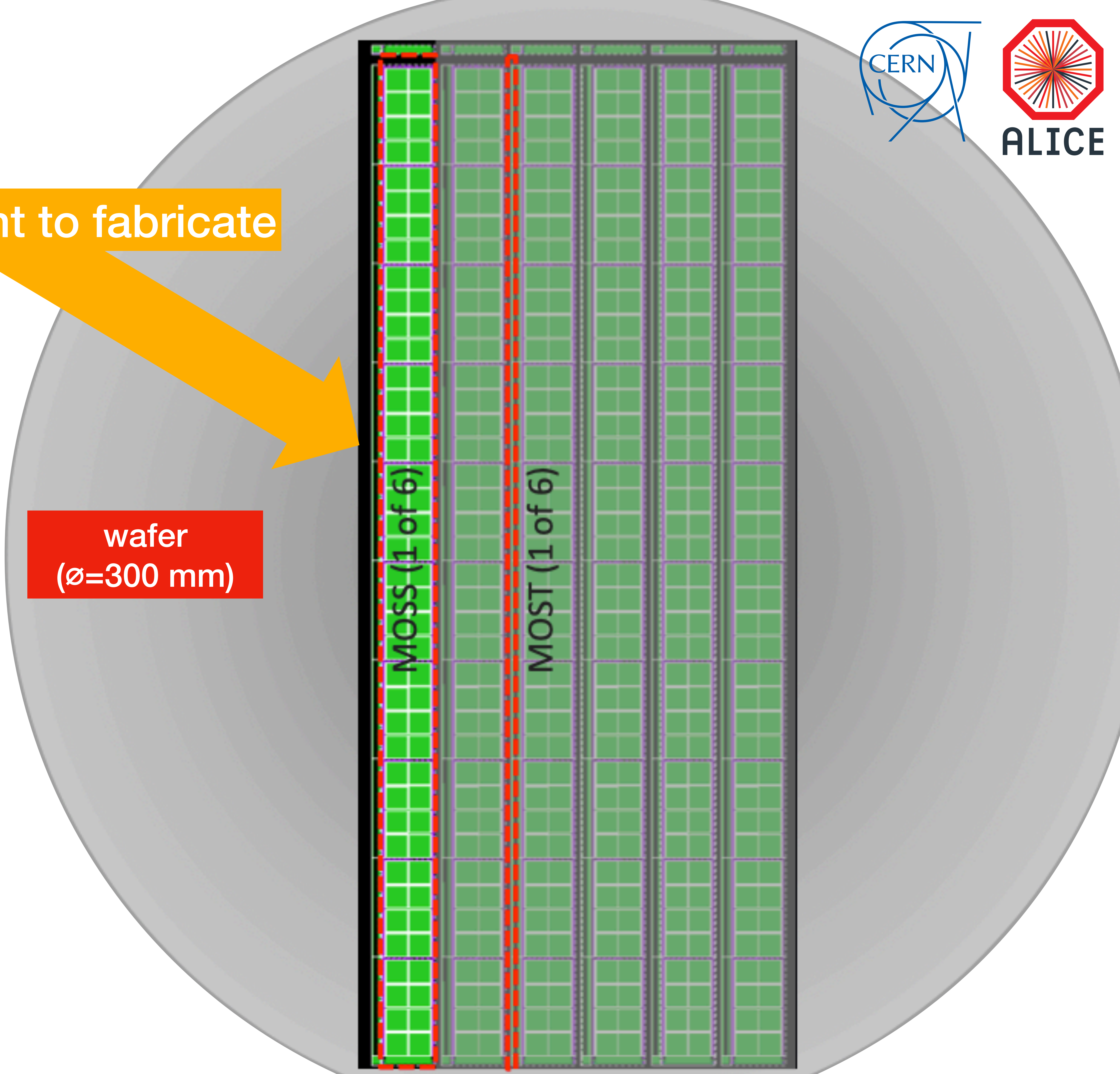
Stitching

simplified principle

what we "design"



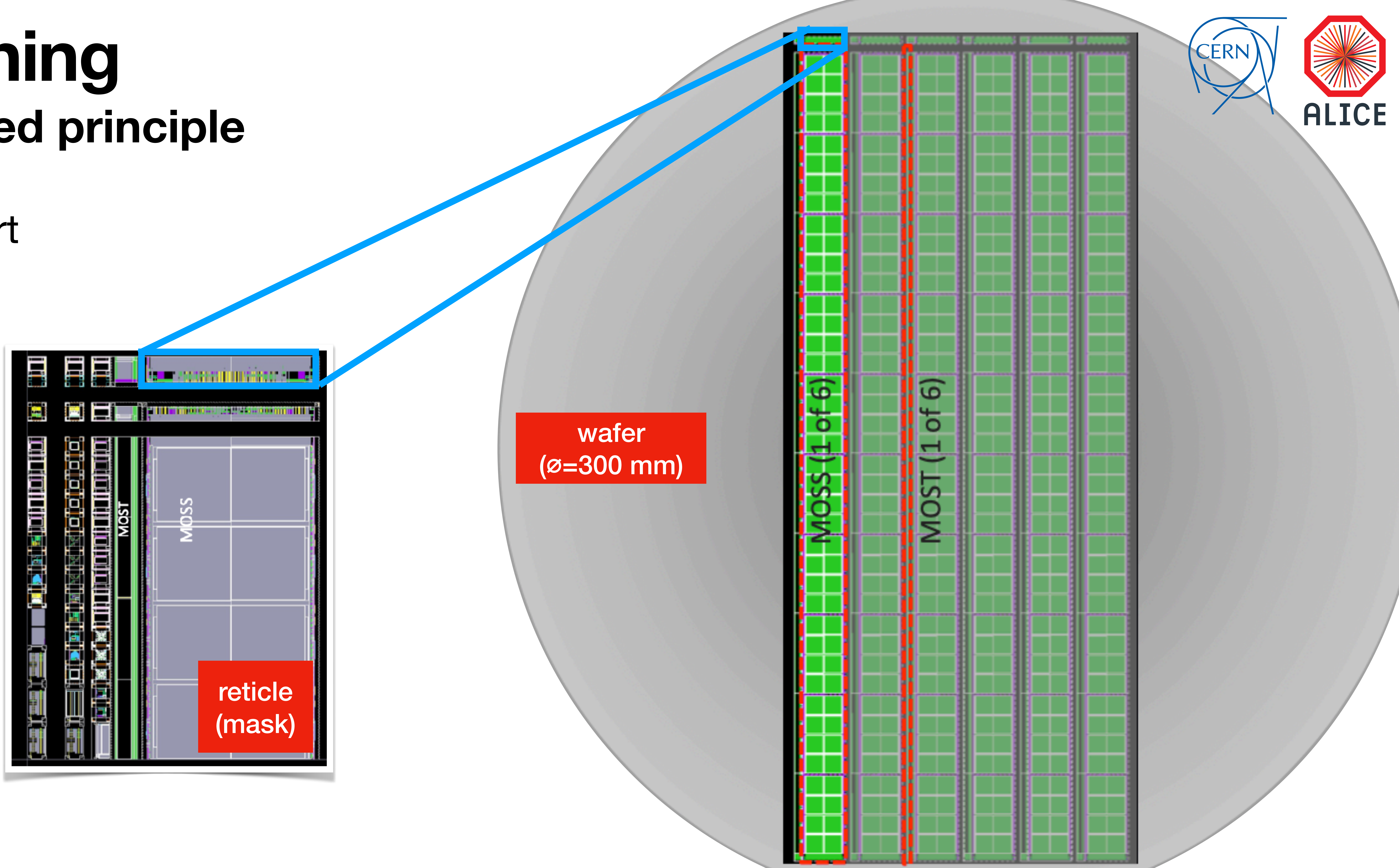
what we want to fabricate



Stitching

simplified principle

- top part



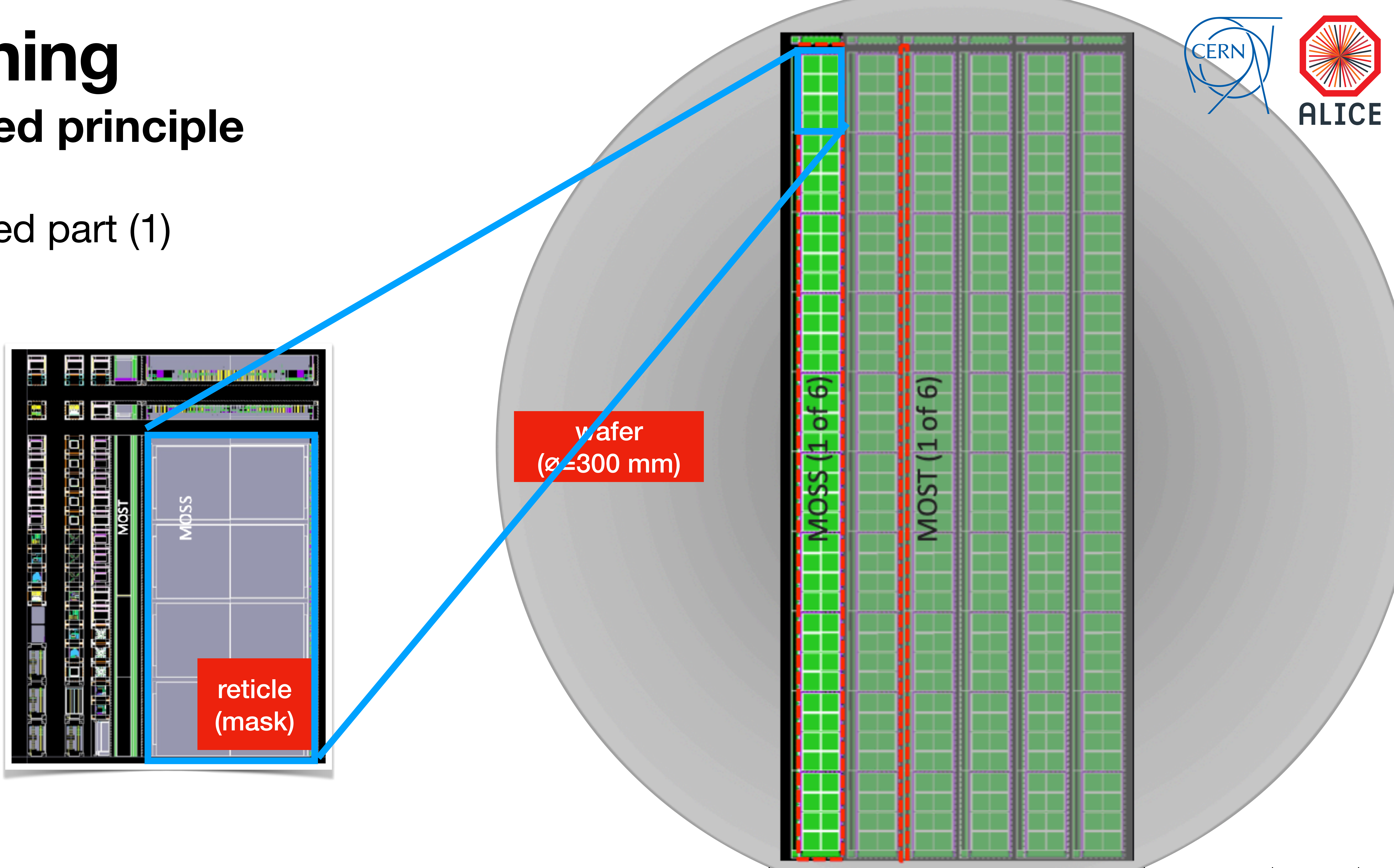
reticle (mask)

wafer (ø=300 mm)

Stitching

simplified principle

- repeated part (1)



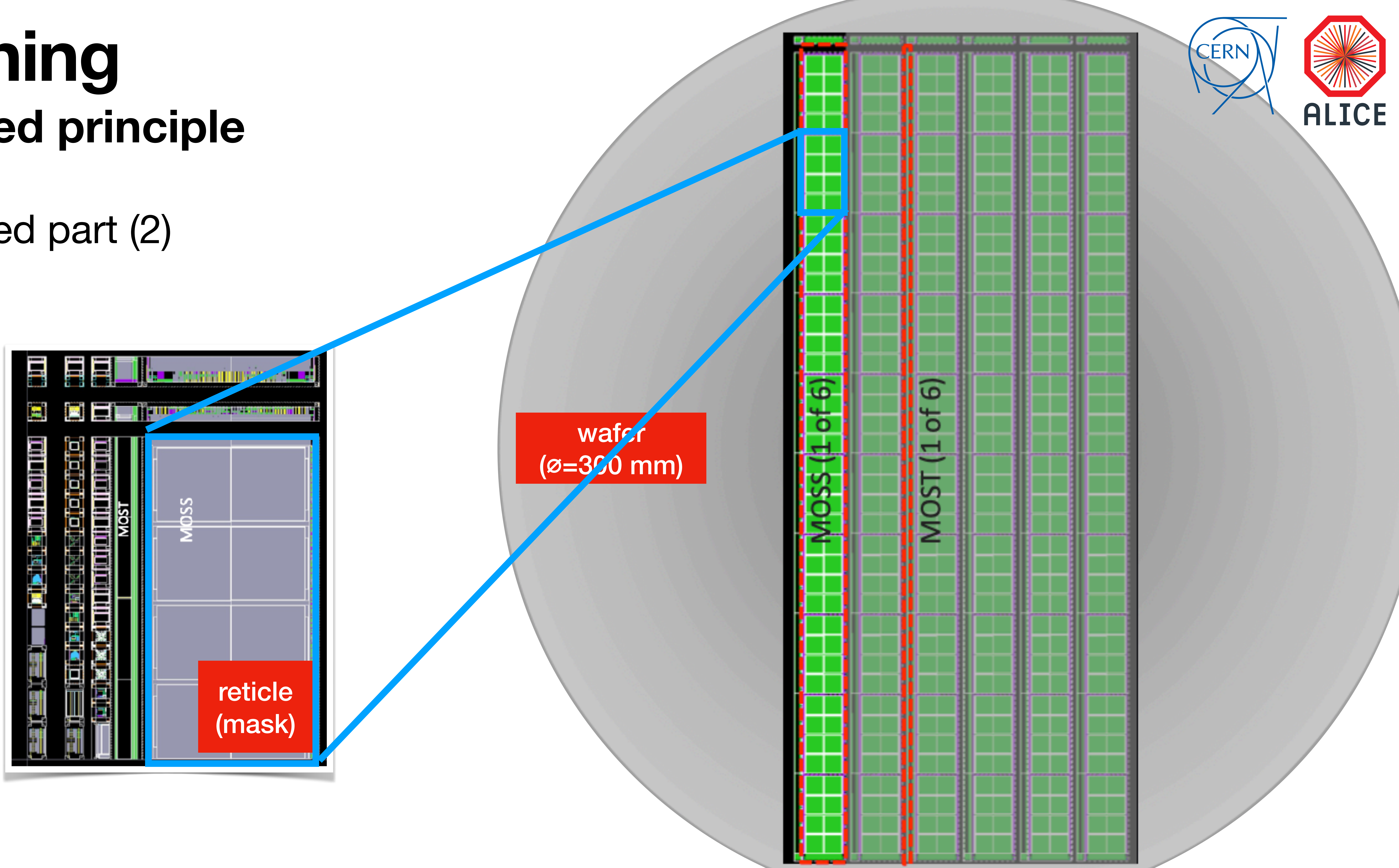
reticle
(mask)

wafer
(⌀=300 mm)

Stitching

simplified principle

- repeated part (2)



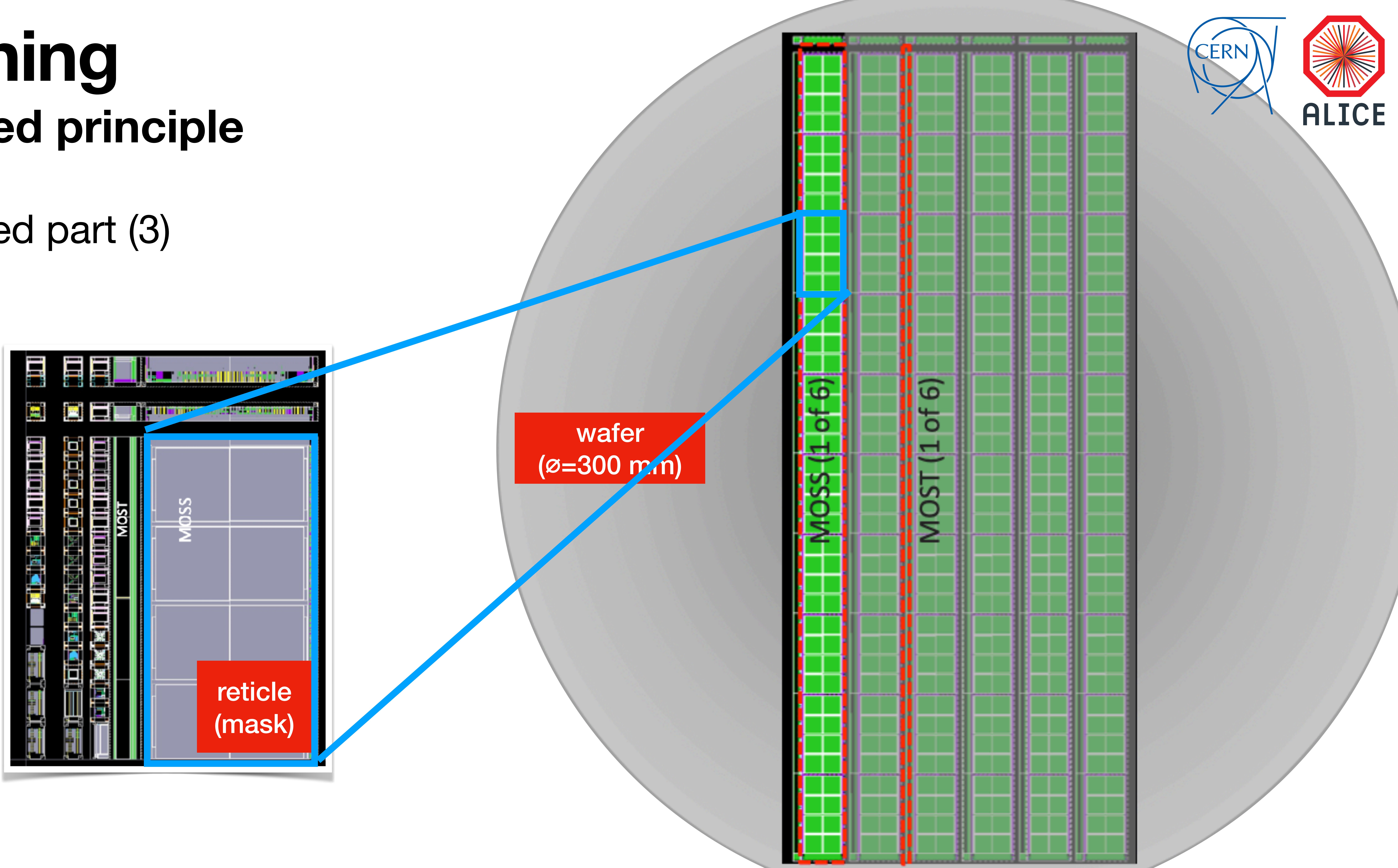
reticle
(mask)

wafer
(ø=300 mm)

Stitching

simplified principle

- repeated part (3)



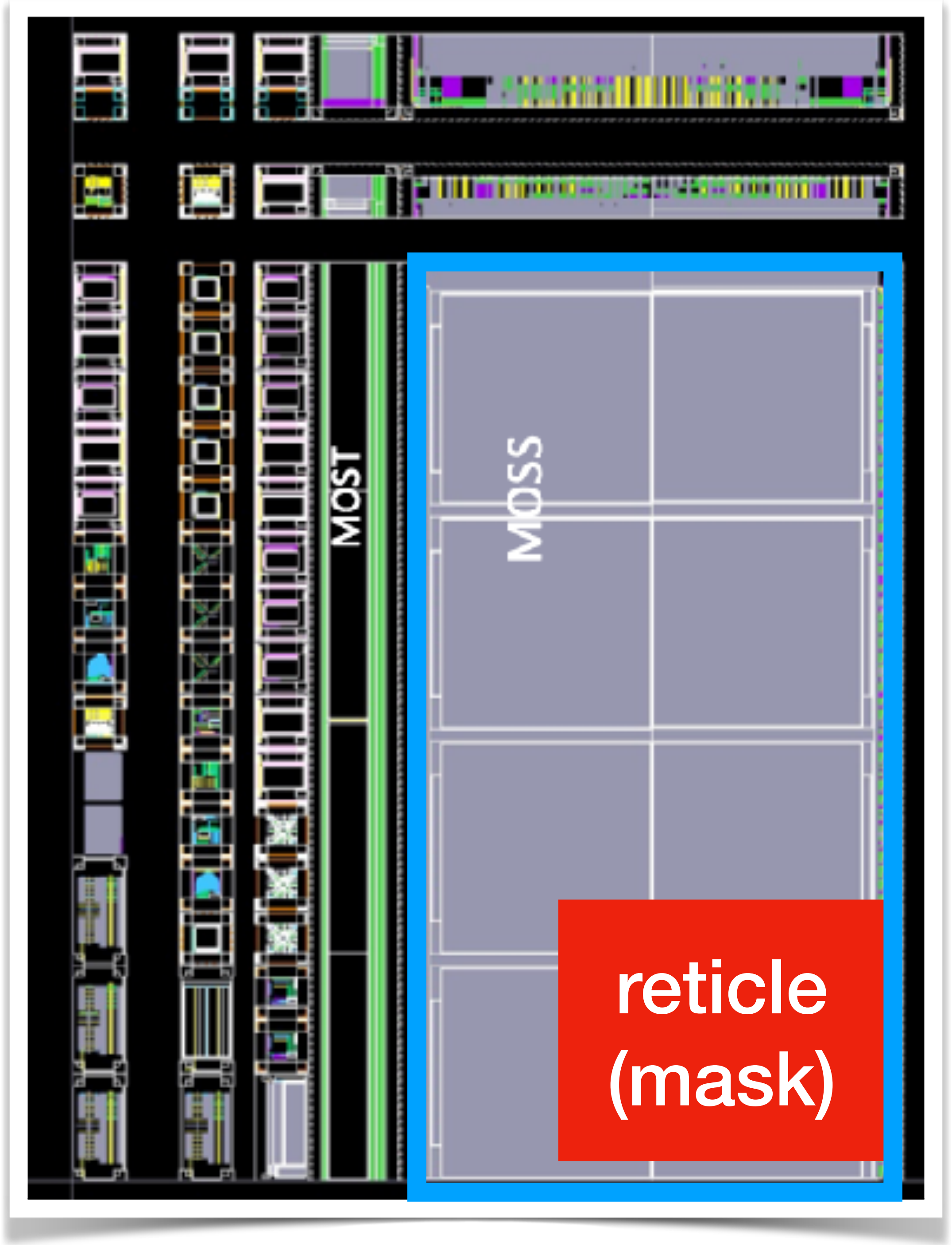
wafer
(ø=300 mm)

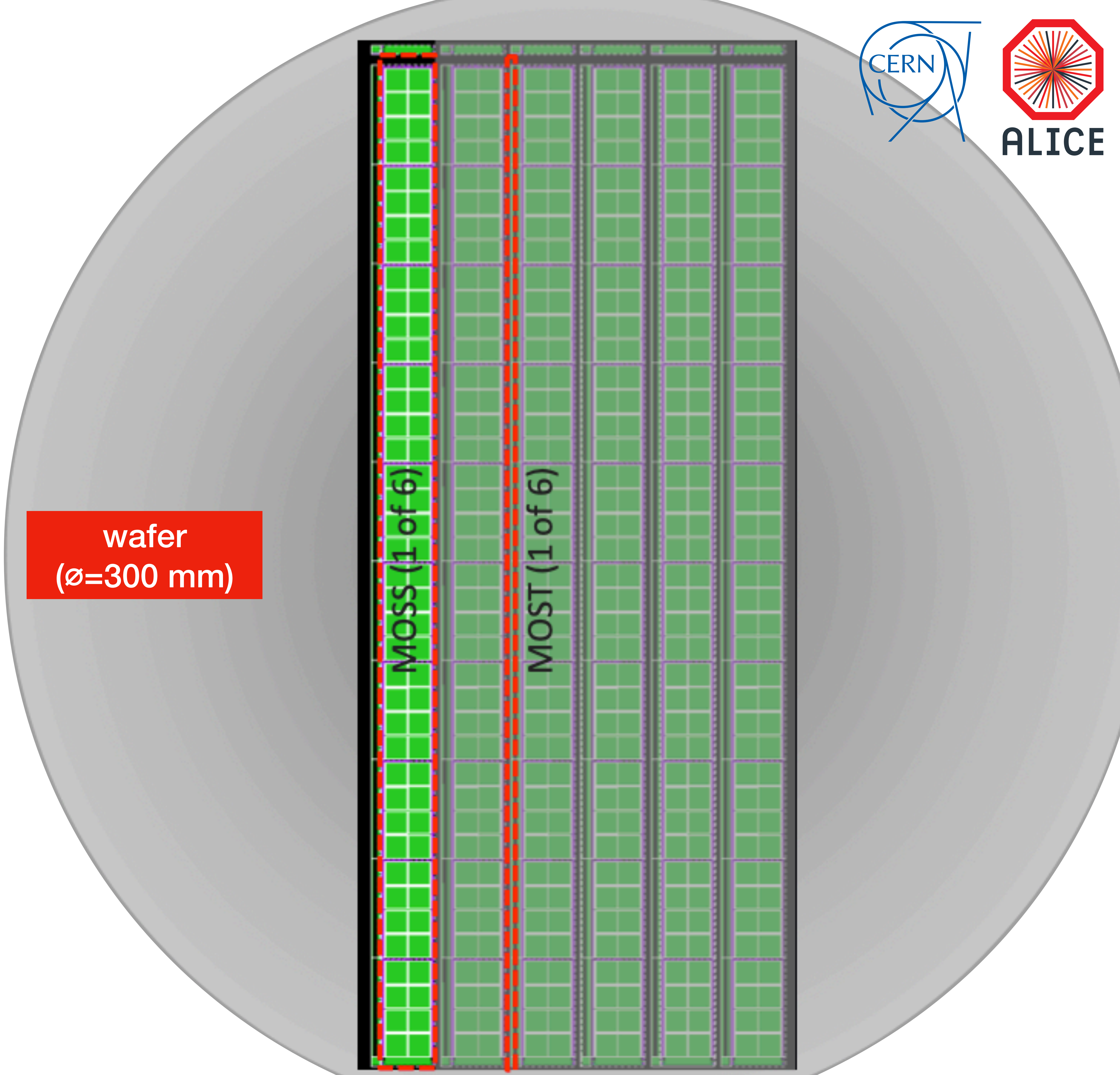
reticle
(mask)

Stitching

simplified principle

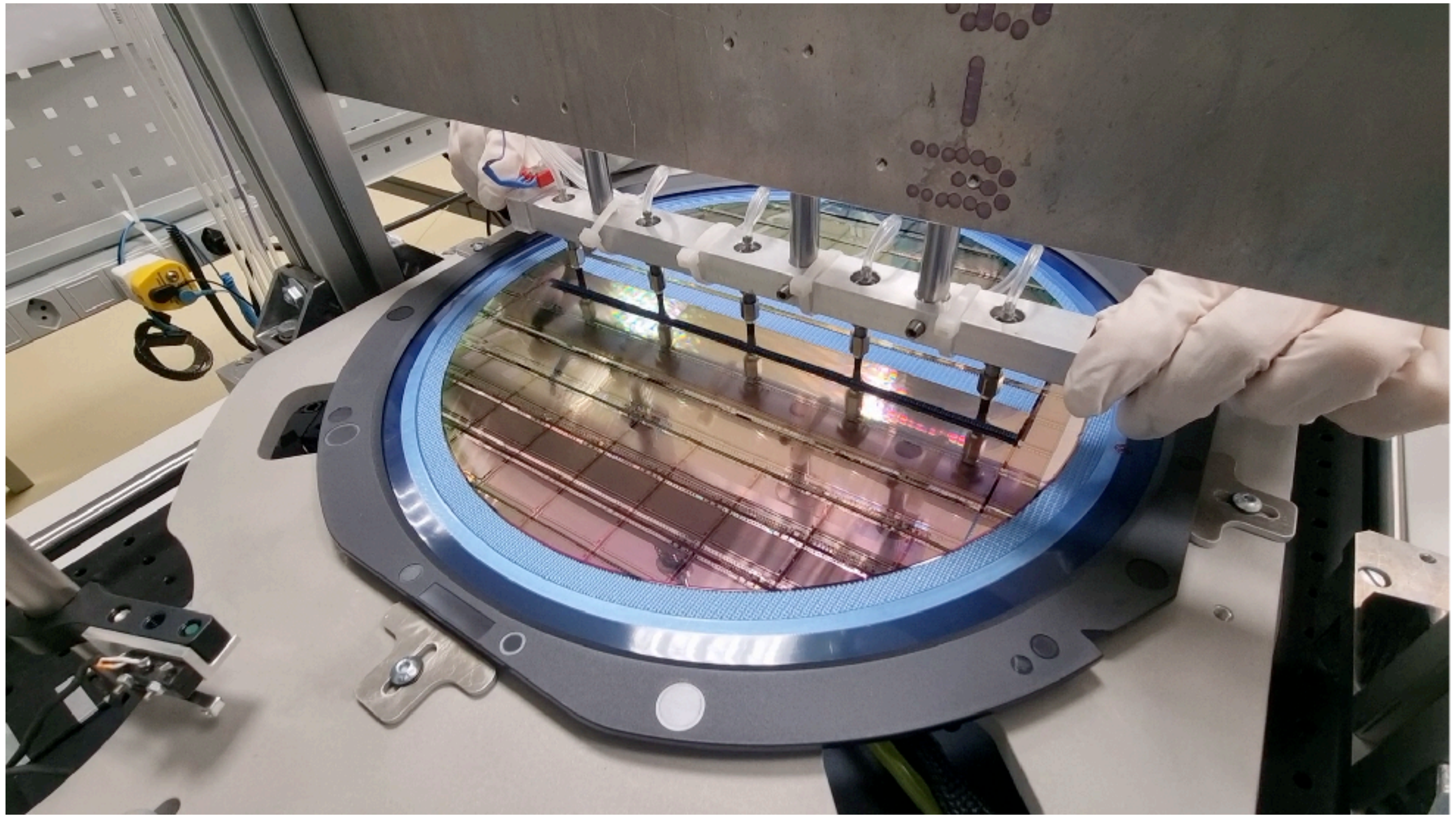
- final circuit is a concatenation of different parts of the masks

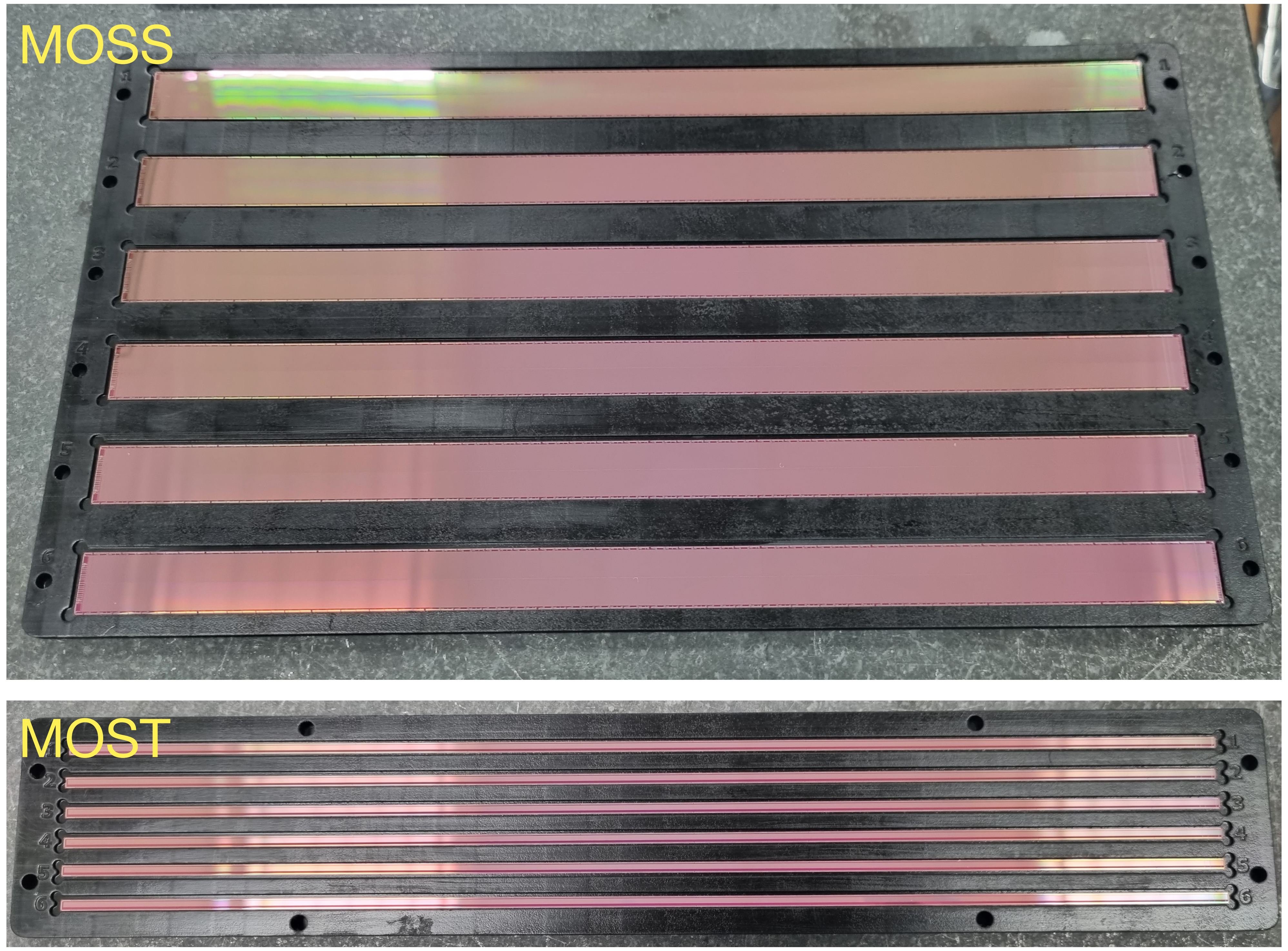




Thinning/Dicing/Picking

- Two pad wafers were thinned and diced (50 µm)
- Chips were picked using dedicated tooling
- Works! — processed wafers underway





ER1

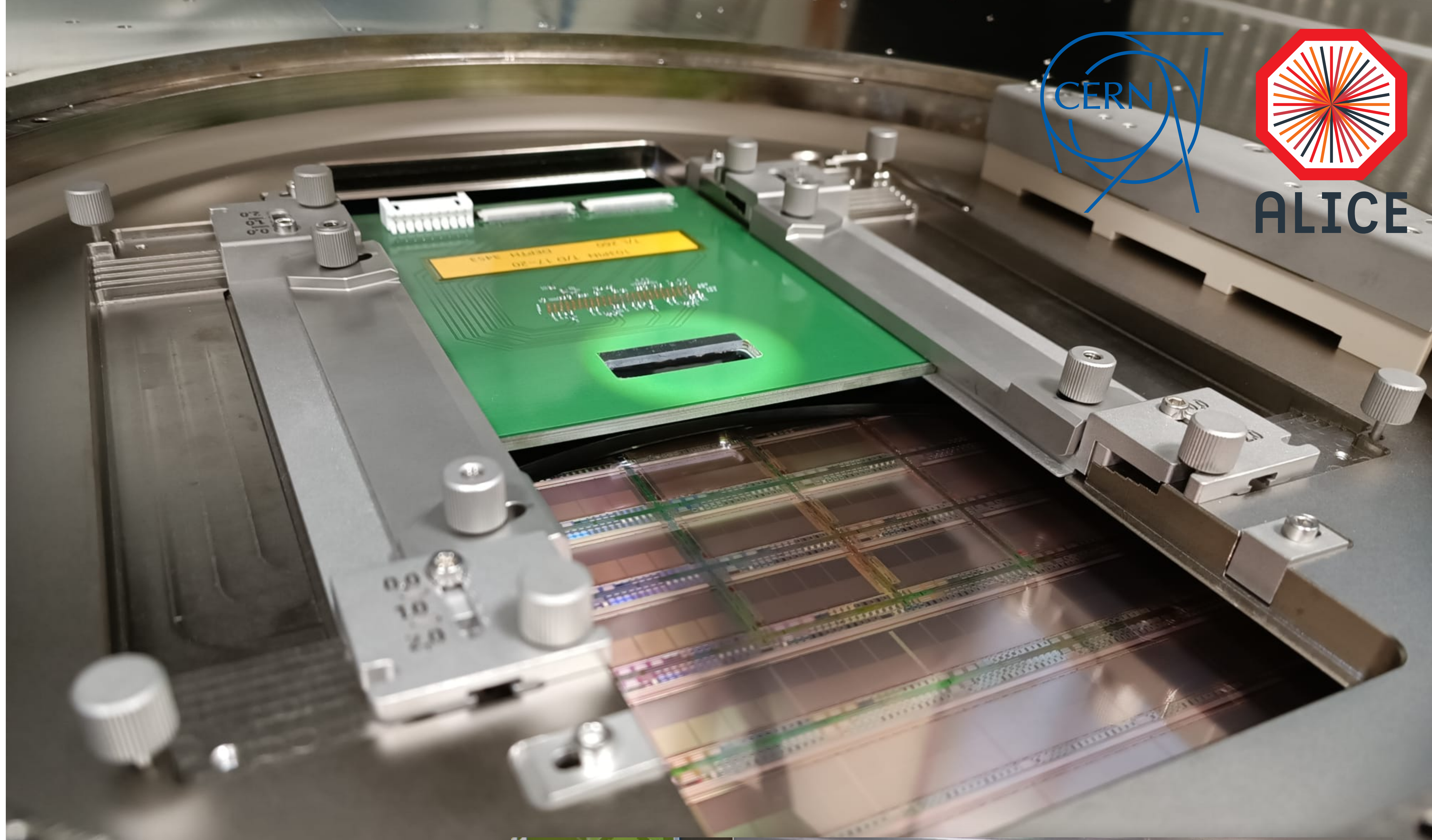
bonding (MOSS)

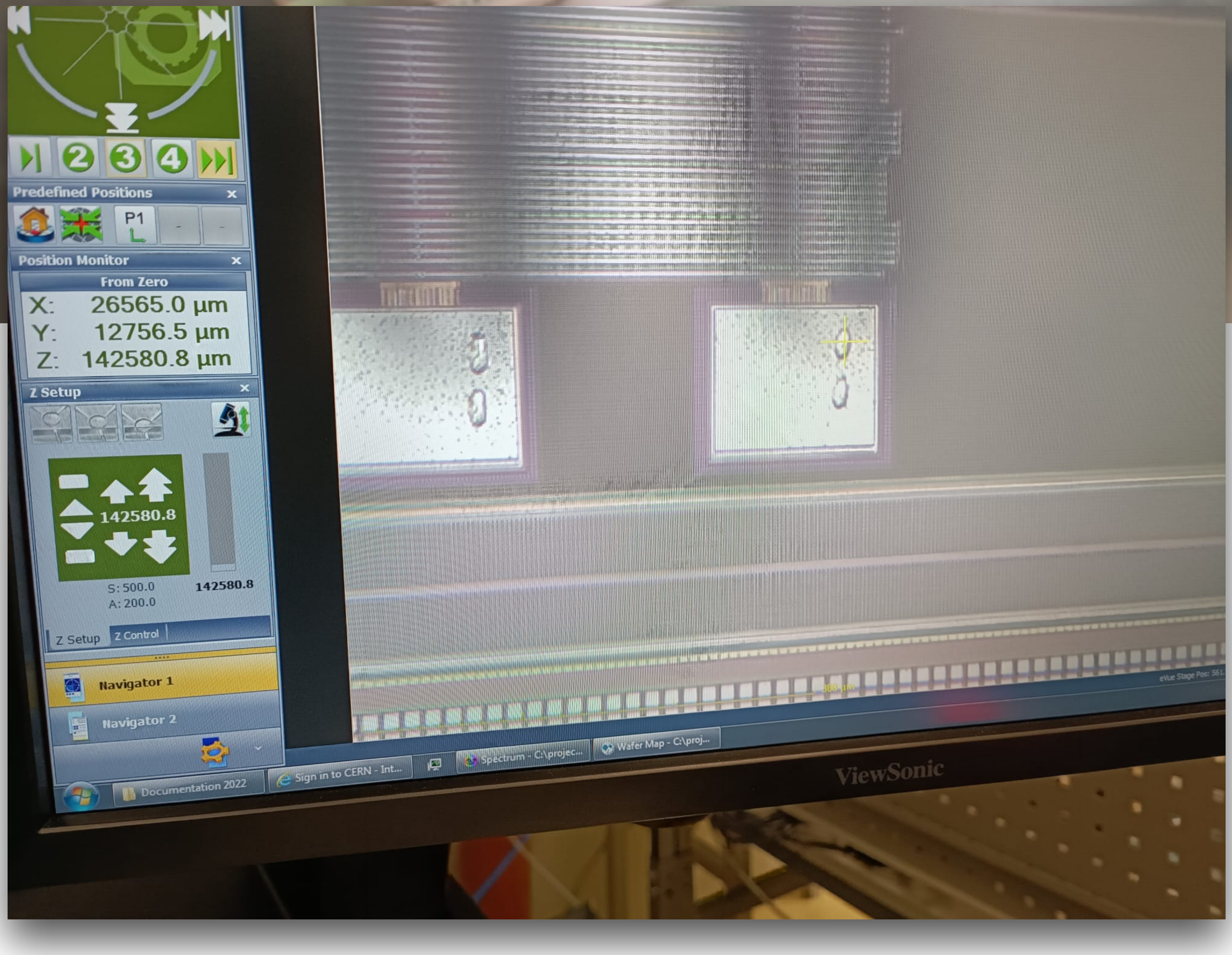
- successfully exercised with pad chips

ER1

wafer probe testing (MOSS)

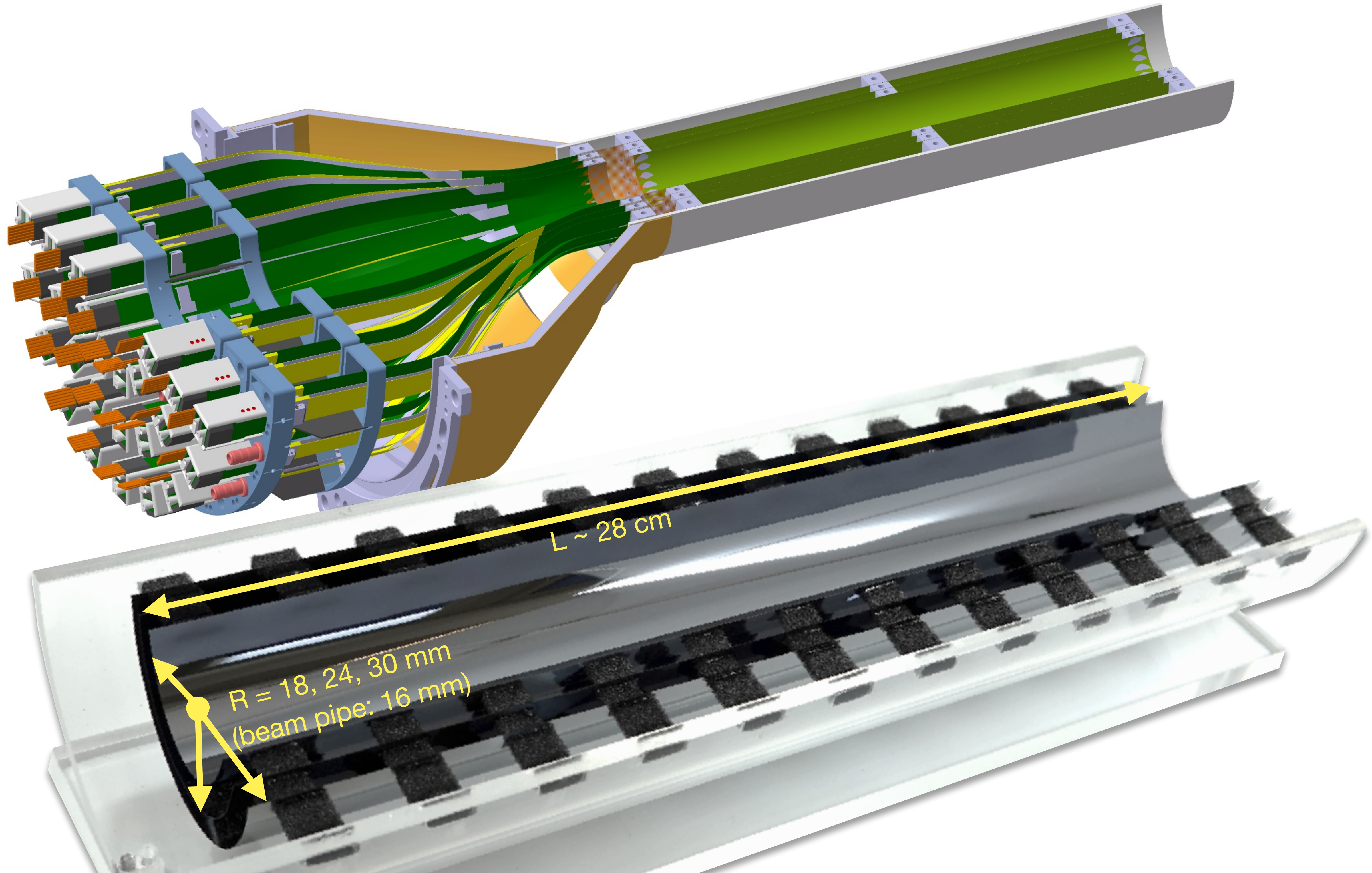
- Dedicated needle card for MOSS ready
- Tests are starting on fully processed wafers
  - chip is **alive!** (powering, slow control, digital pulsing)
- Stay tuned for much more!



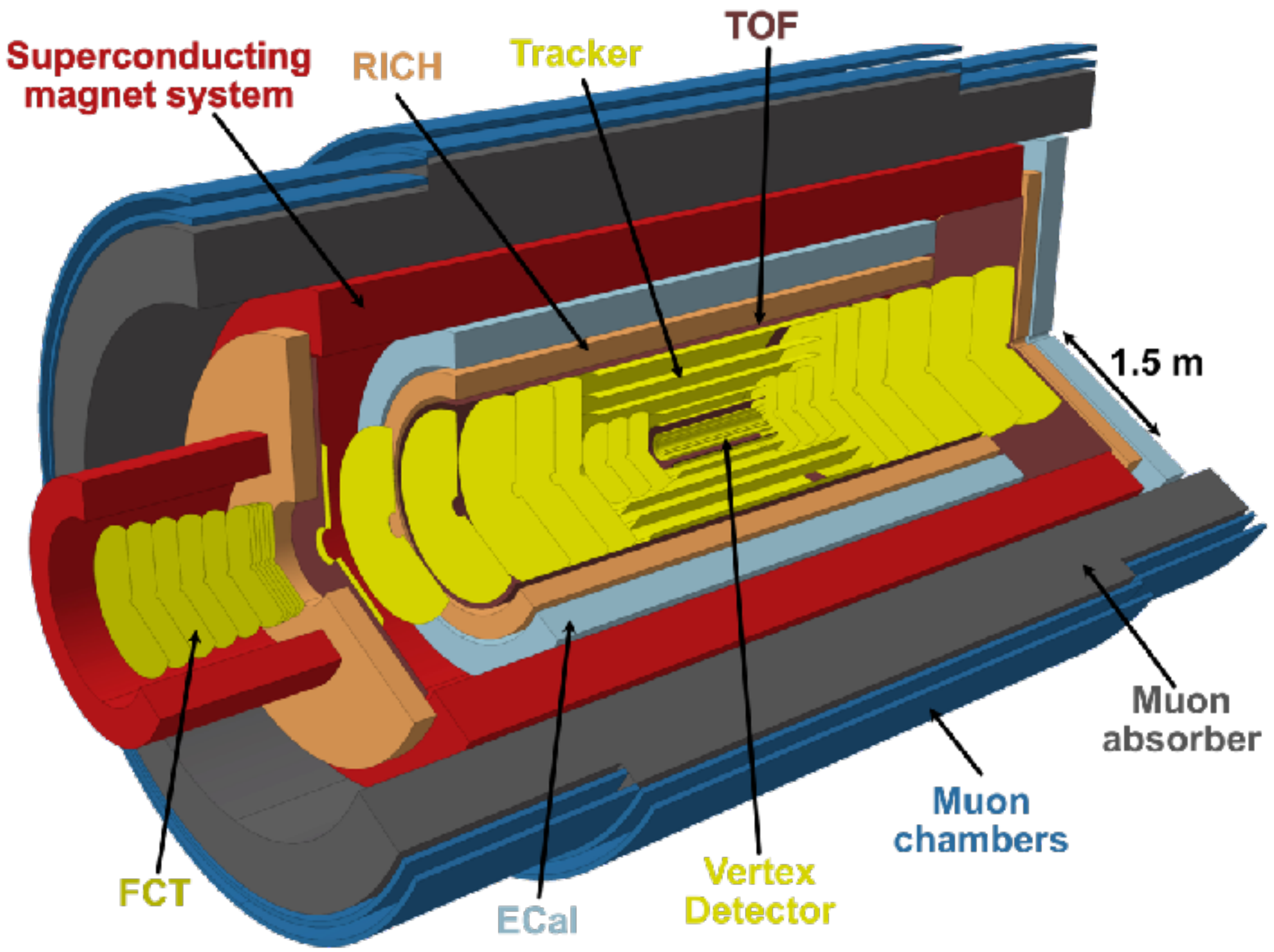

Position Monitor
From Zero
X: 26565.0 µm
Y: 12756.5 µm
Z: 142580.8 µm

Future applications in ALICE

ITS3: wafer-scale, bent MAPS

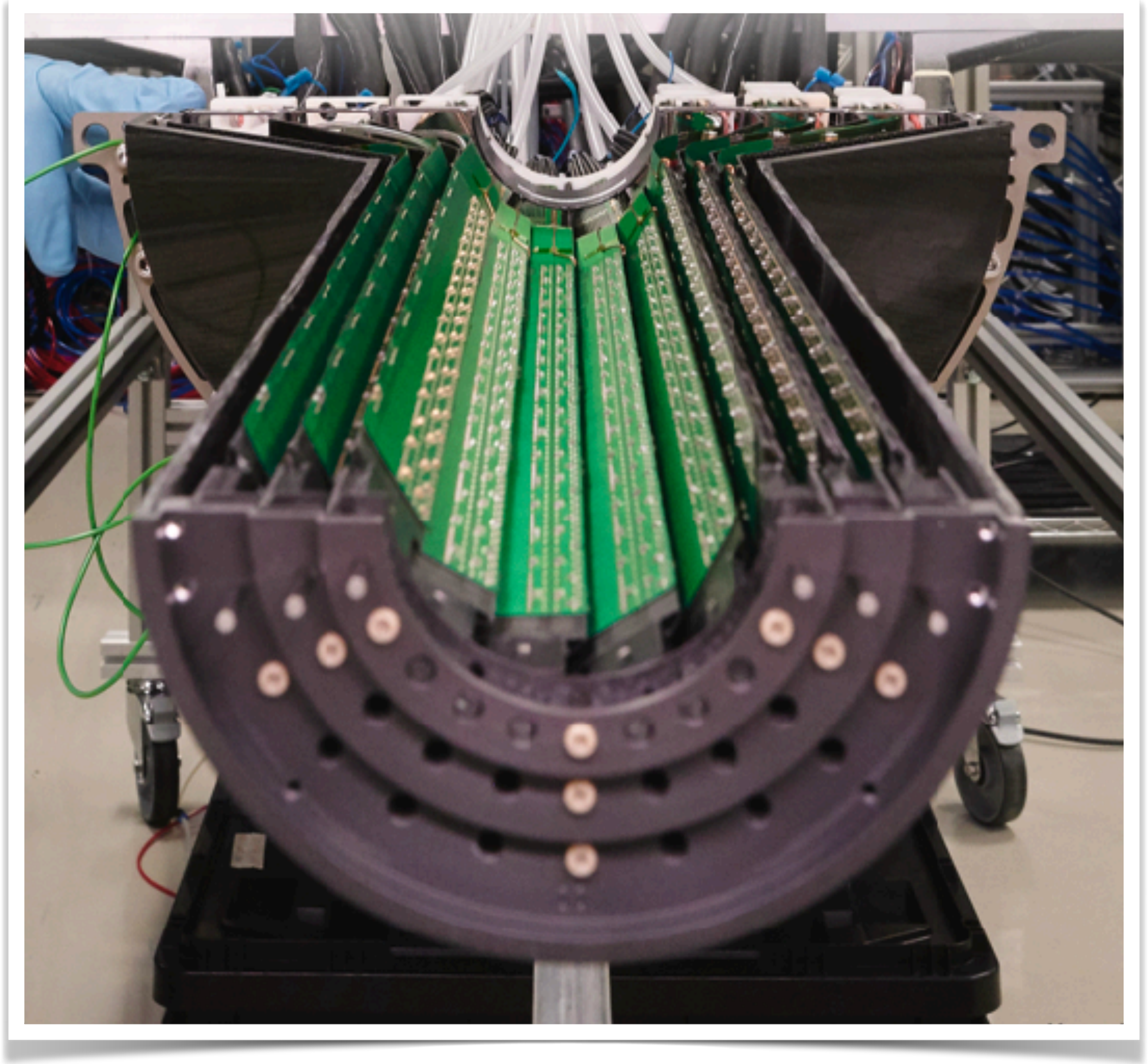


ALICE 3: based on a 60 m² silicon tracker



ALICE ITS3

LHC LS3 upgrade (installation 2027/28)



[ITS3 “engineering model 1” made of 3 layers of dummy silicon, 40-50 µm thick]

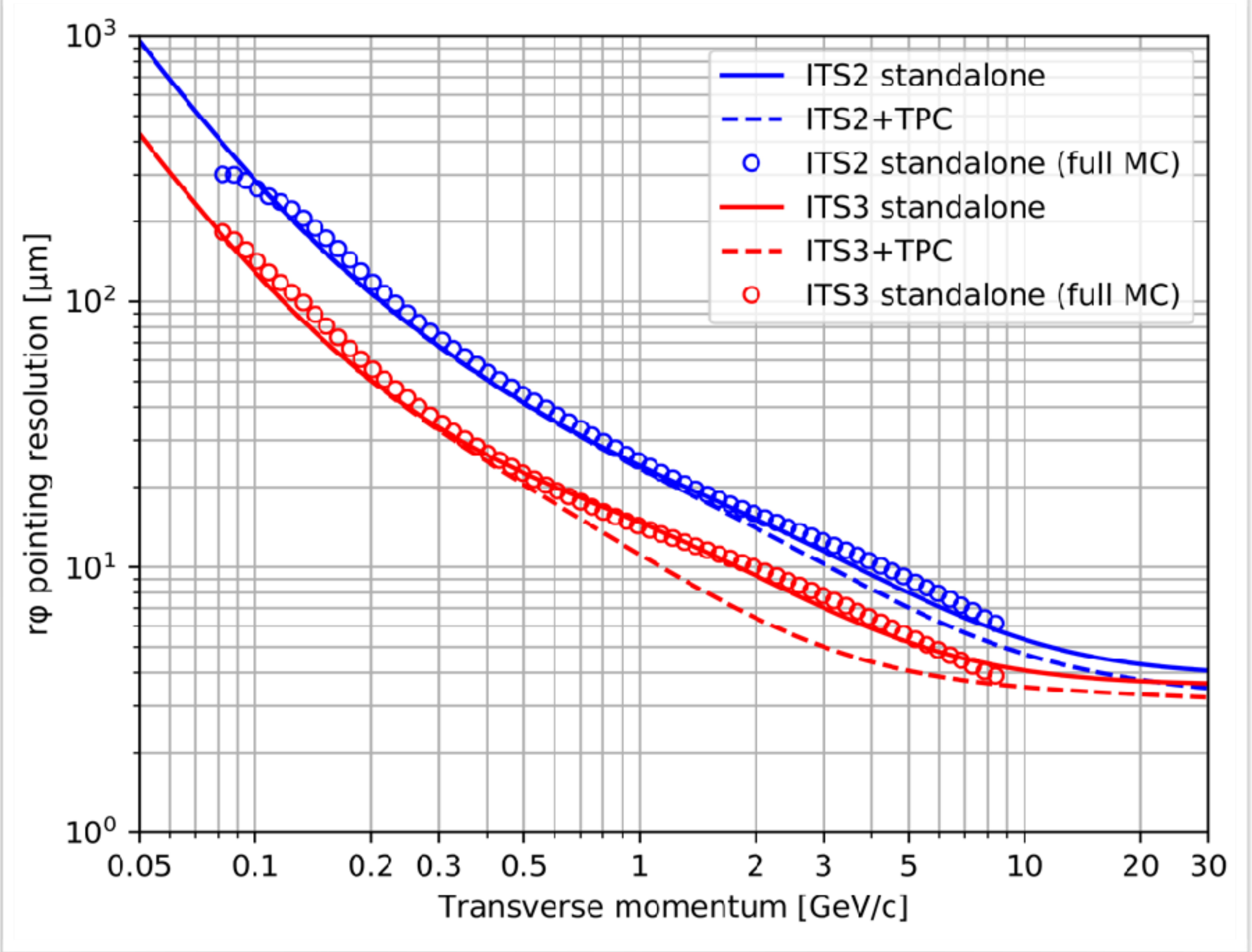
Only 1/7th of the material budget!

- Replacing the barrels by real half-cylinders (of **bent, thin** silicon)
- Rely on **wafer-scale sensors** (1 sensor per half-layer) in **65 nm** technology
- Minimised material budget and distance to interaction point
  → large improvement of vertexing precision and physics yield (“**ideal detector**”)

ALICE ITS3

Performance improvement

pointing resolution



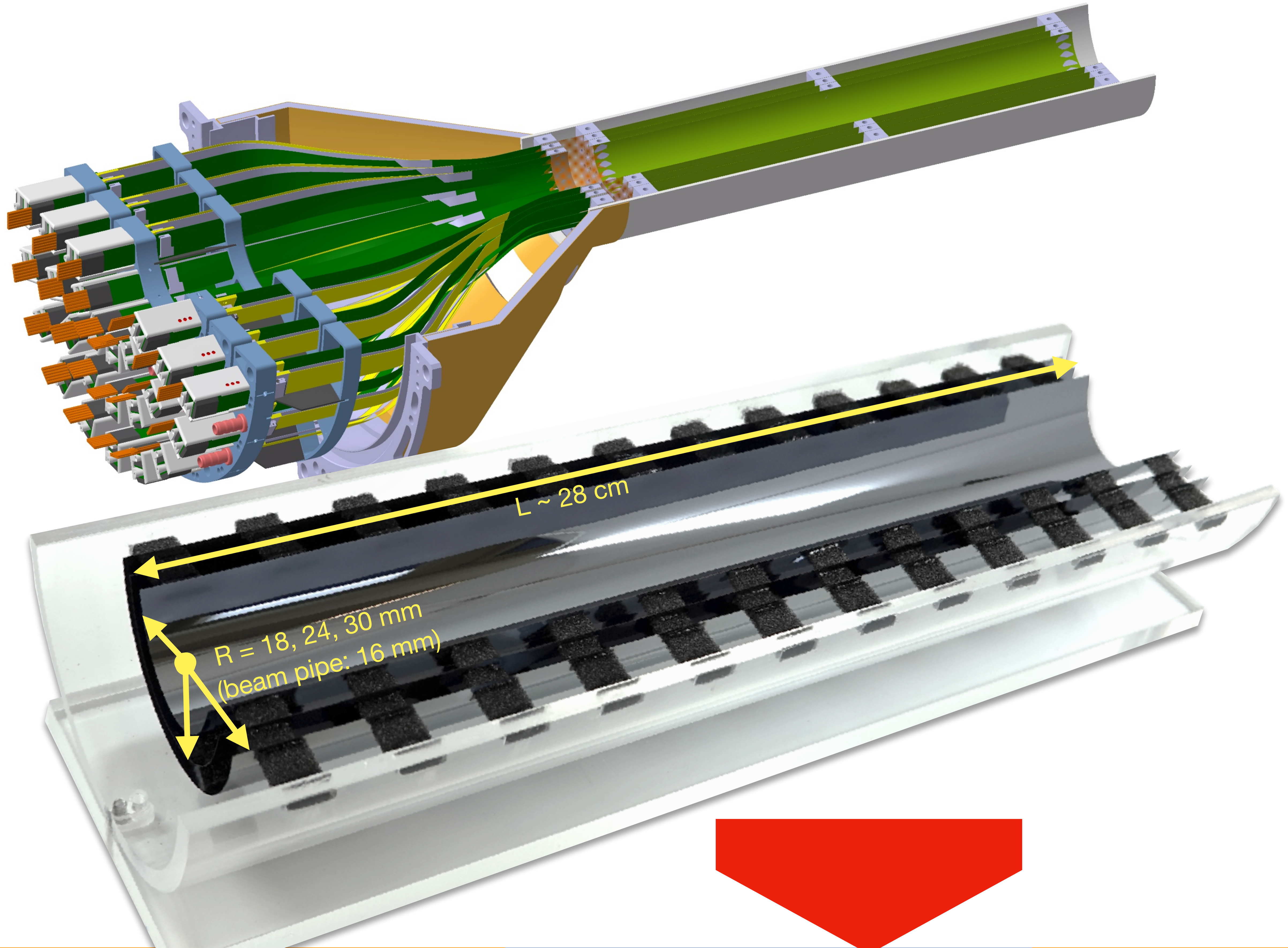
[ALICE-PUBLIC-2018-013]

improvement of factor 2 over all momenta

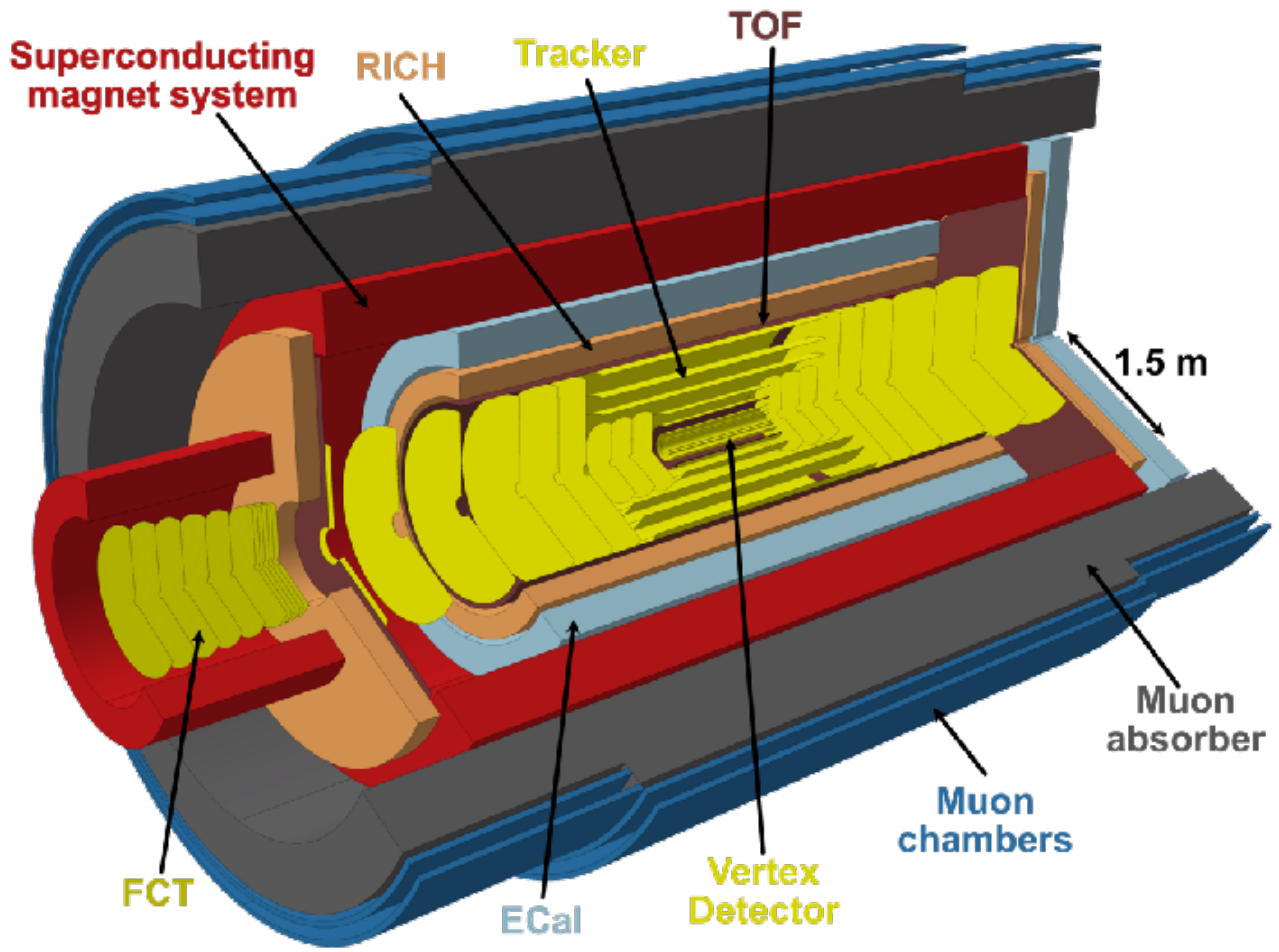
- Improvement of pointing resolution by:
  - drastic reduction of **material budget** (0.3 → 0.05% X_0/layer)
  - being **closer** to the interaction point (24 → 18 mm)
  - thinner and smaller **beam pipe** (700 → 500 μm; 18 → 16 mm)
- Directly boosts the ALICE core physics program that is largely based on:
  - low momenta
  - secondary vertex reconstruction
- E.g. Λ_c S/B improves by factor 10, significance by factor 4

Future applications in ALICE

ITS3: wafer-scale, bent MAPS



ALICE 3: based on a 60 m^2 silicon tracker



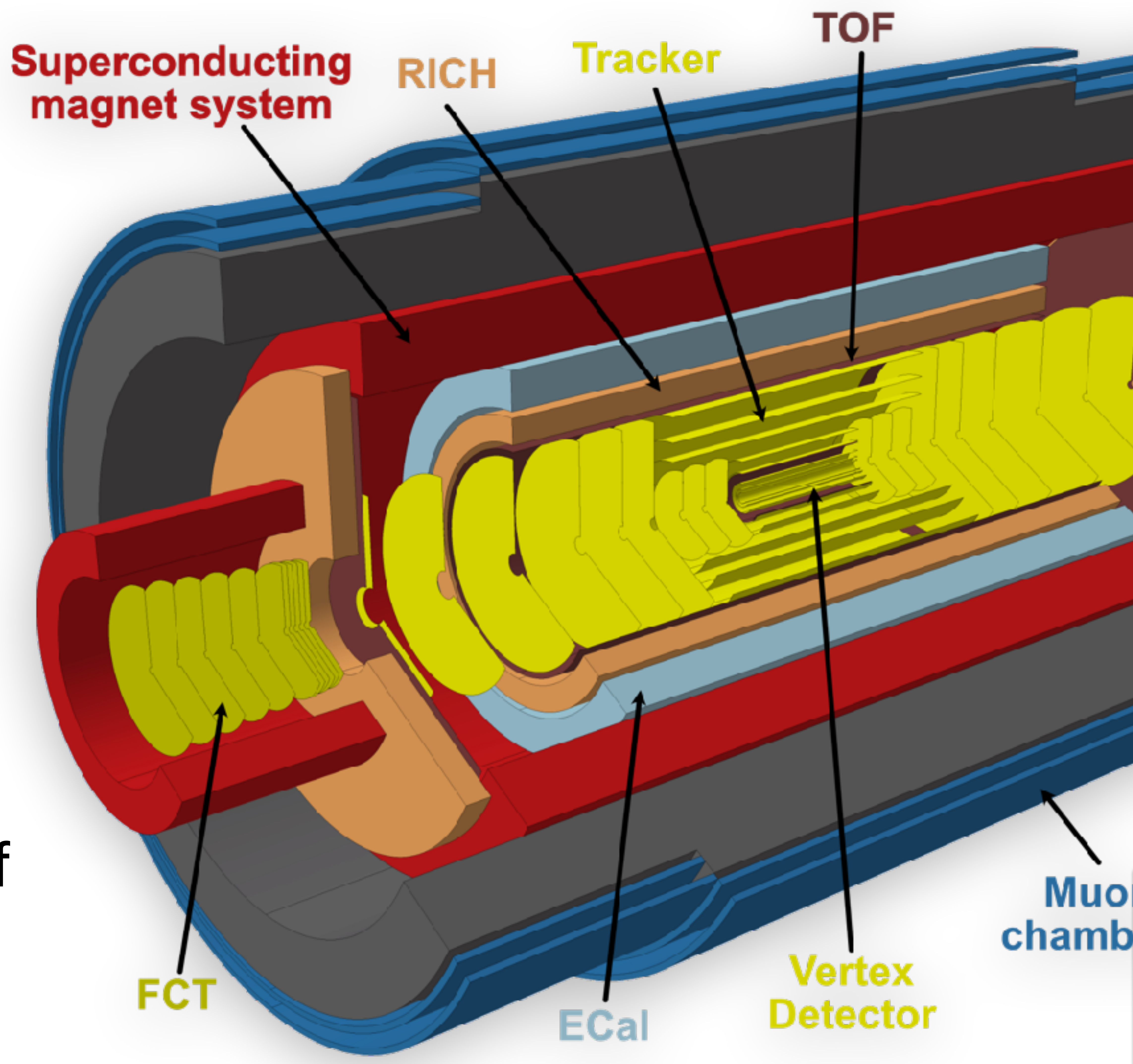
Run 3 | LS3 | Run 4 | LS4 | Run 5

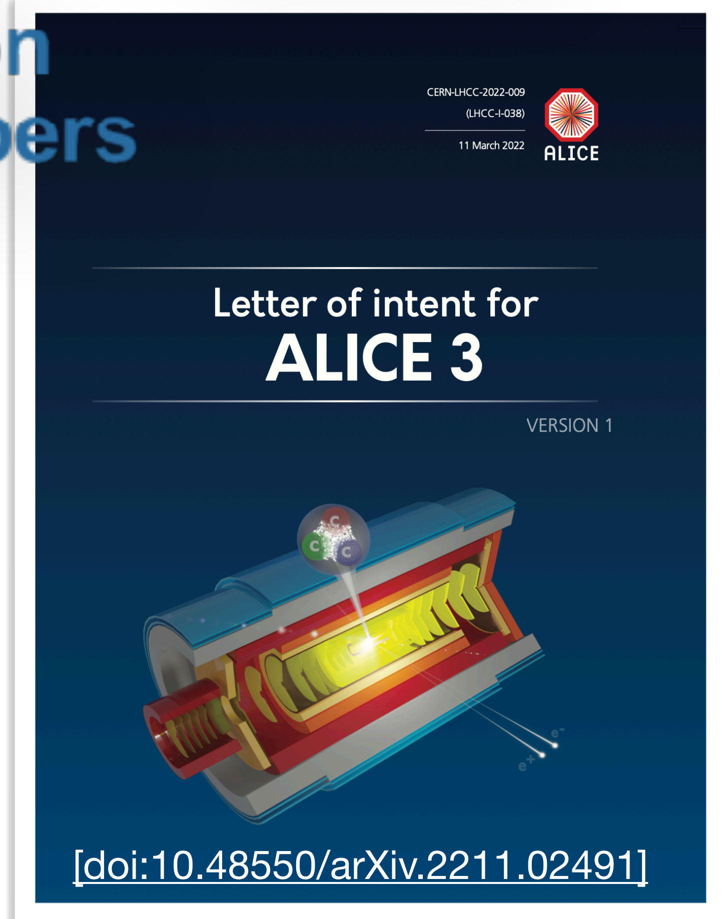
2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037

ALICE 3

LHC LS4 2033/34

- ALICE 3 is centred around a 60 m² MAPS tracker
    - innermost layers will be based on wafer-scale Silicon sensors "iris tracker", similar to ITS3 (but in vacuum)
    - outer tracker will be based on modules like ITS2 (but order of magnitude larger)
- *This is the next big and concrete step for this technology*




CERN-LHCC-2022-009
(LHCC-I-038)
11 March 2022

Letter of intent for
ALICE 3

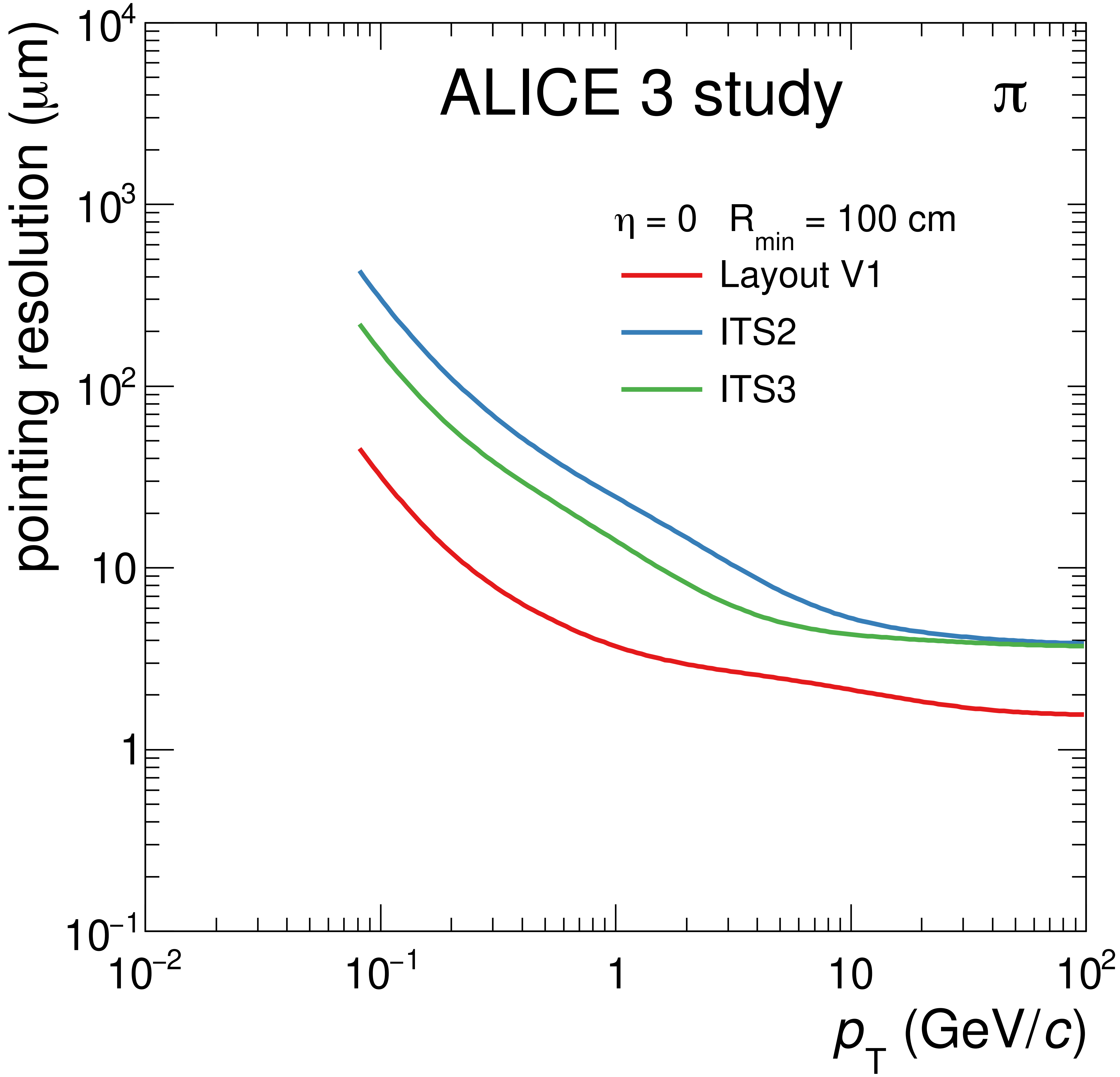
VERSION 1

[doi:10.48550/arXiv.2211.02491]

ALICE 3

pointing resolution

- ALICE 3 is centred around a 60 m² MAPS tracker
  - innermost layers will be based on wafer-scale Silicon sensors "iris tracker", similar to ITS3 (but in vacuum)
  - outer tracker will be based on modules like ITS2 (but order of magnitude larger)
- *This is the next big and concrete step for this technology*



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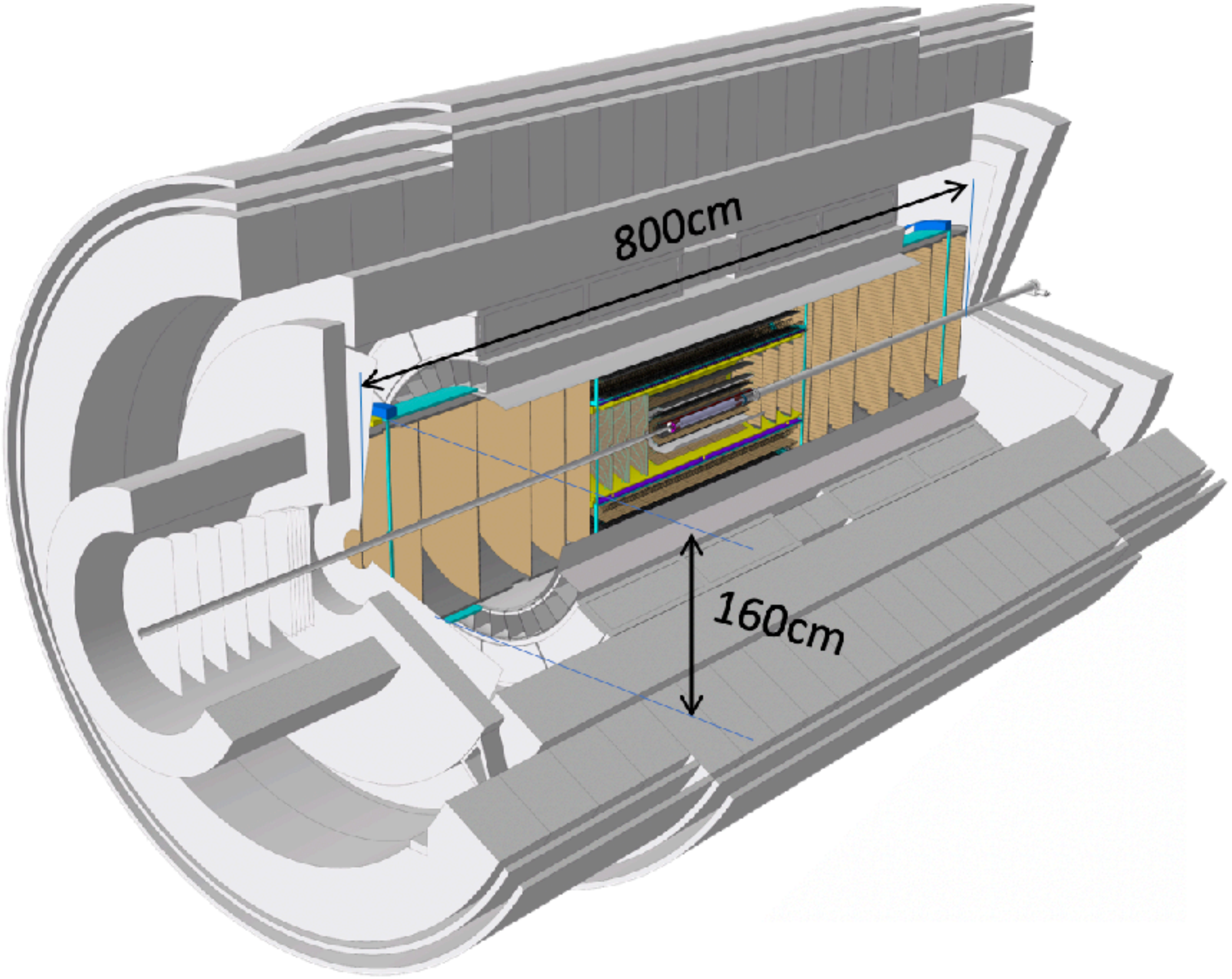
ALICE 3

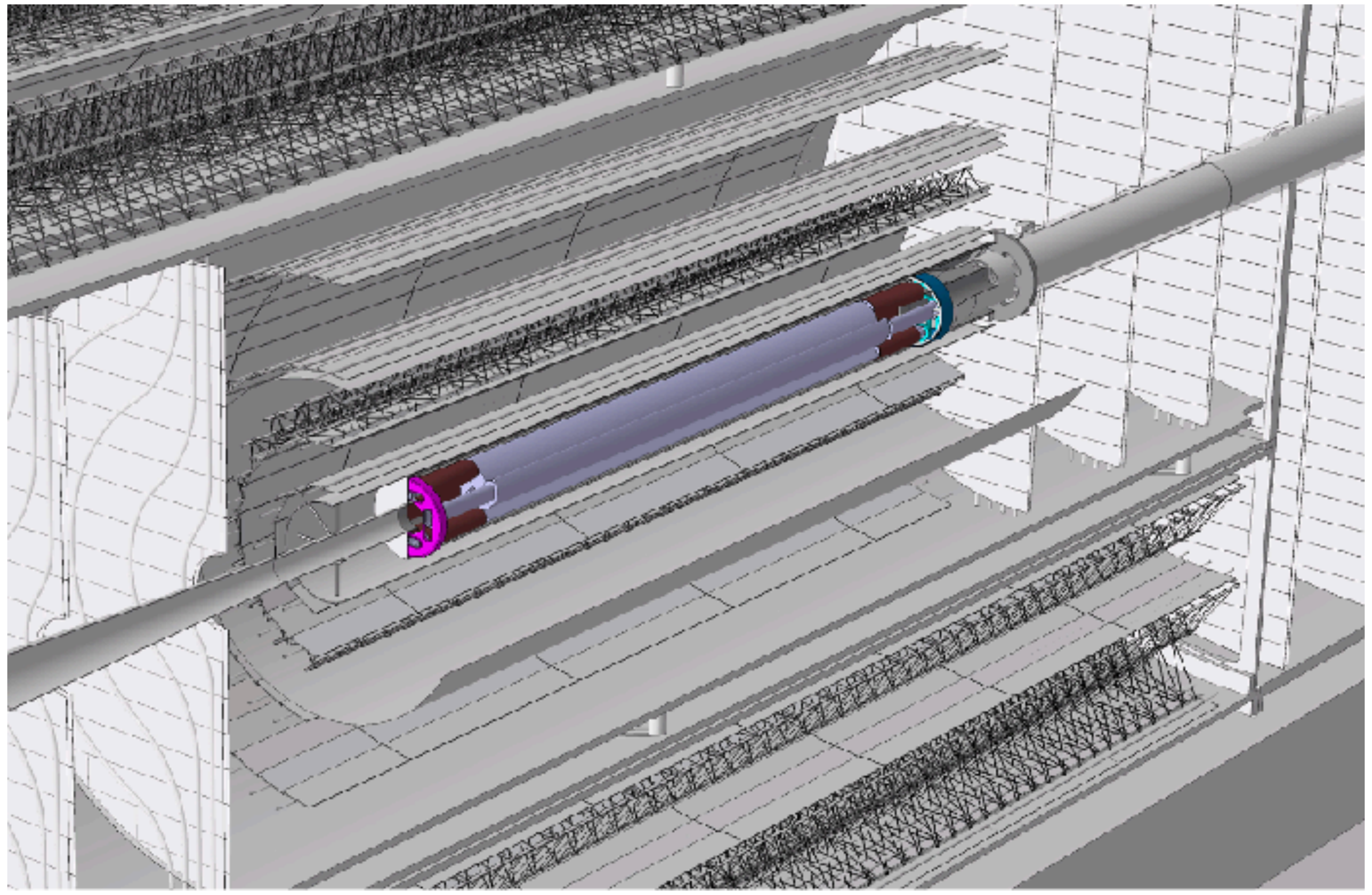
outer tracker

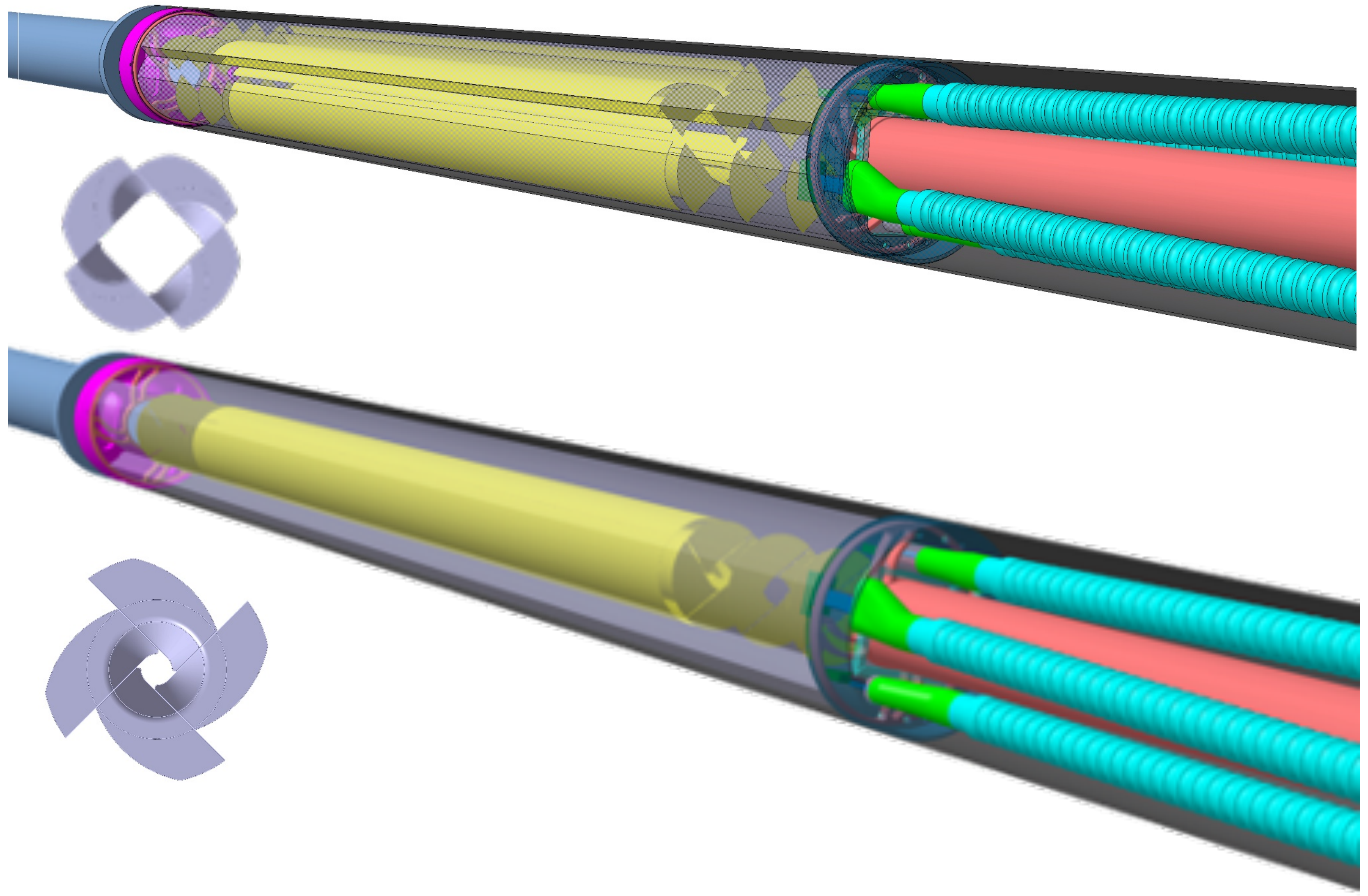


- **60 m²** silicon pixel detector
  - large coverage: ±4η
  - high-spatial resolution: ≈ 10 μm
  - very low material budget: X/X_0 (total) ≲ 10%
  - low power: ≈ 20 mW/cm²
- module (O(10 x 10 cm²)) concept based on industry-standard processes for assembly and testing

ALICE 3

vertex detector

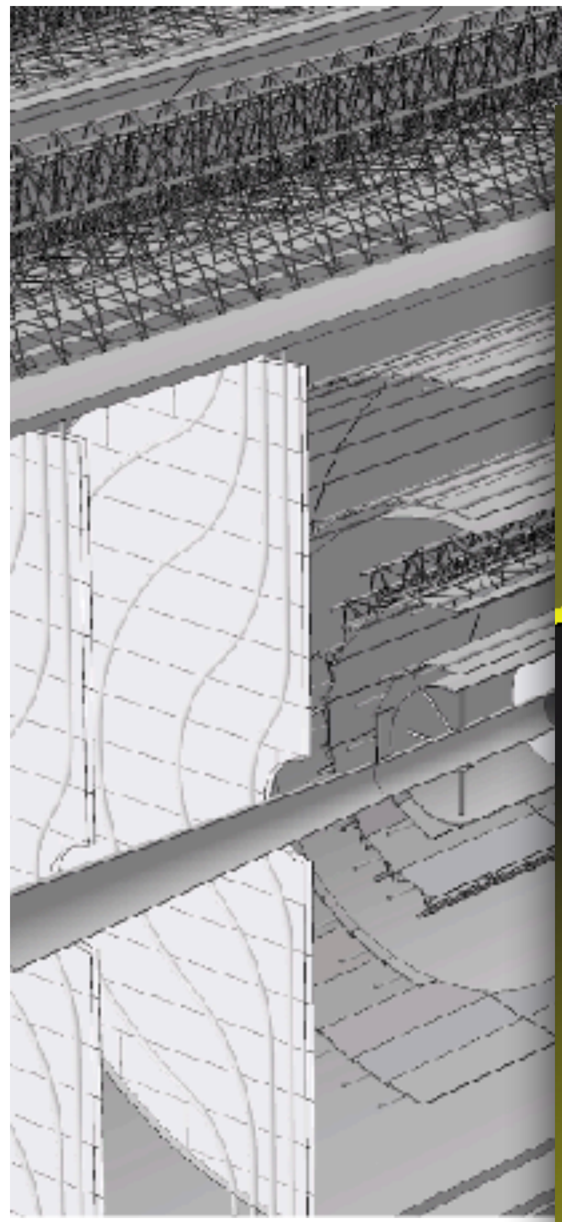


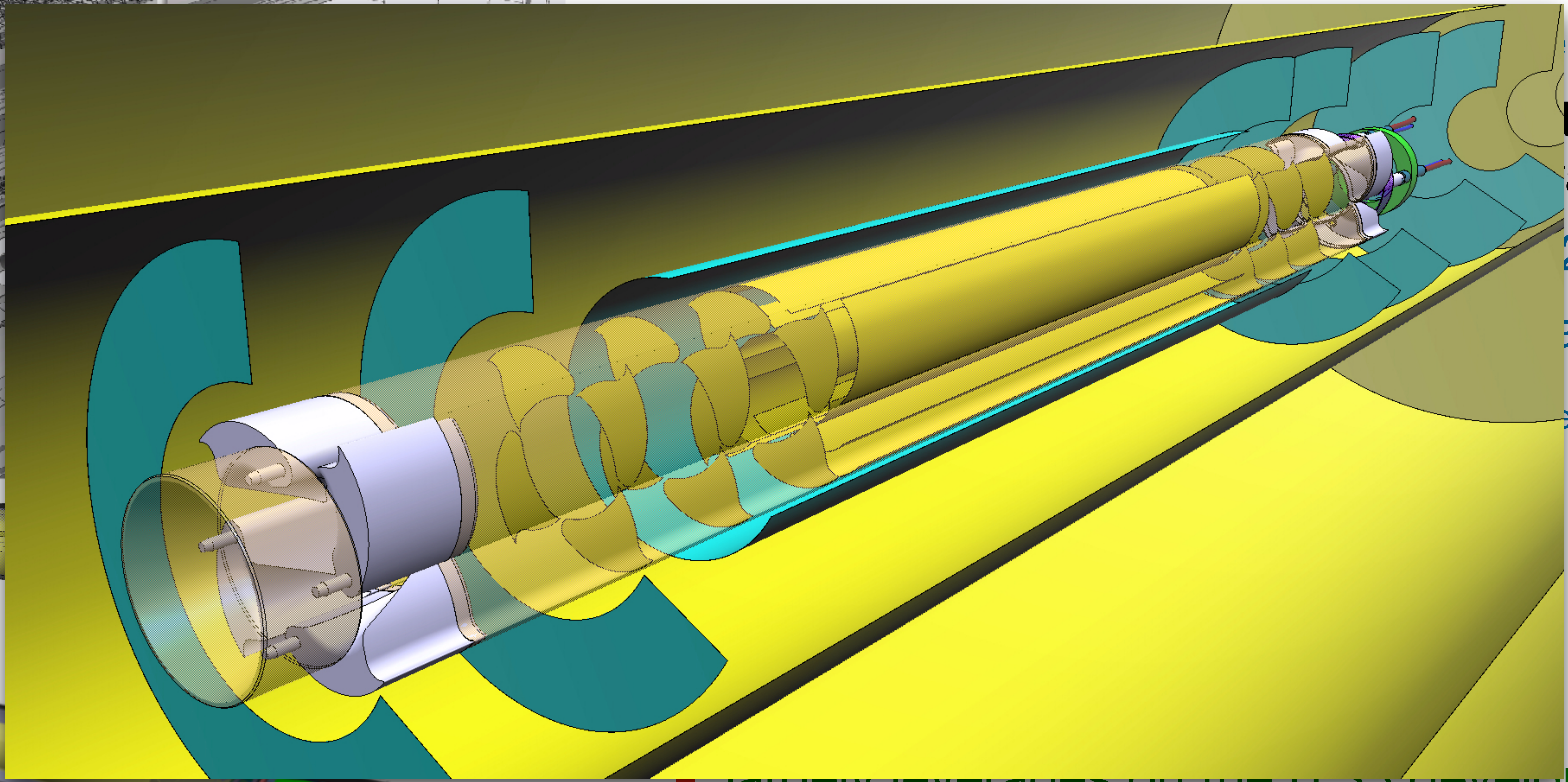


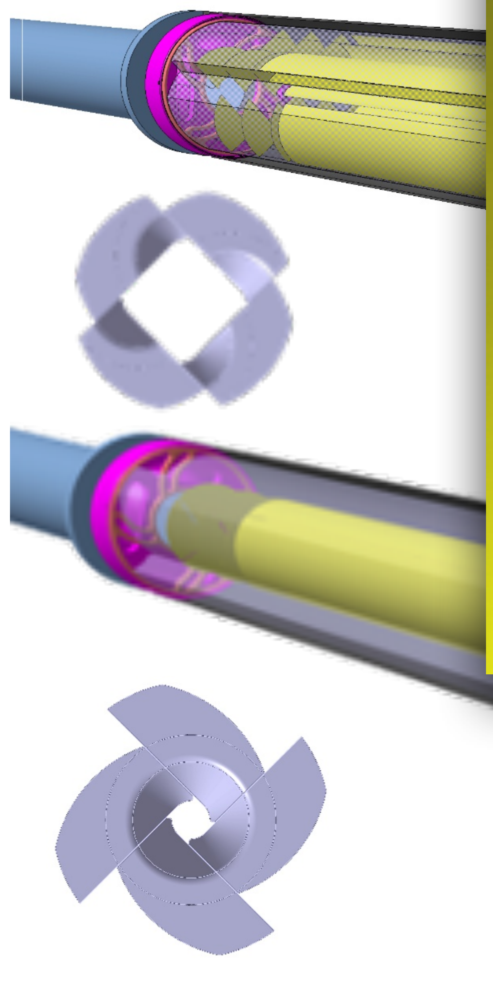
- Based on wafer-scale, ultra-thin, curved MAPS
  - radial distance from interaction point: 5 mm (inside beampipe, retractable configuration)
  - unprecedented spatial resolution: ≈ 2.5 µm
  - … and material budget: ≈ 0.1% X_0/layer
  - at radiation levels of: ≈ 10^{16} 1MeV n_{eq}/cm^2 + 300 Mrad
  - and hit rates up to: 94 MHz/cm^2
- Unprecedented performance figures
  - largely leverages on the ITS3 developments
  - pushes improvements on a number of fronts

ALICE 3

vertex detector







d MAPS

t: 5 mm

ation)

2.5 μm

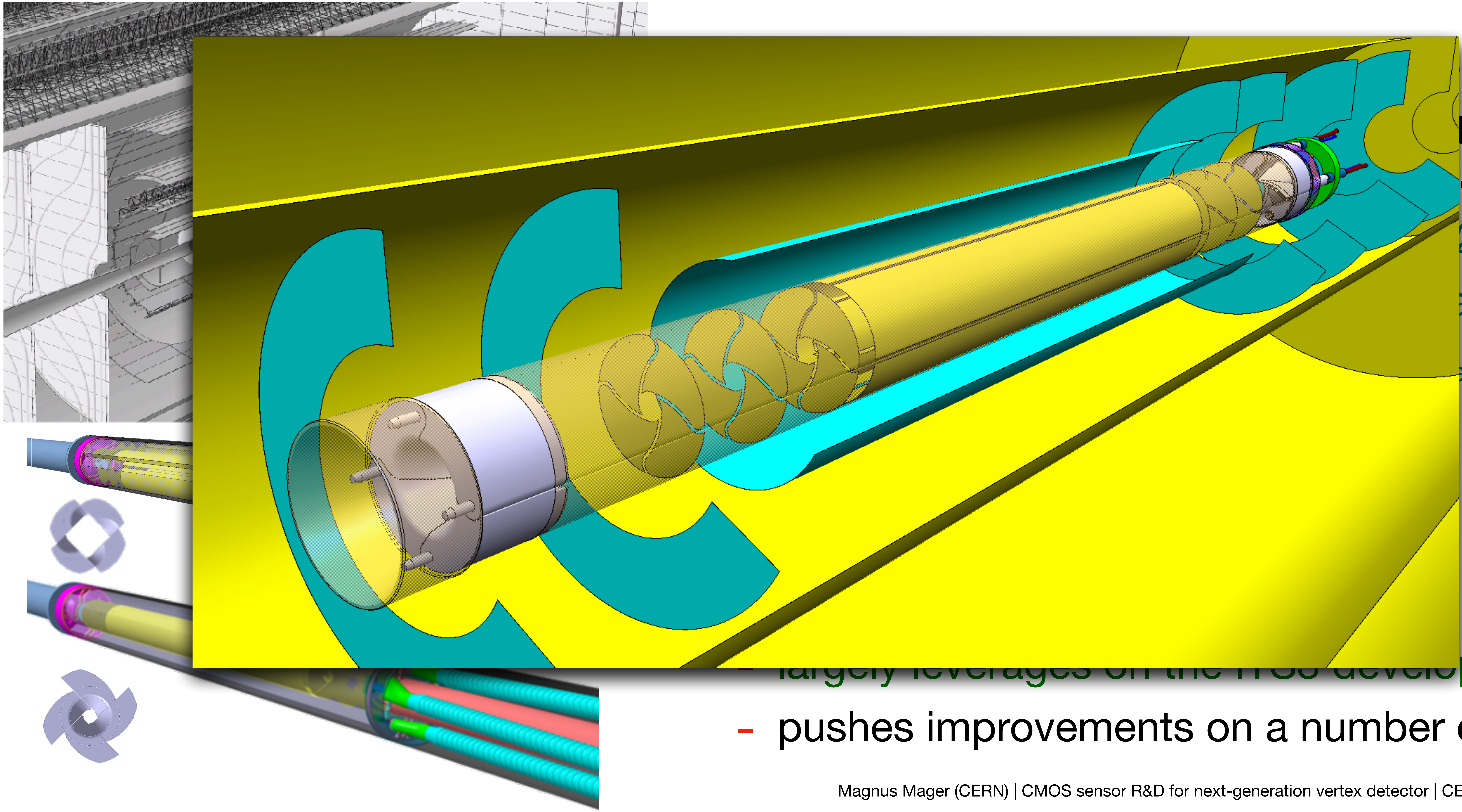
ayer

$_{eq}$/cm^2 +

- largely leverages on the ITS3 developments
- pushes improvements on a number of fronts

ALICE 3

vertex detector



d MAPS

t: 5 mm

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$_{eq}$/cm^2 +

- largely leverages on the ITS developments
- pushes improvements on a number of fronts

Summary

- **ALICE** is continuously developing cutting edge low-material, high-resolution vertex and tracking detectors

- ALICE **ITS2** (now)**:**
  - **10 m² 12.5 GPixel** tracker based on the **ALPIDE** chip (180 nm)

- ALICE **ITS3** (LS3) project is on track, significantly pushing MAPS R&D:
  - **65 nm** process qualified
  - **stitched design** exercised, *testing started*

- With **ALICE 3** (LS4), the R&D will continue in a natural way:
  - increased **spatial resolution**, **radiation hardness** and **rate capabilities** + **in-vacuum operation** (vertex detector)

- **Developed concepts and technology very well suited for future lepton colliders**


Thank you!
DRINK ME