Development of a wafer-scale CMOS pixel sensor for particle detection

Liang Zhang[1]

on behalf of

Yang Zhou[2], Chenxu Wang[3], Min Luo[3], Anqing Wang[1], Leyang Dou[3], Ruikai Zhang[3], Guoqiang Yan[2], Jianing Dong[1], Mingyi Dong[2], liangchenglong Jin[2], Long Li[1], Qinglin Geng[1], Linghui Wu[2], Guangyan Xiao[2], Meng Wang[1]

[1]Institute of Frontier and Interdisciplinary Science and Key Laboratory of Particle Physics and Particle Irradiation, Shandong University, Qingdao, 266237, Shandong, China

[2]Institute of High Energy Physics Chinese Academy of Sciences, 19B Yuquanlu, 100049, Beijing, China

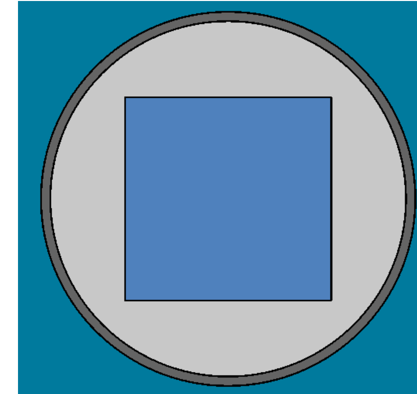
[3]School of Information Science and Engineering, Harbin Institute of Technology, Weihai 264209, China

Outline

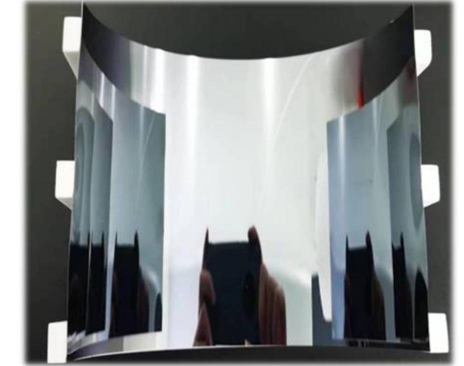
- **Motivation**
- **Wafer-scale CMOS pixel sensor R&D**
  - Architecture
  - Pixel circuit
  - Digital control and data processing
  - Stitching layout
  - Readout electronics
  - Wafer thinning and bending
- **Summary**

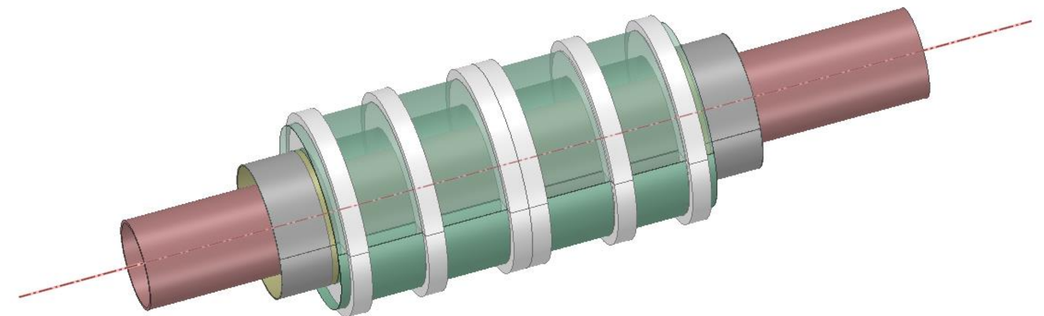
Motivation

- **Wafer-scale CMOS pixel sensor using stitching technology**
  - A wafer can be scribed into one die
- **Attractive features**
  - It can be bended with very thin thickness
    - ✓ Self-support
    - ✓ Few chips can form a cylinder
  - Very low material budget
    - ✓ The power consumption is mainly concentrated in the peripheral circuit
    - ✓ Cooling outside the sensitive area
    - ✓ Peripheral circuits are directly drawn out at the end
    - ✓ Less electronics pinout required
- **It has a high potential**
  - Being developed @ CERN for the ALICE-ITS3
  - For the inner tracker of BESIII, CEPC ....



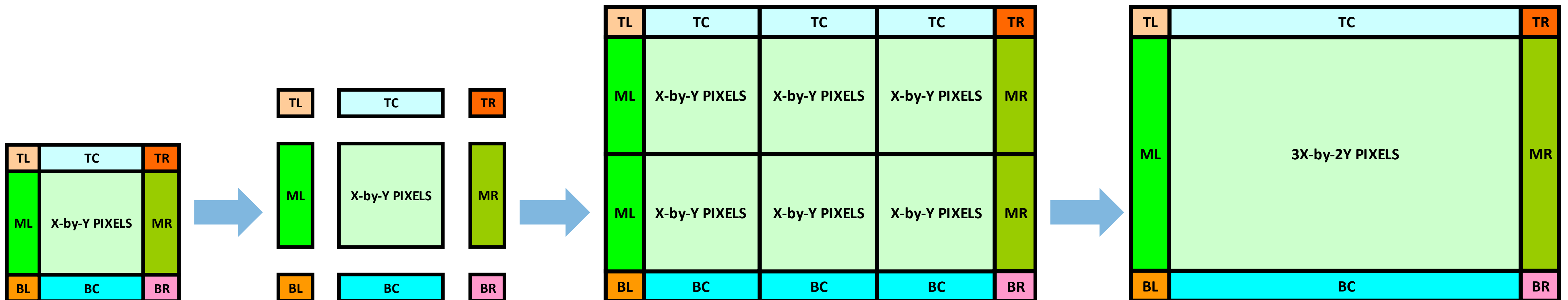
8 inch wafer





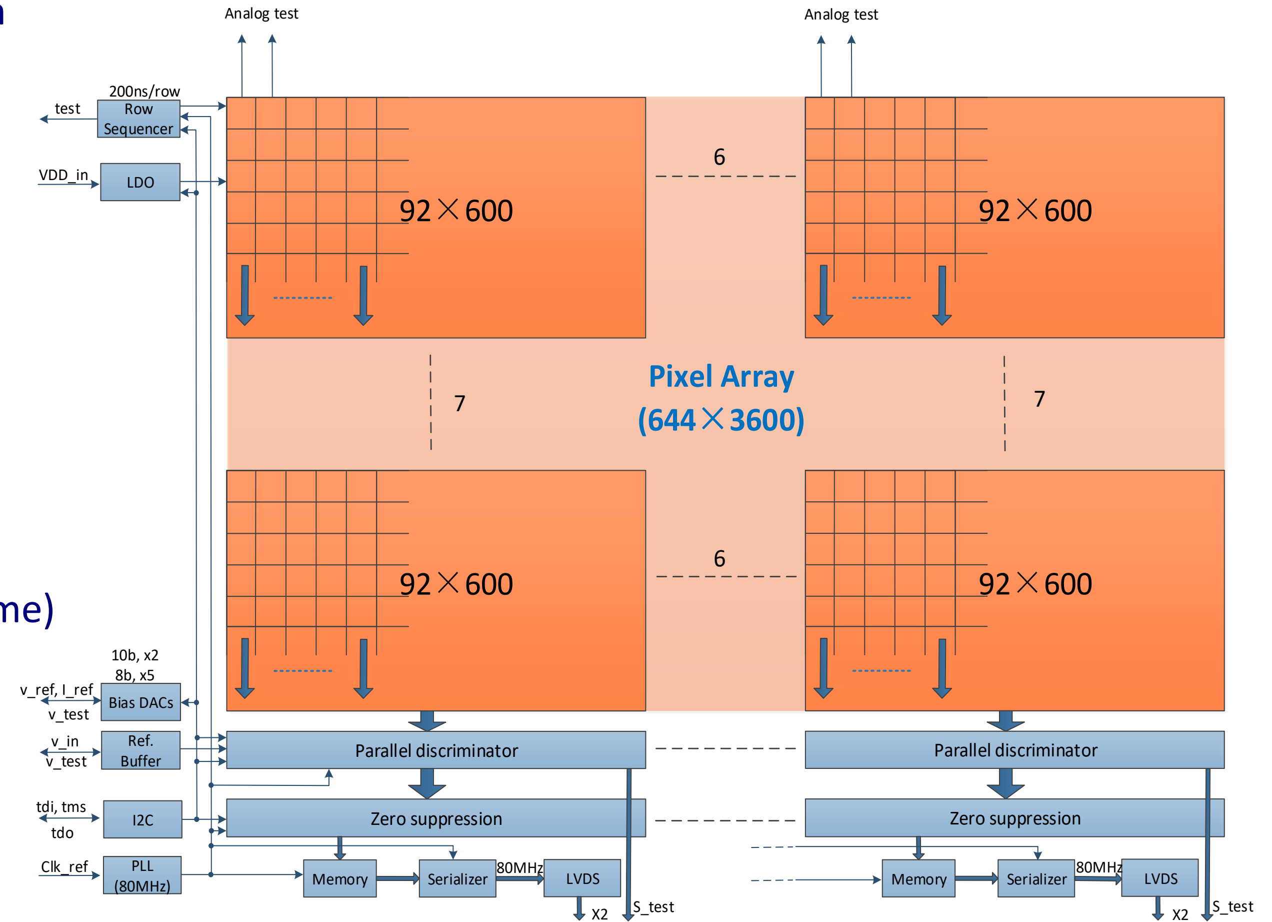
Wafer-scale CMOS pixel sensor

- The reticle size of the chip is about few cm^2
- Stitching technique has bee developed in order to realize larger chips
  - Up to a wafer-scale chip
- Stitching components
  - 9 segments: TL, TC, TR, ML, MC, MR, BL, BC, BR

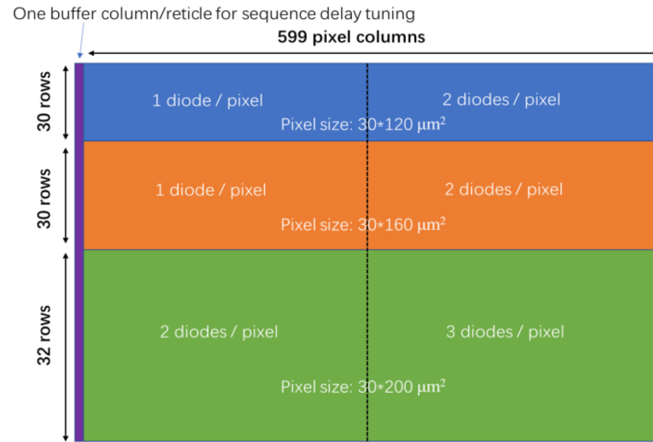


Chip architecture

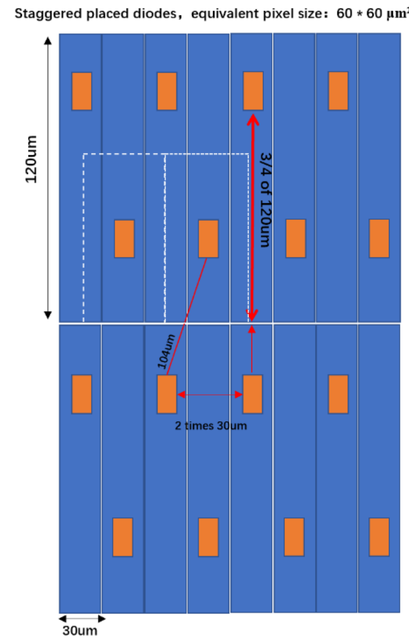
- **350 nm CIS process**
  - Epitaxial layer: thickness 14 µm, resistivity 500 - 2kΩ·cm
  - 4 metal layers
  - No deep P-well: PMOS cannot be used in pixel circuit
- **Total size**
  - ~11×11 cm^2 (only one die in a wafer)
- **Pixel array**
  - Basic pixel array: 92 rows × 600 columns
  - After stitching: 644 rows × 3600 columns
  - Rolling shutter readout mode (200 ns/row, ~129 µs/frame)
- **Full functional chip**
  - Analog test point for pixel array
  - Column-level discriminator
  - On-chip zero suppression
  - Interface: Bias DAC/Buffers/I2C/PLL/LVDS/LDO ……
- **Submitted in Feb 2023**

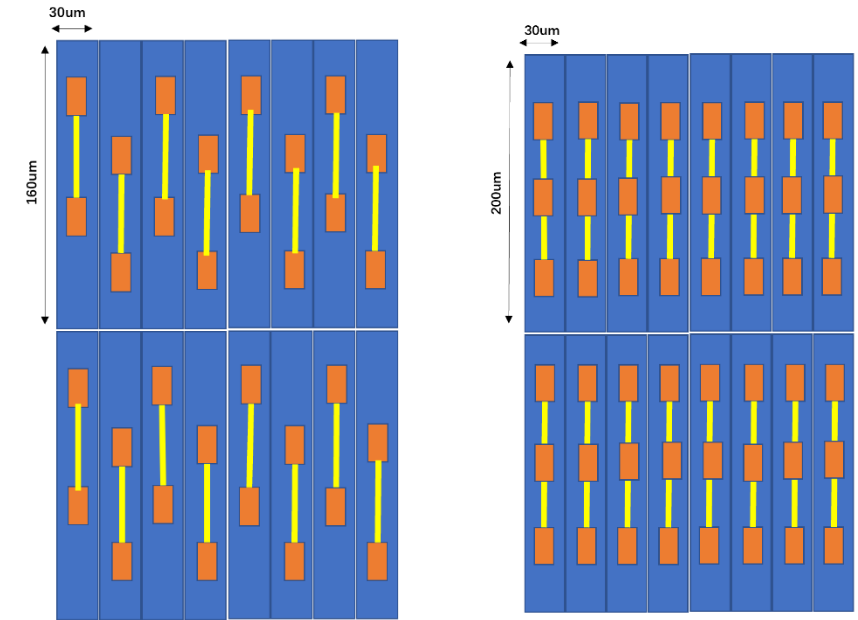


Pixel architecture and column readout



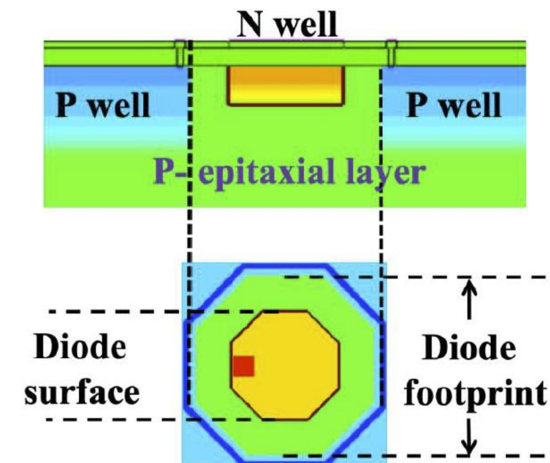
Basic pixel array with 6 submatrices





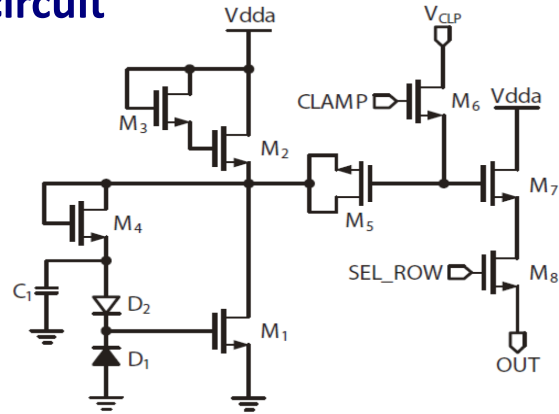
3 different diode arrangements are used

- **Rectangular pixels: increased readout speed**
  - rϕ : 30 μm
  - Z : 120/160/200 μm
- **6 submatrices:** study charge collection and charge sharing
  - Different pixel sizes and diode arrangements
- **Octagonal diode:** 20 μm^2
- **Diode surface/footprint:** 0.1

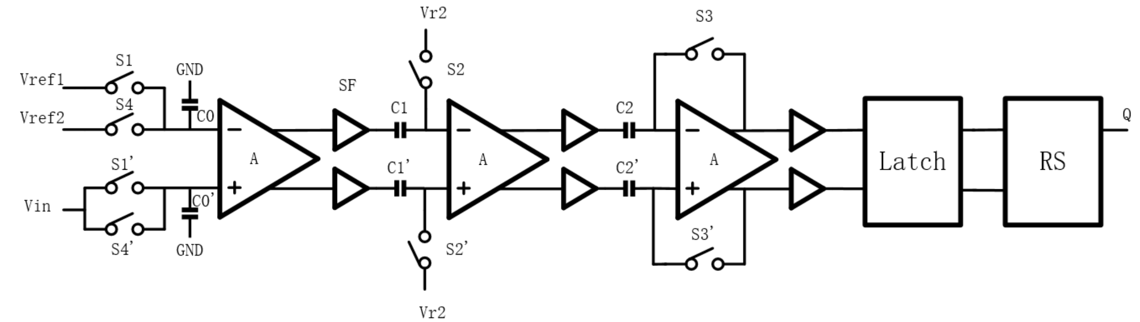


Pixel architecture and column readout

In-pixel circuit



Column-level discriminator



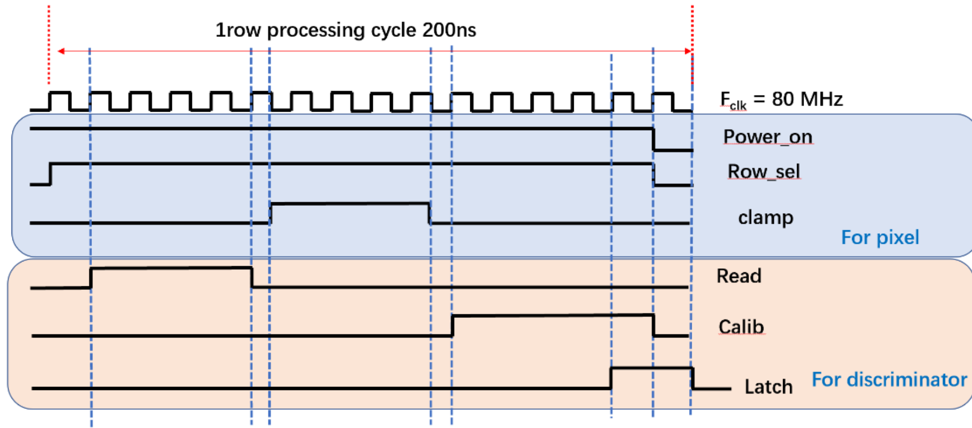
Diodes No.	Amp. Gain	SF	CVF [μV/e⁻]
1	14	0.8	135
2	13.5		75
3	11		40

*Reference: A.Dorokhov, “Optimization of amplifiers for Monolithic Active Pixel Sensors”, IPHC

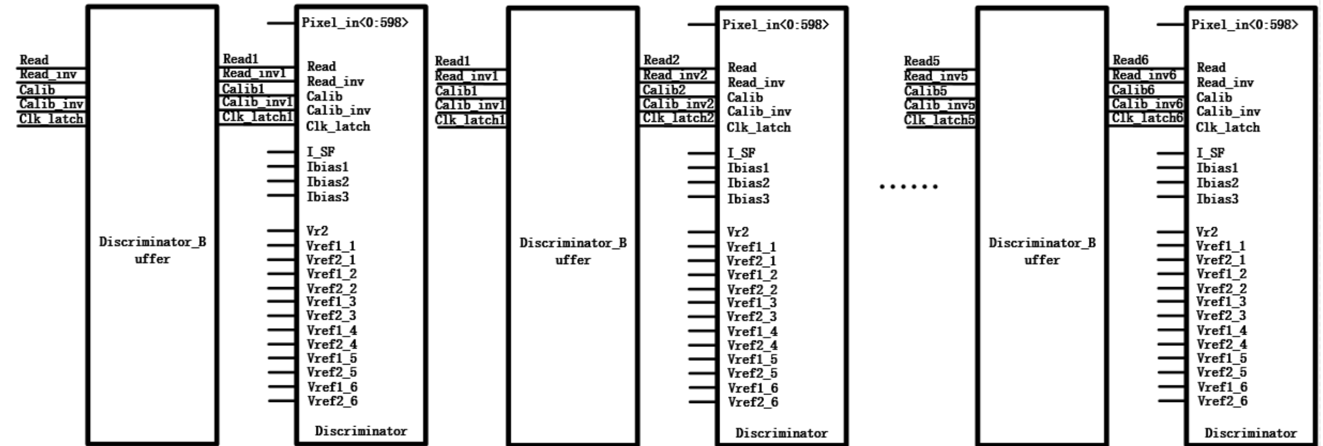
Discriminator performance:

- Offset cancellation technique
- Threshold: V_{ref1}-V_{ref2}
- Power consumption: 134 μW
- Area: 30×290 μm^2
- Thermal noise: 158 μV

Pixel architecture and column readout



Timing for pixel and discriminator: 200ns @ 80 MHz clock

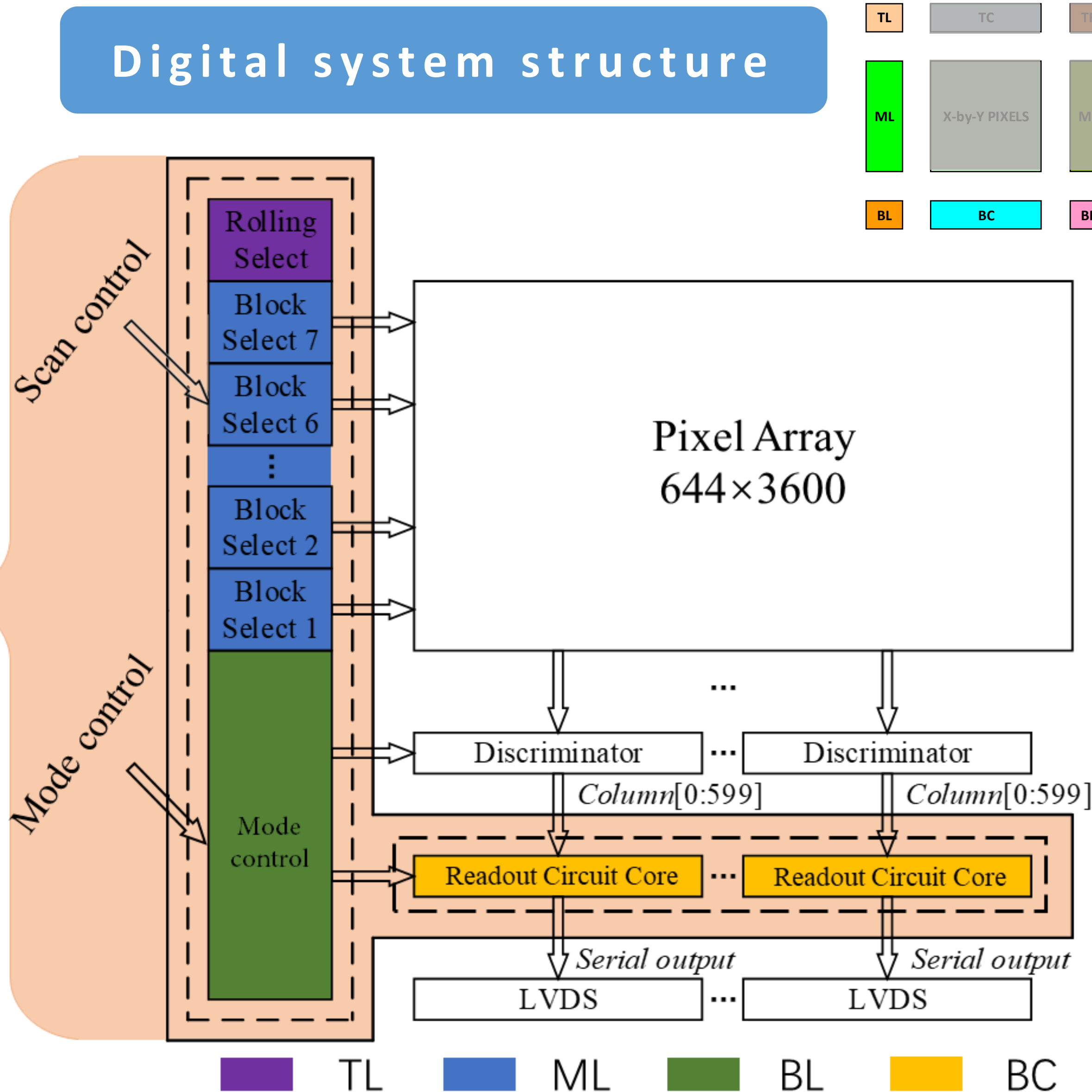


Combination of total 3600 column-level discriminators

- **Basic clock 80MHz**
  - 200 ns/row
  - Readout time: ~ 129 µs/frame
- **Power consumption**
  - ~ 25 mW/cm^2 (pixel matrix area)

- **Every 600 columns driven by one buffer**
  - Improve driving capability, reduce delay time, keep timing matching
- **Threshold voltages Vref1 & Vref2 are divided into 6 groups**
  - Increase drive capability, reduce settling time

Digital control and data processing



Functions

Scan control

- ❑ Provide rolling shutter sequence
- ❑ Composed of 7 blocks with 92 rows each block

Mode control

- ❑ Integrate interactive interface
- ❑ Change working mode & generate control signal

Readout circuit core

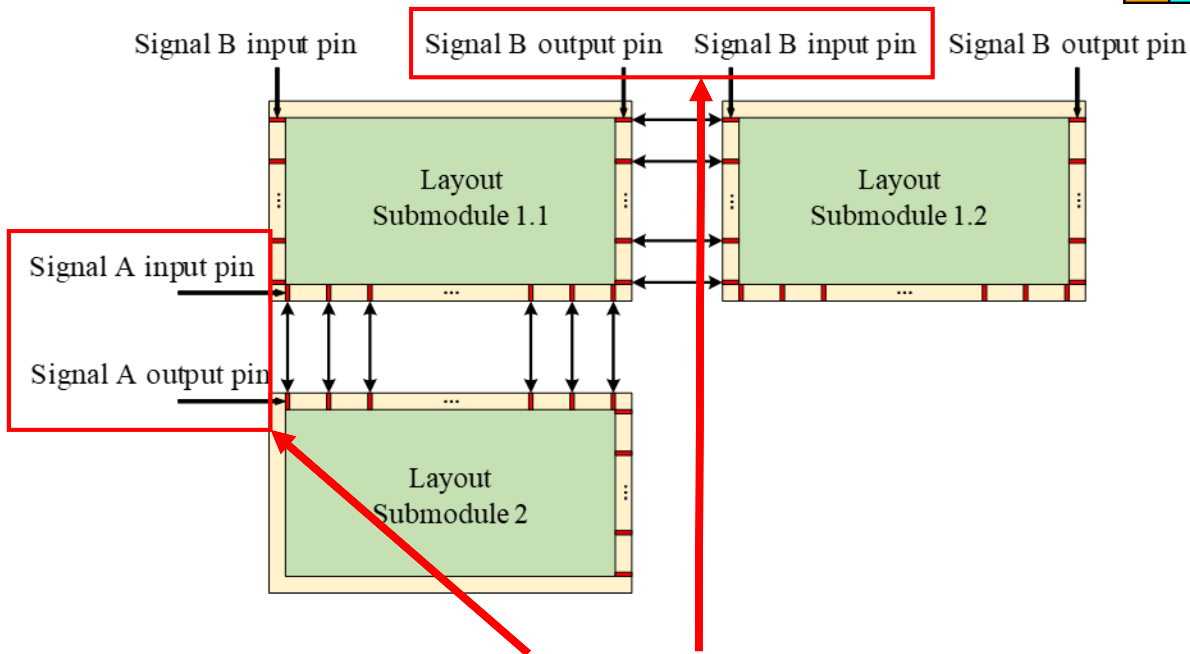
- ❑ Data readout, suppression, storage and serial output
- ❑ Composed of 6 blocks with 600 columns each block

Digital control and data processing

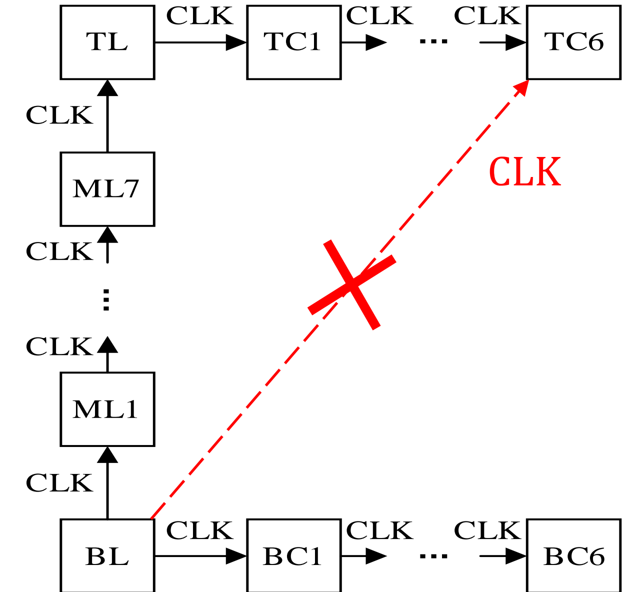
Signal transmission between sub-modules

TL	TC	TC	TC	TR
ML	X-by-Y PIXELS	X-by-Y PIXELS	X-by-Y PIXELS	MR
ML	X-by-Y PIXELS	X-by-Y PIXELS	X-by-Y PIXELS	MR
BL	BC	BC	BC	BR

Place & route in long distance

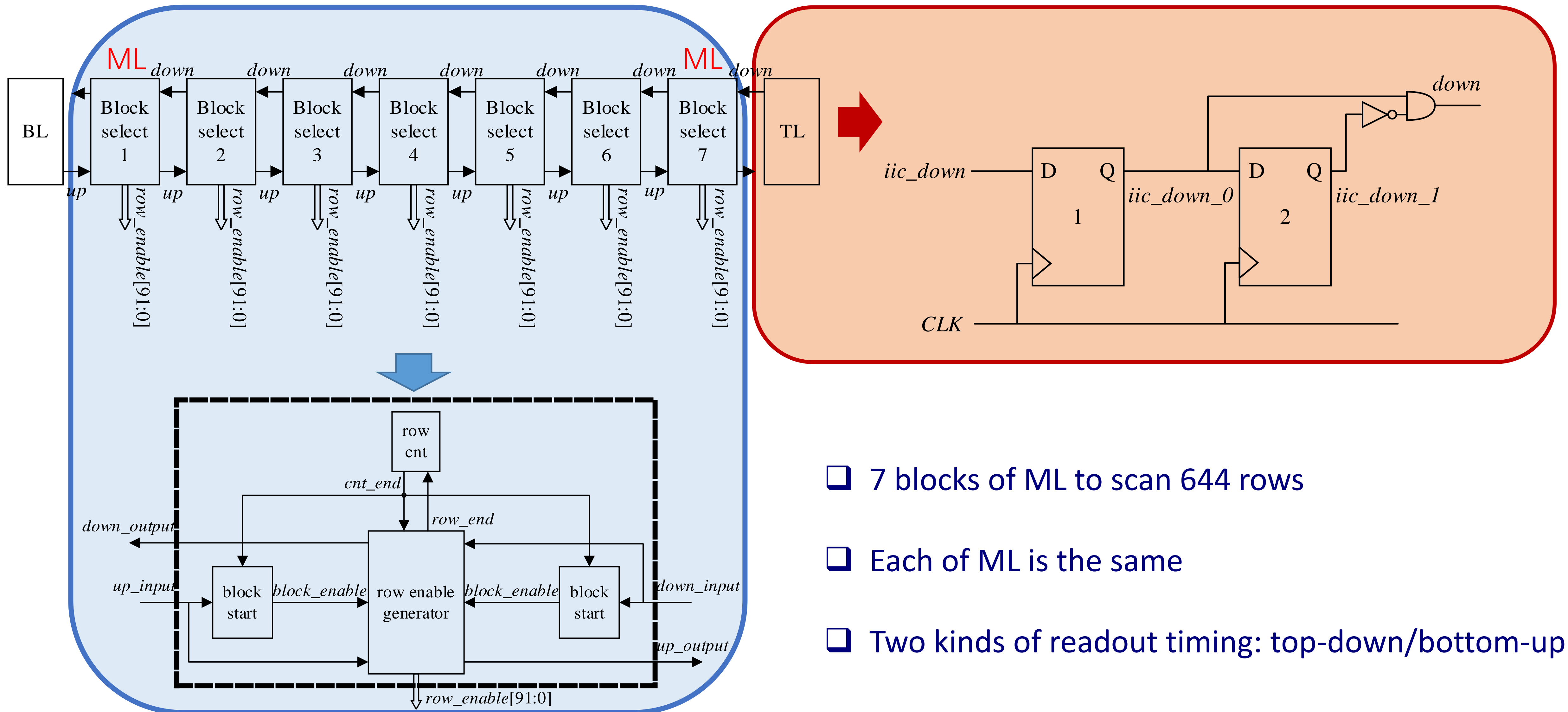


Pin-position between sub-modules MUST be matched



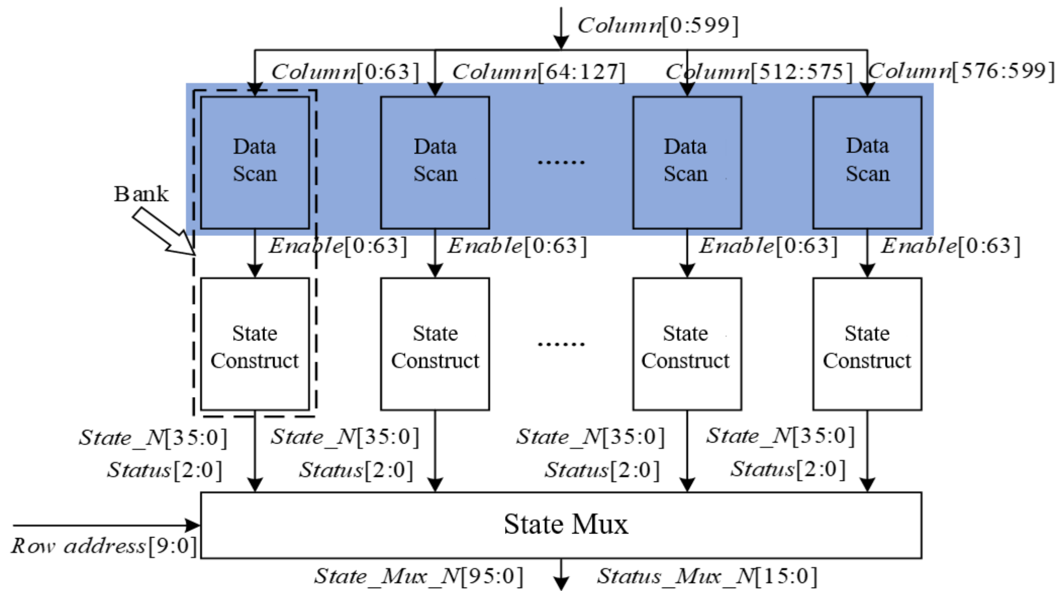
Cross-module signal transmission route MUST be carefully planned

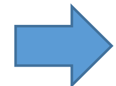
Digital control and data processing – scan control

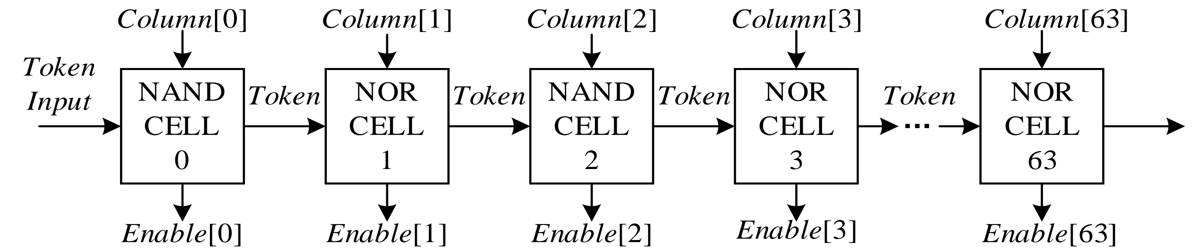


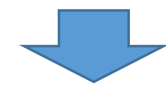
- 7 blocks of ML to scan 644 rows
- Each of ML is the same
- Two kinds of readout timing: top-down/bottom-up

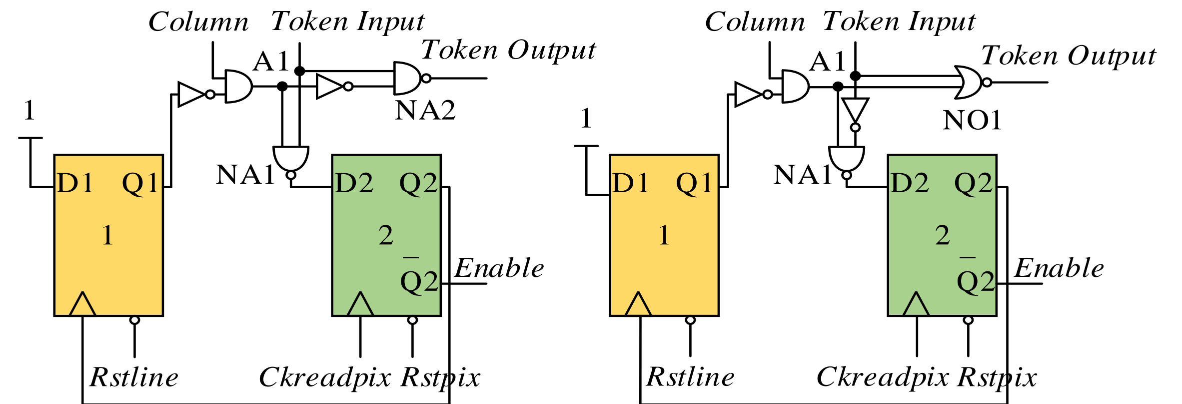
Digital control and data processing – readout circuit





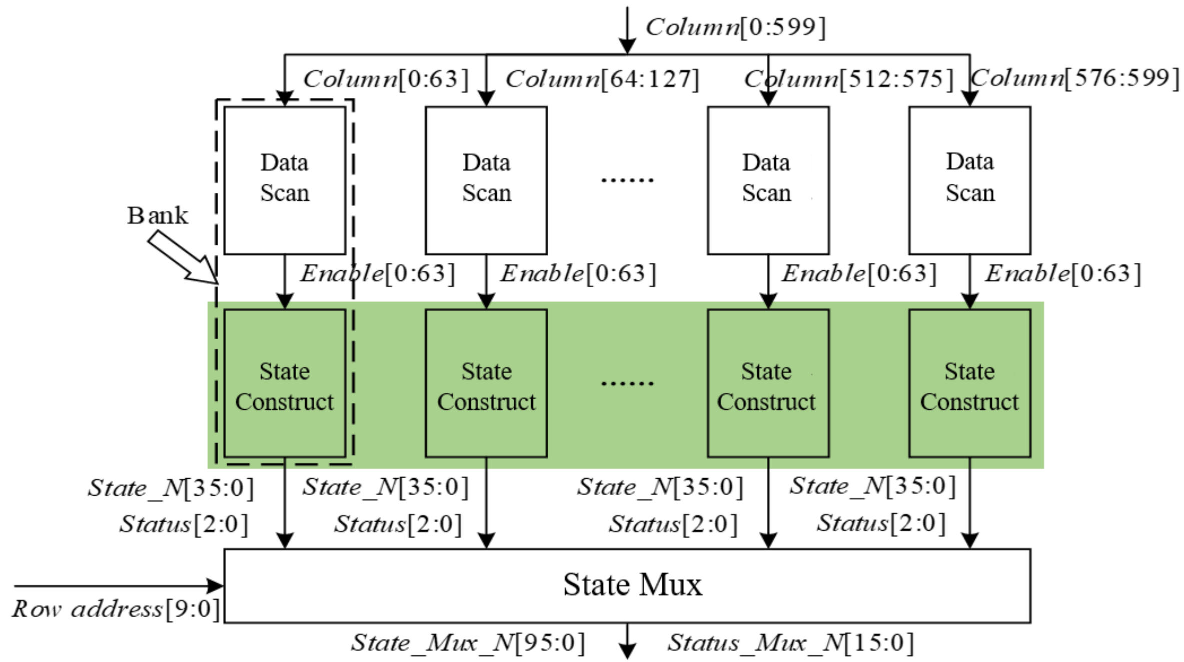


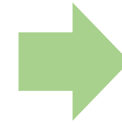


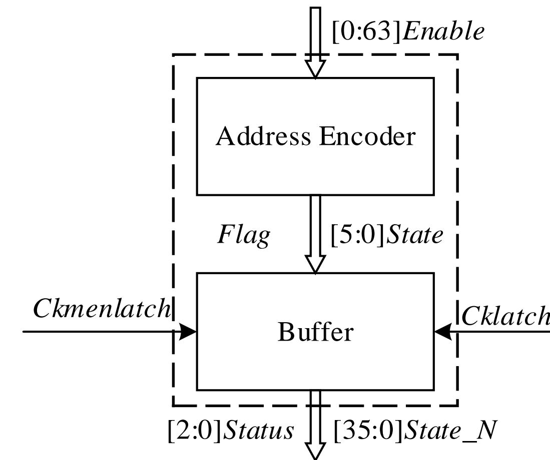


- The column outputs are divided into 10 groups, each group consisting of data scan and state construct.
- **Token blocker:** if there is a signal in the column, the token is blocked.
- **Token unlocker:** if the token is blocked, 'enable' is valid and the token is unlocked after the next input arrives.
- Through the token chain, the hit is readout one by one with a 64-bit data format.

Digital control and data processing – readout circuit







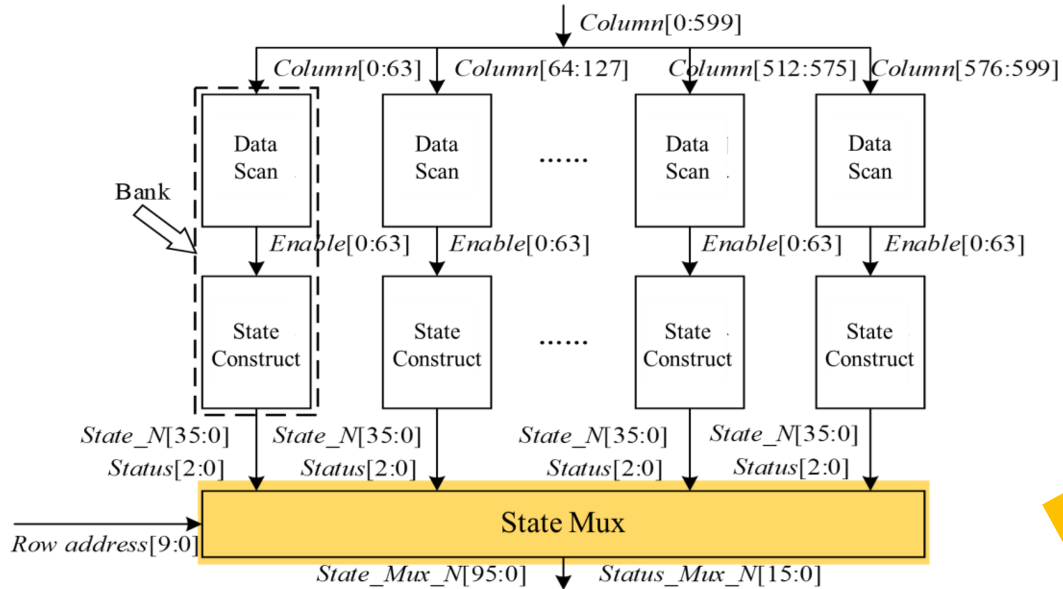
State															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0										
Mark						Address of BANK				Address in BANK					

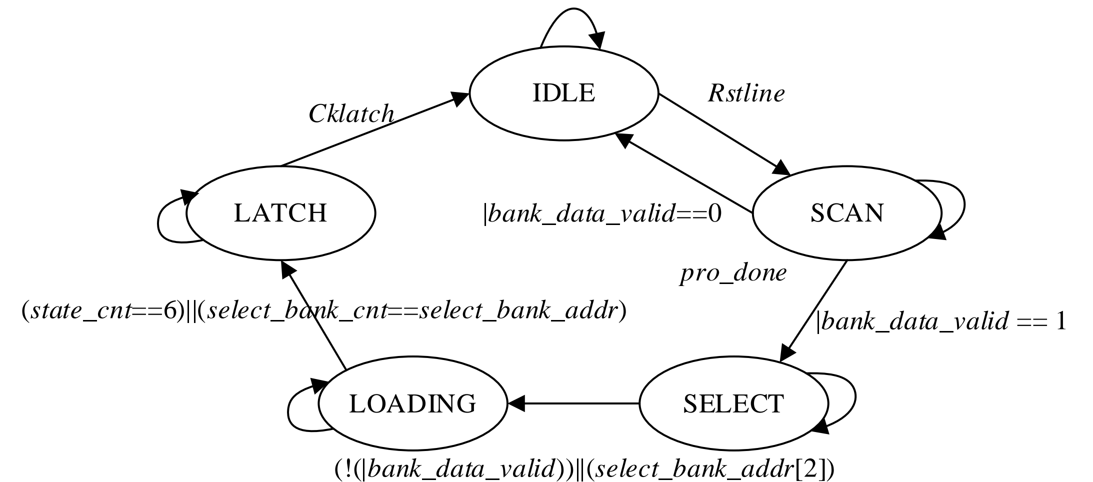
Status															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
1	1	0													
Mark			Number of State			Row address									

To be encoded   Already encode

- **Address encoder:** encode the 64-bit wide Enable signal into a 6-bit wide state.
- **Data buffer:** collect all the states in a bank and encode into status.

Digital control and data processing – readout circuit





State															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0										
Mark						Address of BANK				Address in BANK					

Status															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
1	1	0													
Mark			Number of State			Row address									

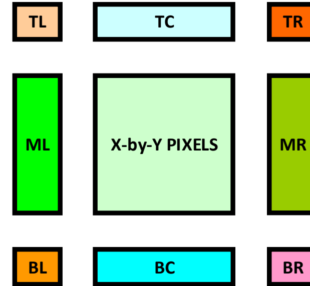
Encode during state mux (green) Already encode (blue)

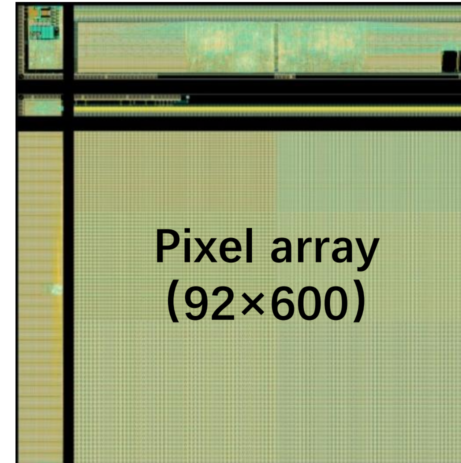
- **State mux:** Add Row and BANK address to status and state, respectively
- **compression ratio:** according to the physics environment, there are maximum 40 pixels in a column of reticle.

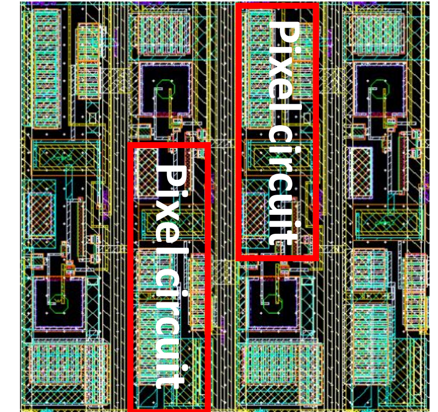
77: 1

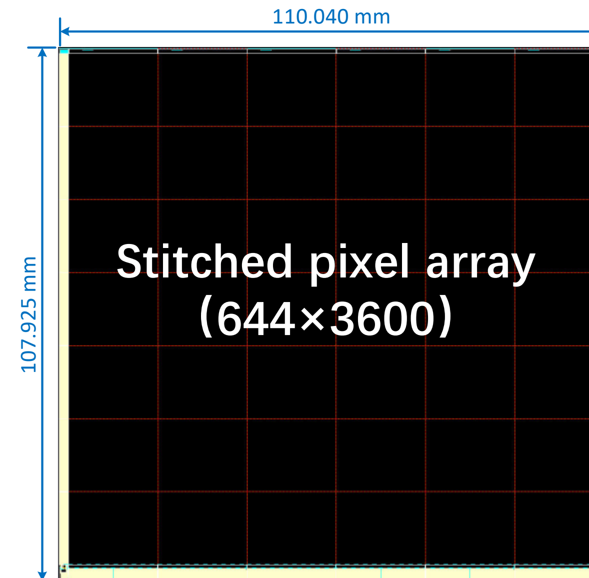
Stitching layout

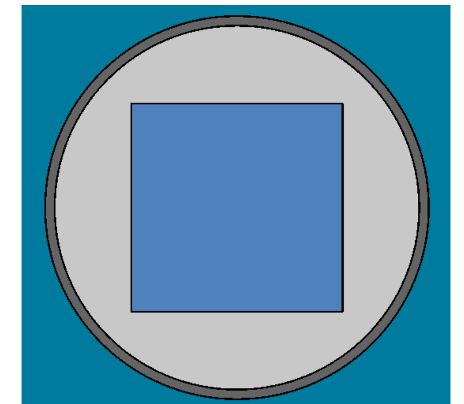
- **Reticle floorplan**
  - Area: ~ 2×2 cm^2
  - 9 groups of modules
    - TL,TC,TR,ML,MC,MR,BL,BC,BR
    - Pixel array in a reticle: 92×600
- **Stitching**
  - Area: ~ 11×11 cm^2
  - Pixel array
    - 7 rows and 6 columns
    - Total pixel array: 644×3600







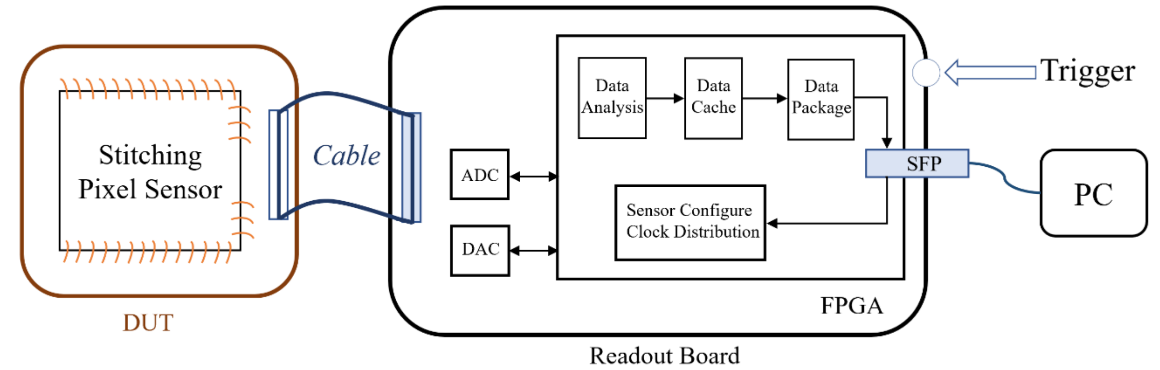


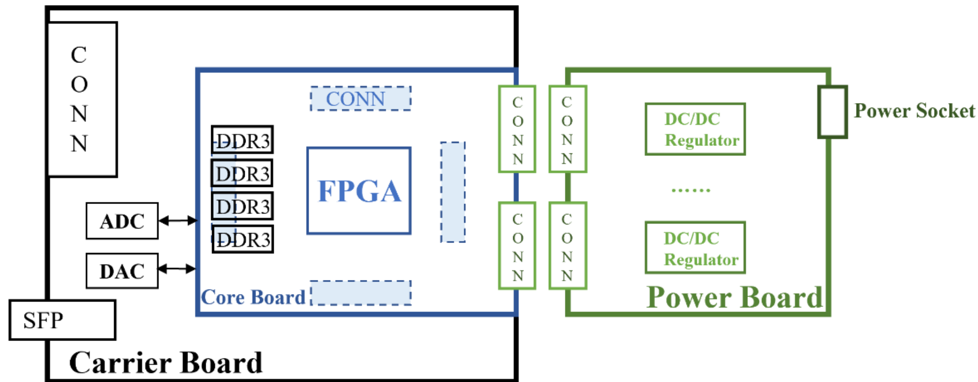


8 inch wafer
(die size 11 cm × 11 cm)

Readout electronics

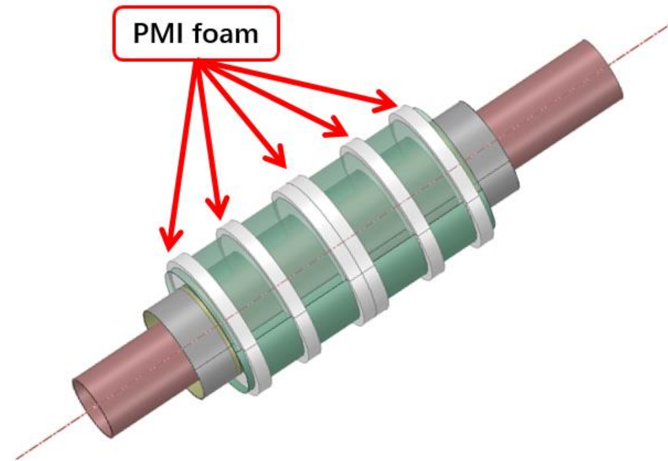
- **DUT board**
  - Few components, connector, wire bonding
- **Readout board**
  - FPGA core board: XC7K325T, DDR3
  - Carrier board: ADC, DAC
  - Power board: supply different voltages

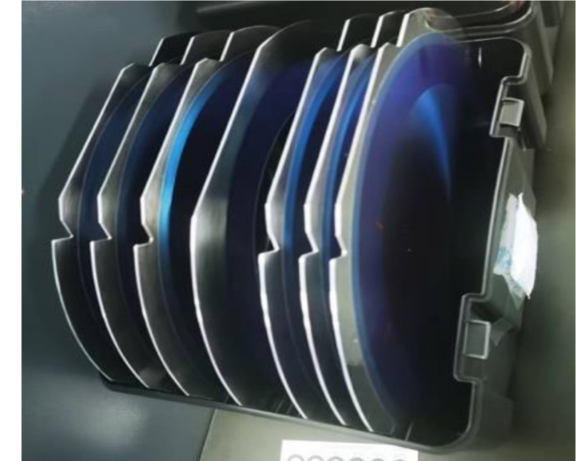


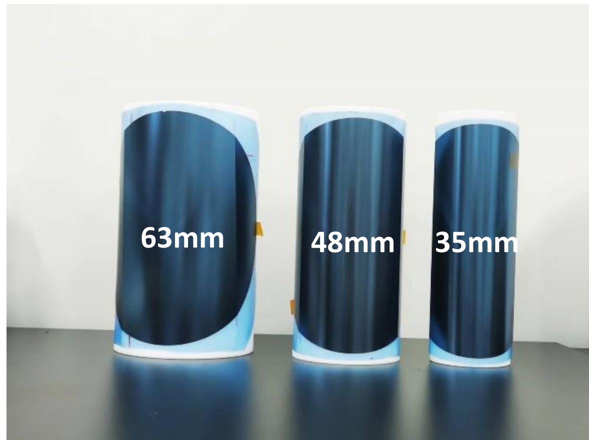


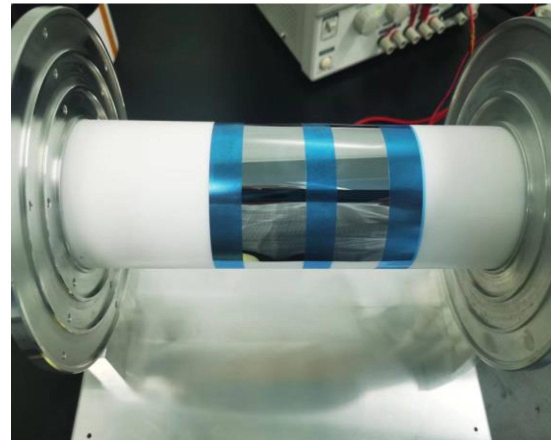
Wafer bending and bonding study

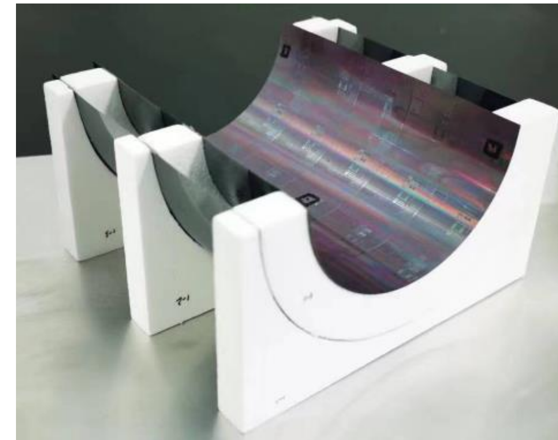
- Dummy wafer is used to thin down to 50 μm
- Wafer bending with different radii
- Ring support
  - Wafer bending and fixed with glue
  - PMI: High strength, low material, mass density is about 0.05g/cm^3

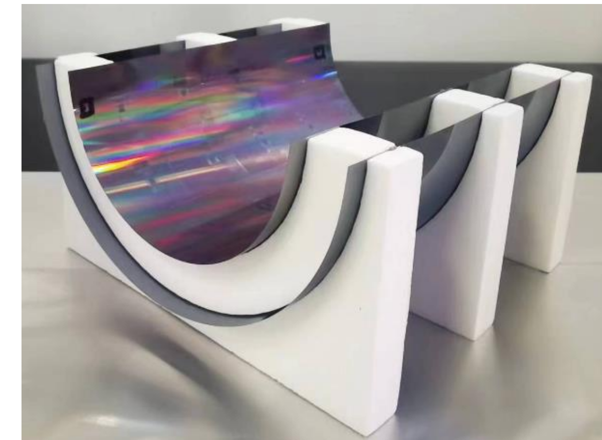








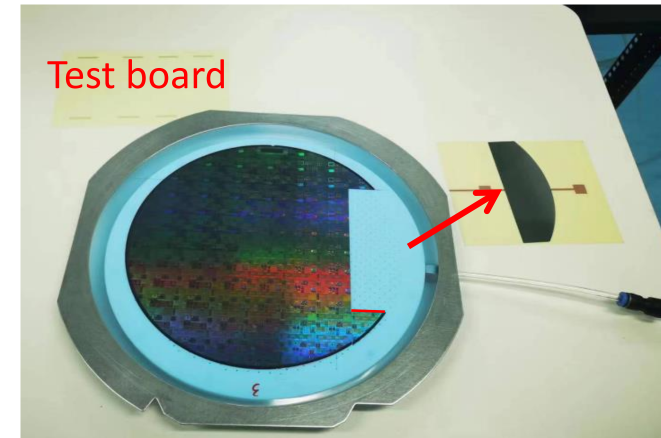


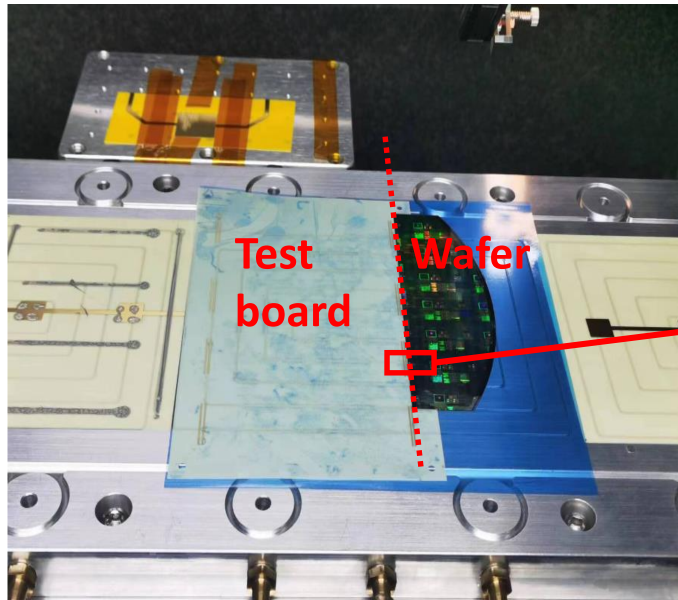


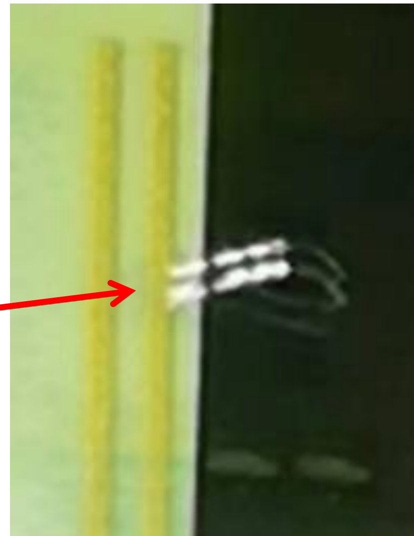
Wafer bending with radii 63mm, 48mm and 35mm

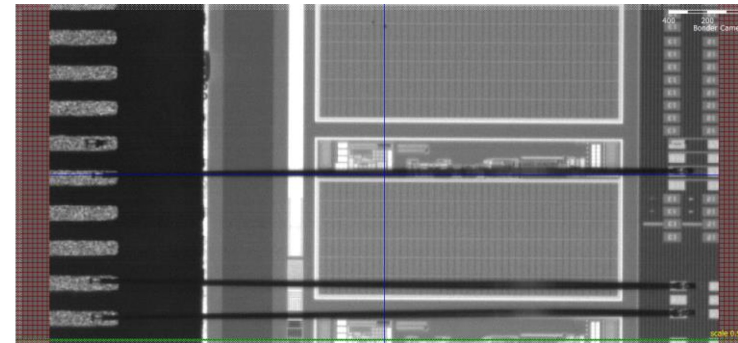
Wafer bending and bonding study

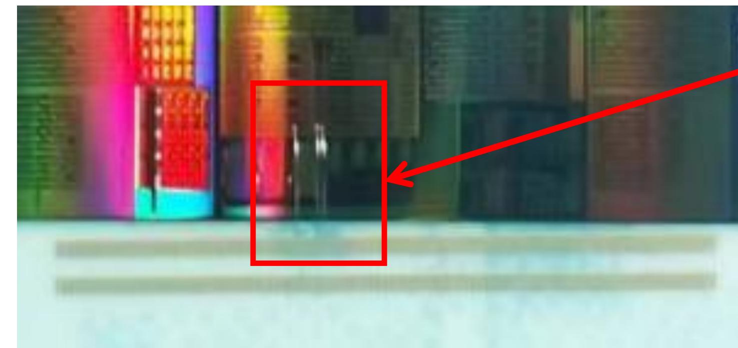
- **Wire bonding with thinned dummy wafer**
  - Dicing a part of dummy wafer
  - Bonding with test board
  - The wire shape doesn't change after bending

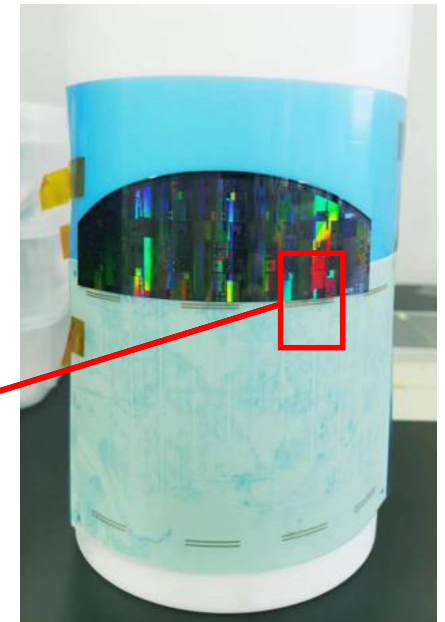












Summary

- The thinned wafer-scale CMOS pixel sensor will have extremely low material budget, having a high potential for the inner tracker.
- A wafer-scale sensor prototype has been designed and submitted. It expects to be back at the end of July.
- The readout electronics have been ready for the test.
- Wafer thinning and bending have been studied, and they perform well.

Acknowledgements

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Thanks