The Mighty Tracker project for the LHCb upgrade

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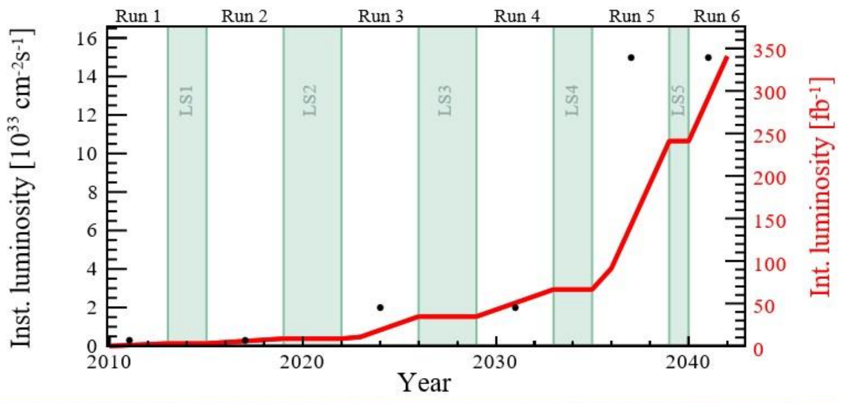
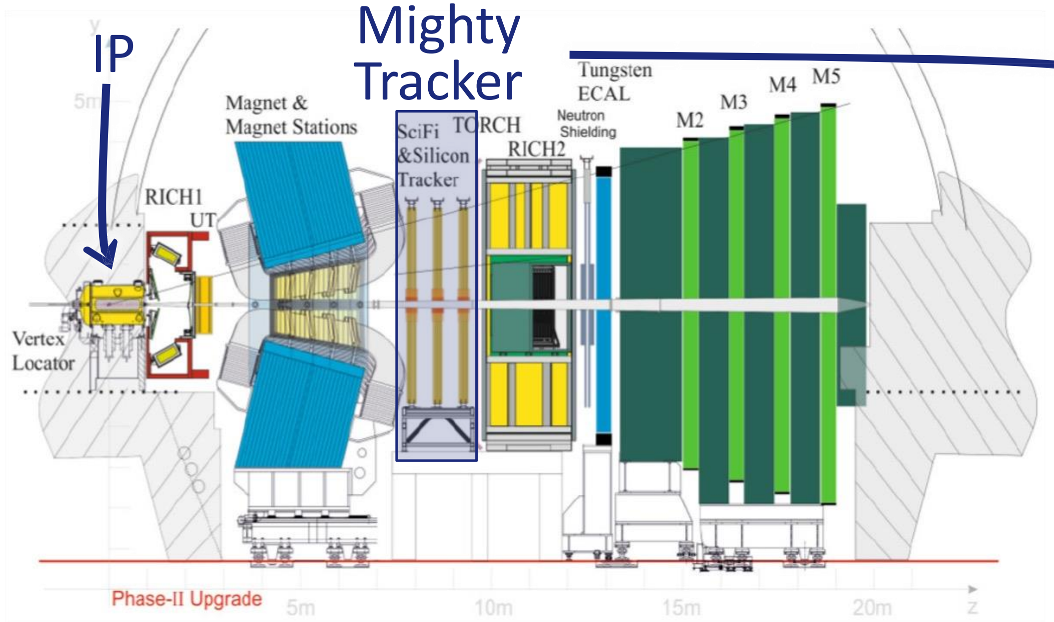
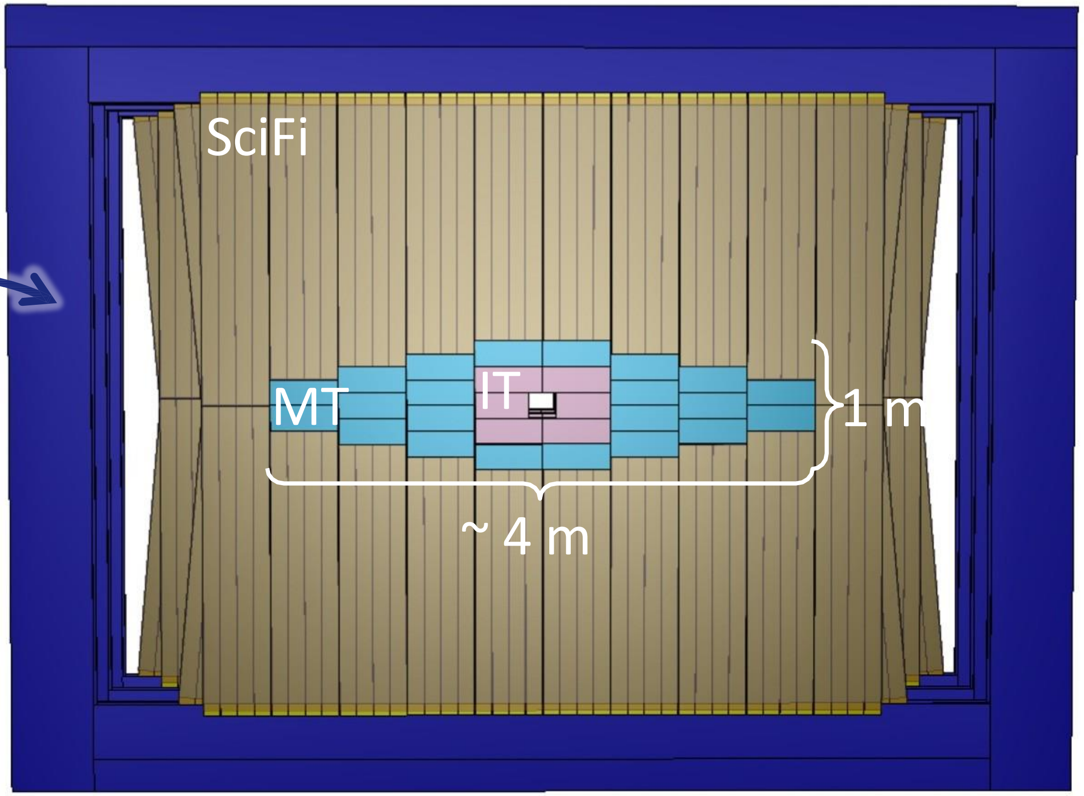
LHCb

- Towards High Luminosity LHC
  - Increased luminosity and data
- Major tracking detector system upgrade
  - Mighty Tracker
  - Proposed hybrid tracking detector to balance cost and physics/detector performance needs

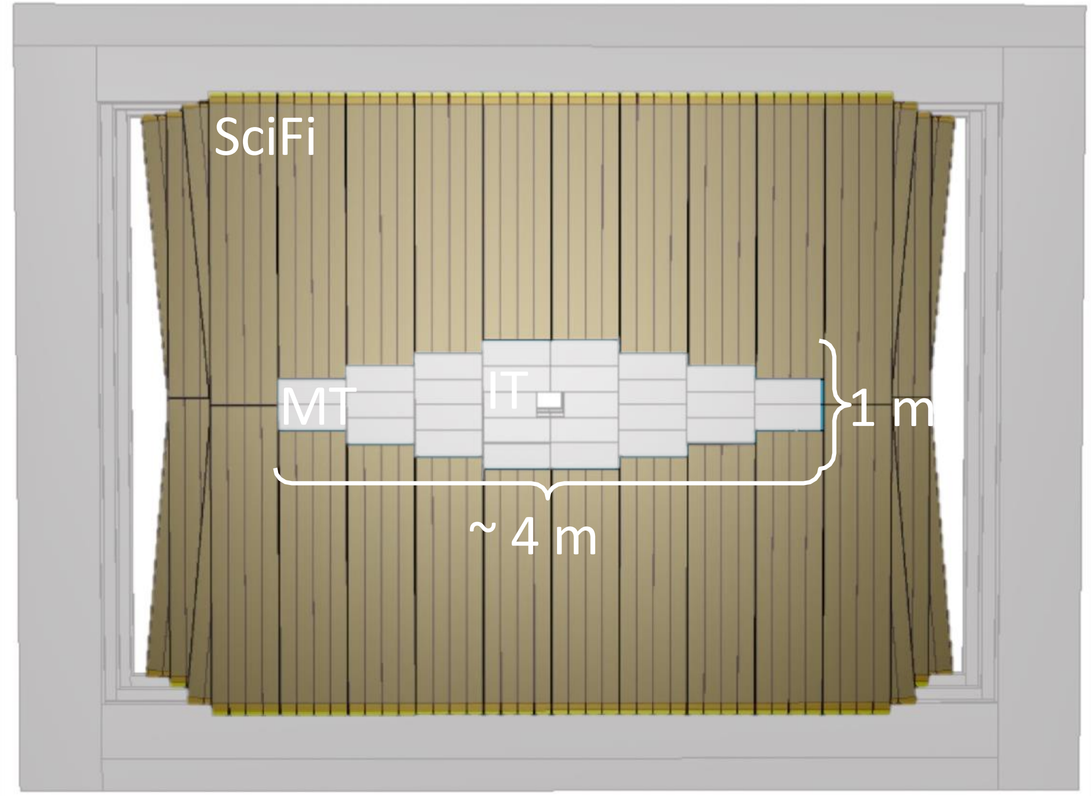






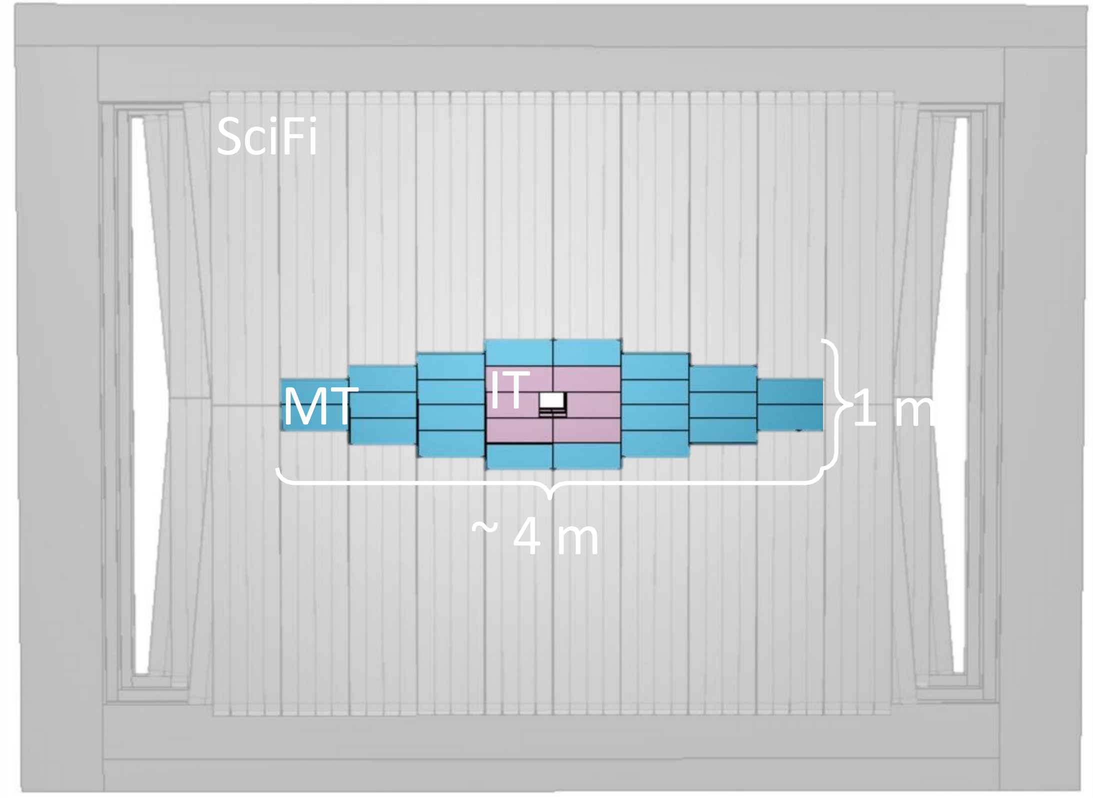
Mighty Tracker

- **Scintillating Fibre Tracker (SciFi)**
  - Outer region
  - Twelve layers of scintillating fibres with SiPM readout
  - Installed in LS2, replacements in LS3

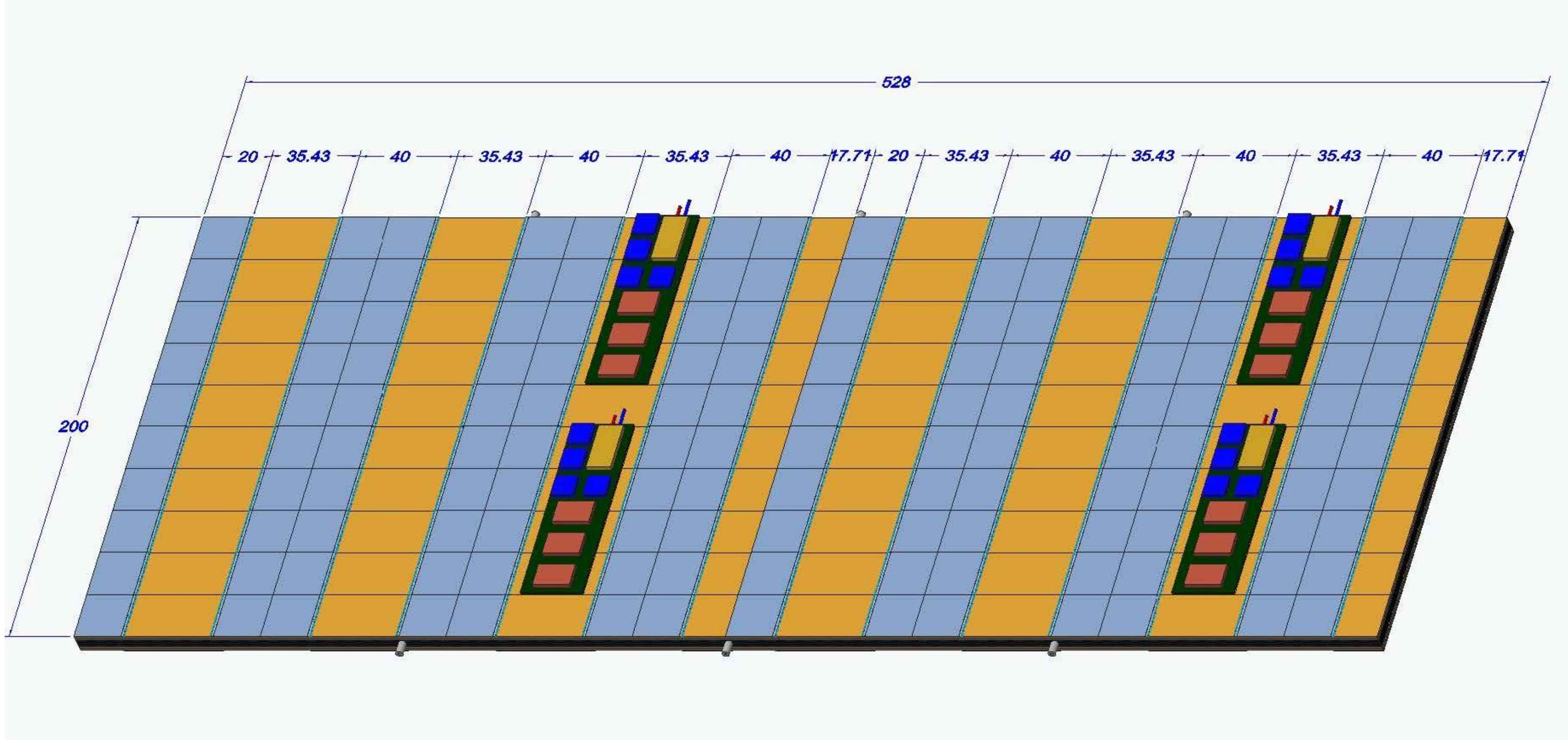


Mighty Tracker

- **Scintillating Fibre Tracker (SciFi)**
  - Outer region
  - Twelve layers of scintillating fibres with SiPM readout
  - Installed in LS2, replacements in LS3
- **Monolithic High Voltage CMOS sensors**
  - Inner Tracker (IT) and Middle Tracker (MT)
  - Instrument six layers with silicon sensors
    - HV-CMOS pixel chip MightyPix
  - To meet the anticipated requirements on granularity, radiation tolerance and cost
  - Installation in two stages: LS3 (Inner Tracker) and LS4 (Middle Tracker)
  - Total silicon area (IT + MT) $\sim 18\ m^2$ (minus beam-pipe hole)



Mighty Tracker modules



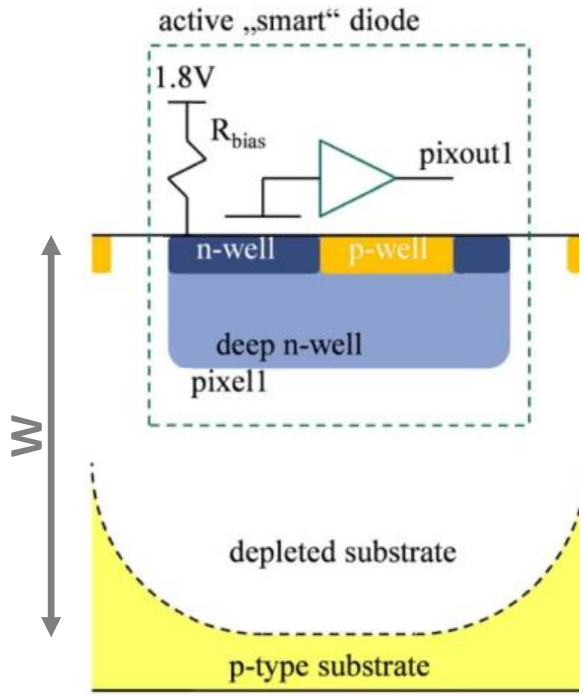
Source: Framework TDR for the LHCb Upgrade II

- **Single Mighty Tracker module**
  - Each grey rectangle represents an HV-CMOS pixel chip
  - The other side has an offset arrangement such that the entire plane is covered

Monolithic silicon sensors – High Voltage CMOS

- Sensor and readout chip integrated in single device
- In industry-standard High Voltage CMOS processes
  - No bump-bonding is needed
    - **Thin sensors (50 µm)**
    - **Small pixel size possible (50 µm x 50 µm)**
    - Faster production
    - Higher yields
    - More cost effective (100k€/m^2)
  - Large bias voltage (V_{bias} > 200 V)
    - **Fast charge collection by drift (< 200 ps charge collection and 3 ns time resolution)**
    - **Good radiation tolerance (10^{15} 1 MeV n_{eq}/cm^2)**
  - High resistivity wafers (10 Ω·cm < ρ < 2-3 kΩ·cm)
  - In-pixel amplification (strong signals)
  - High-rate capability

➔ $W = \sqrt{\rho \cdot V_{bias}}$



I. Peric, IEEE JSSC 2021

MightyPix: design challenges

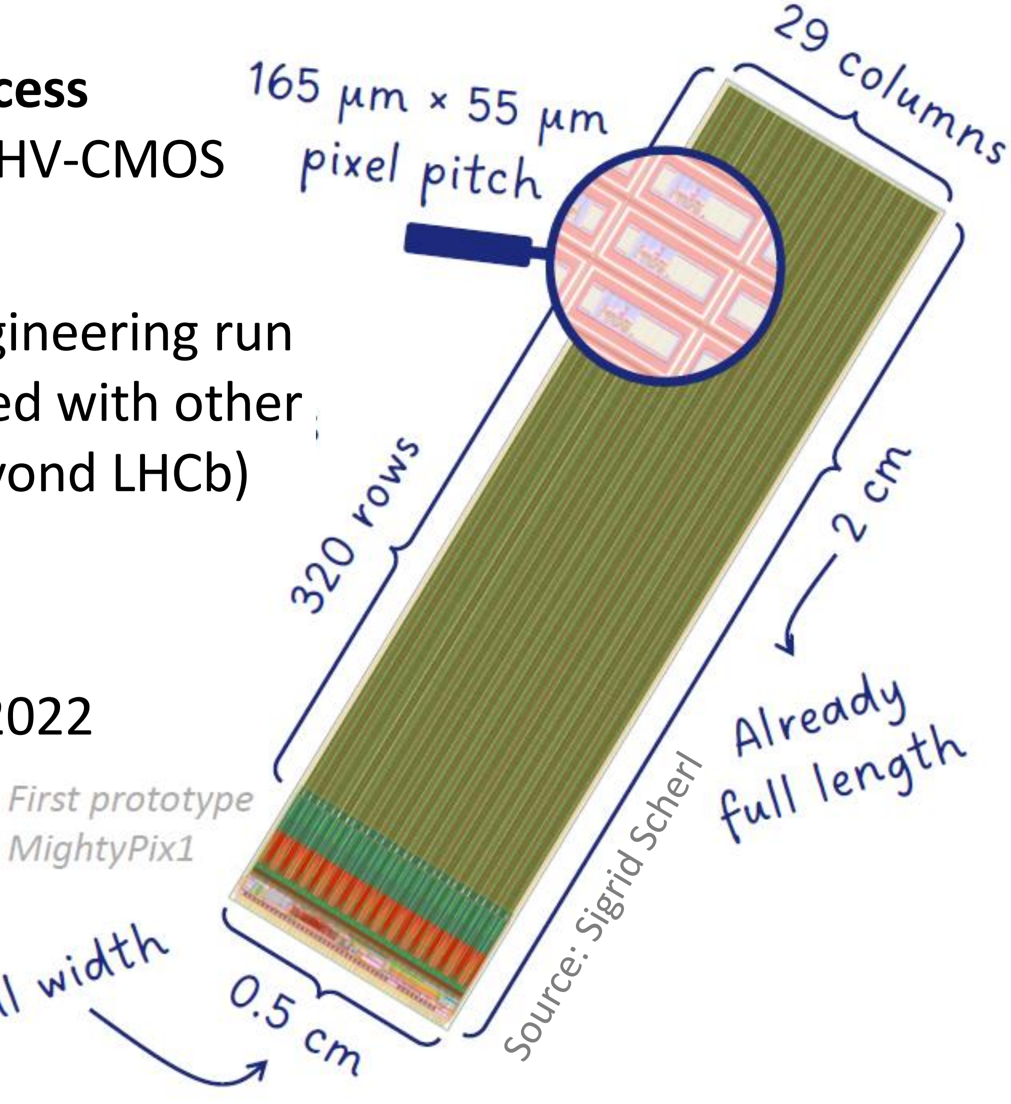
Parameter	Value
Chip size	~ 2 cm x 2 cm
Chip thickness	200 µm
Pixel size	< 100 µm x 300 µm (with smaller sizes to be explored)
Timing resolution	~ 3 ns
In-time efficiency	> 99% within 25 ns window
Power consumption	< 150 mW/cm^2
Data transmission	4 links of 1.28 Gb/s each
Radiation tolerance	6E14 1 MeV n_{eq}/cm^2 NIEL
Inactive area	< 5%
Compatibility with the LHCb readout system	

LHCb-INT-2019-007, 2019

- Dedicated R&D programme to develop a High Voltage CMOS sensor chip (MightyPix)
- The programme builds on previous designs ATLASPix (ATLAS ITk upgrade) and MuPix (Mu3e)

MightyPix1

- **Technology process**
  - TSI 180 nm HV-CMOS
- **Submission**
  - MPW in engineering run (wafer shared with other projects beyond LHCb)
  - May 2022
- **Delivery**
  - December 2022

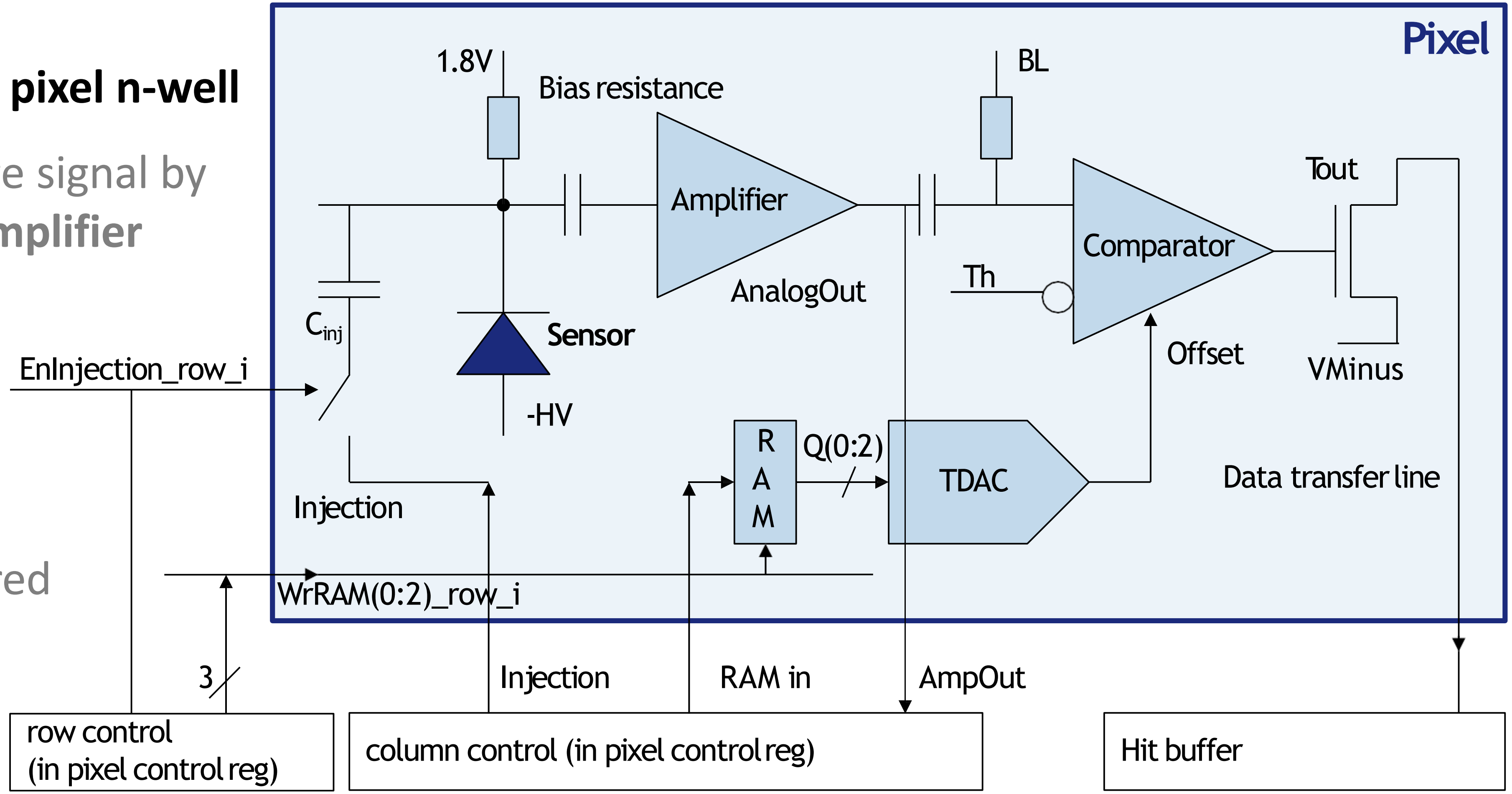


- **Data format**
  - 2 x 32 bit words per hit
- **Data output rate**
  - 1.28 Gbit/s going to lpGBT
- **Digital interfaces**
  - TFC: Timing and Fast Control
  - I2C: Slow Control
  - SR: Config. Shift register interface
- **Clock generation**
  - External: 40 MHz and 640 MHz coming from lpGBT
  - Internal: CML and CMOS PLL with 40 MHz reference clock
- **Bias voltages**
  - Integrated 10 bit voltage DACs

MightyPix1

Analogue readout

1. Charge collected by **pixel n-well**
2. Converted to voltage signal by **Charge Sensitive Amplifier**
3. Analogue voltage pulse converted to digital signal by **comparator**
4. Hit information stored in **hit buffer**



Source: Ivan Perić

MightyPix1

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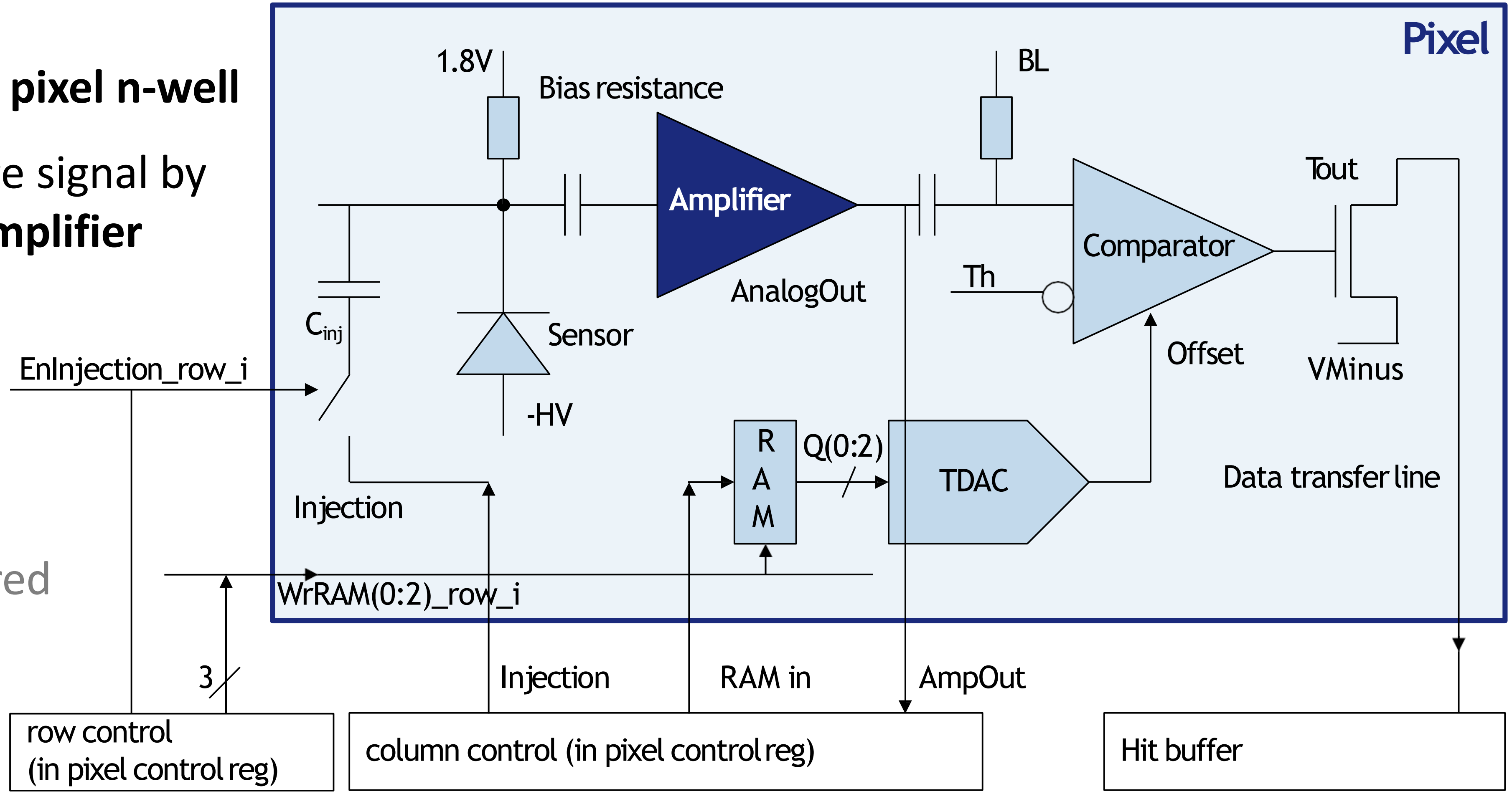
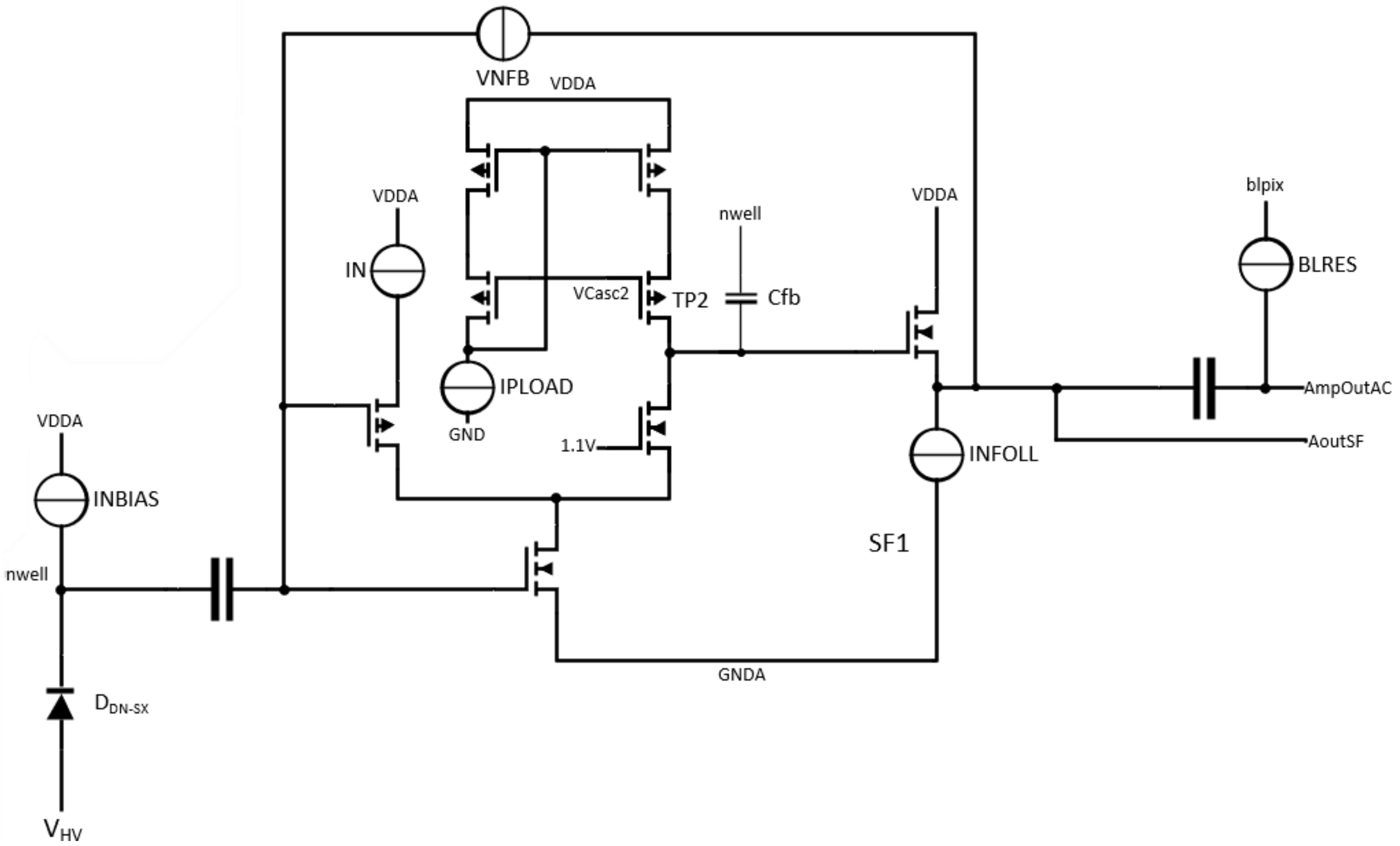


Source: Ivan Perić

MightyPix1

Amplifier

- Integrated inside the pixel
- CMOS type amplifier
- Equivalent Noise Charge (ENC) 67 e- (88 fF pixel capacitance)
- Time-walk 2.4 ns (2.4 ke- to 24 ke- signals)



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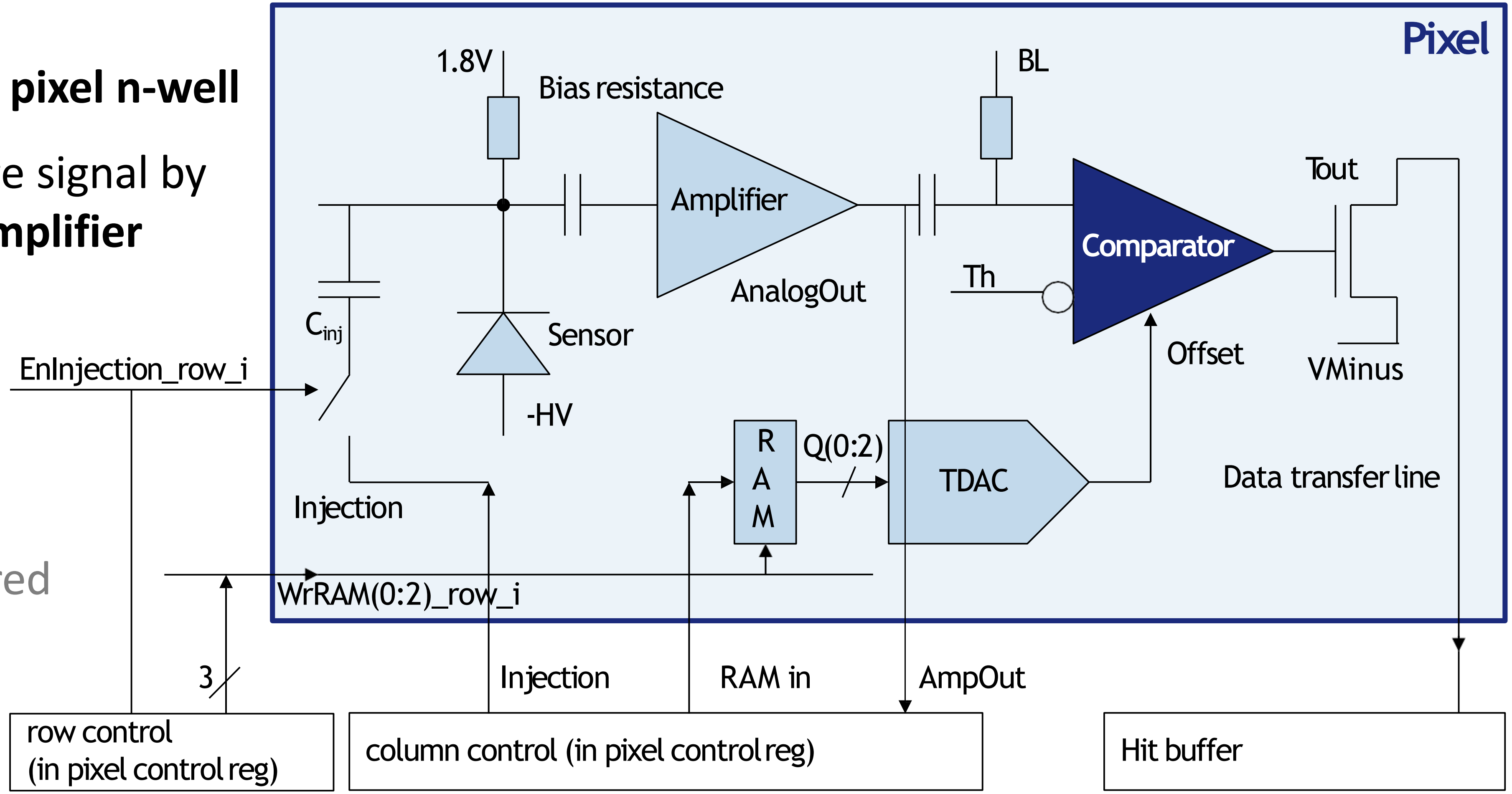

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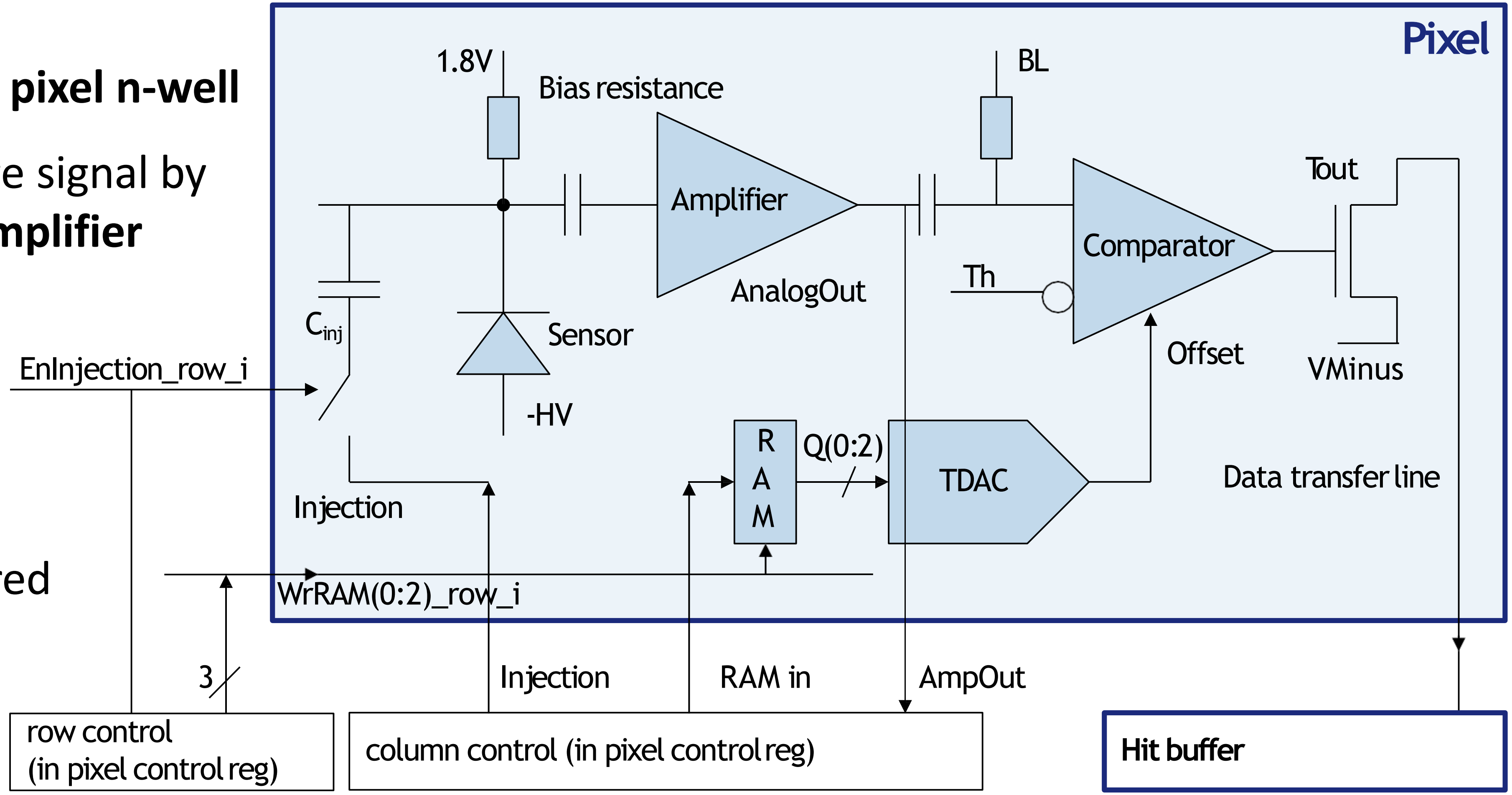
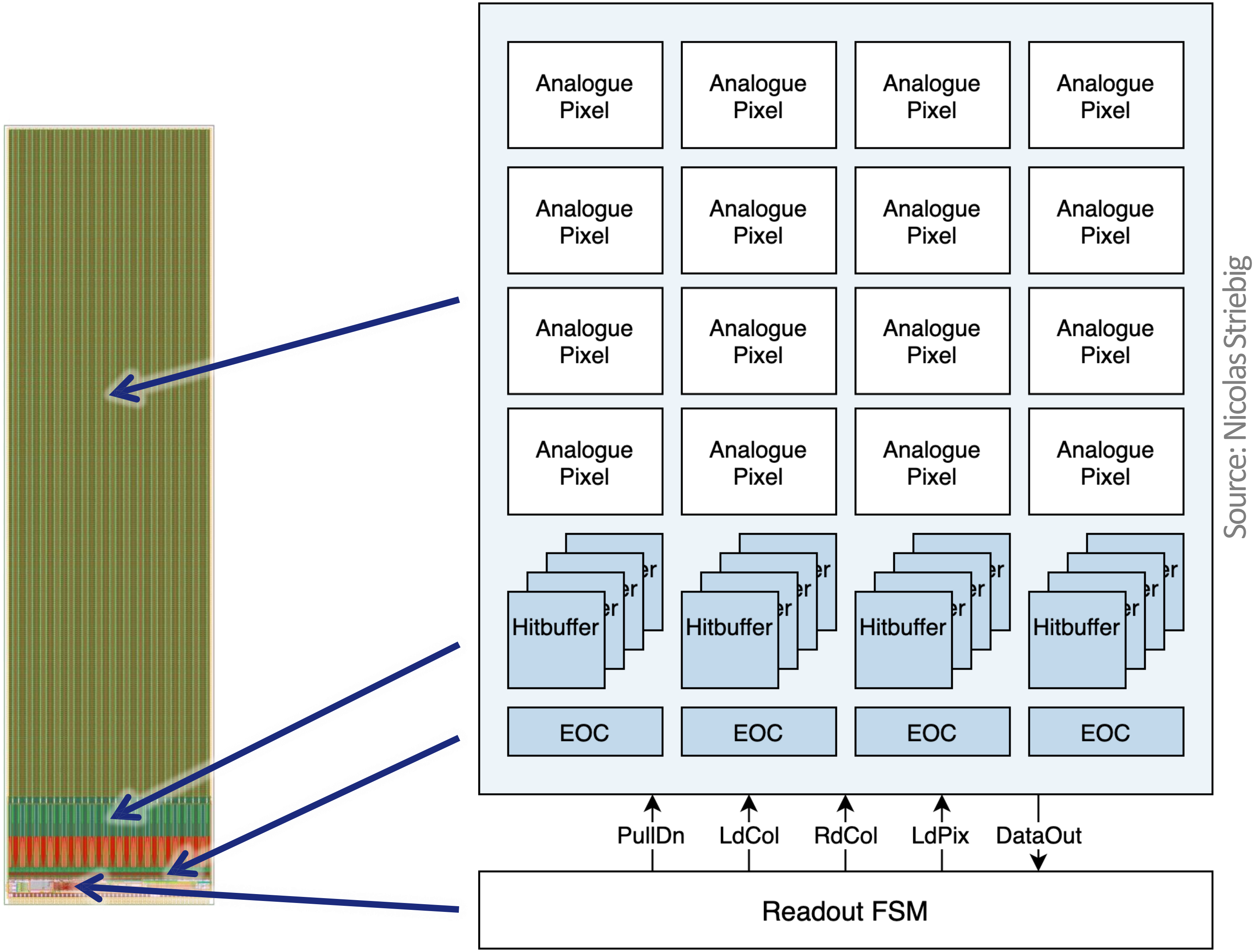


Source: Ivan Perić

MightyPix1

Digital readout

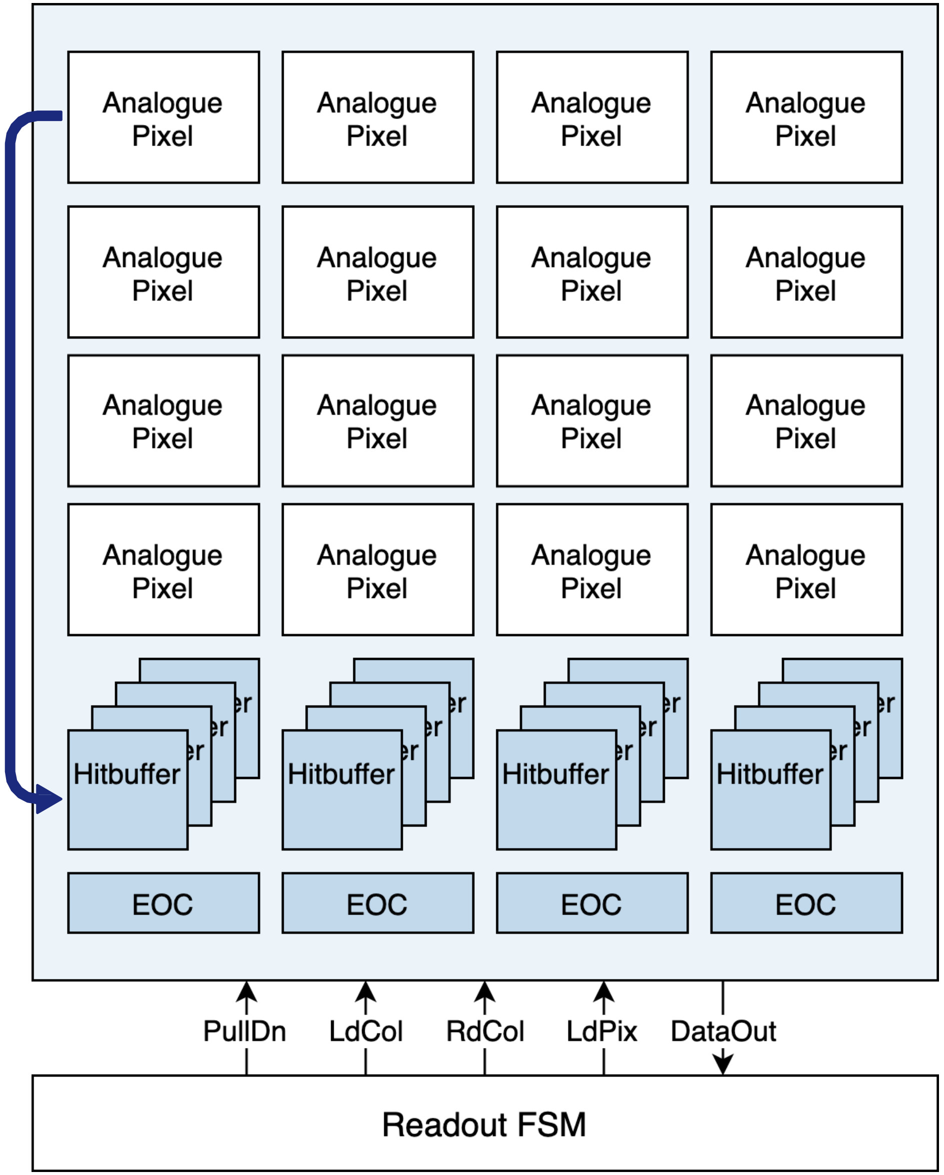
- Readout driven by Readout Control Unit (RCU) Finite State Machine (FSM)



MightyPix1

Digital readout

4. Hit information stored in **hit buffer**
5. Data loaded from highest active hit buffer to End of Column (EoC) buffer
6. Read data from EoC
7. For every hit 2 x 32 bit data words
8. Parallel scrambler analogue to VELOPix
9. Data sent to serialiser tree and sent out



Source: Nicolas Striebig

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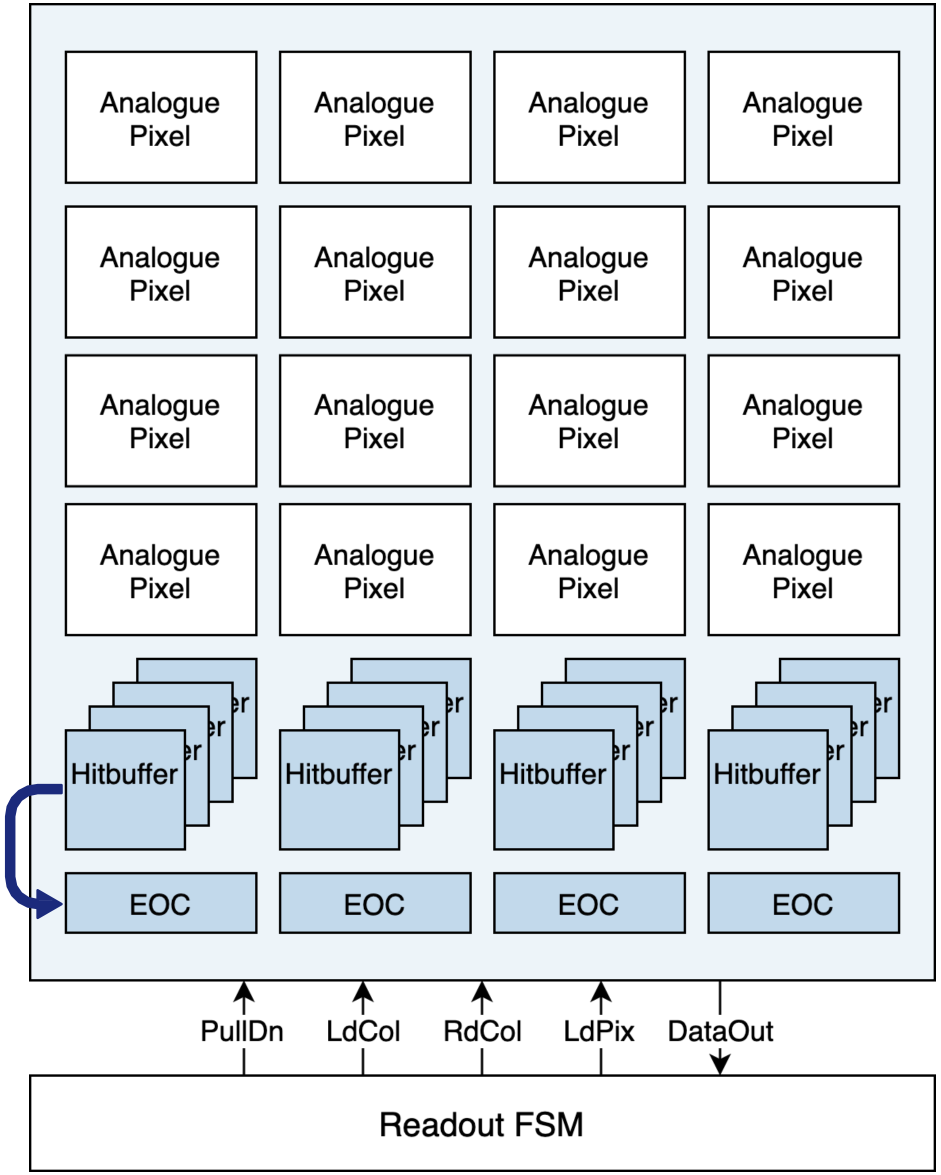

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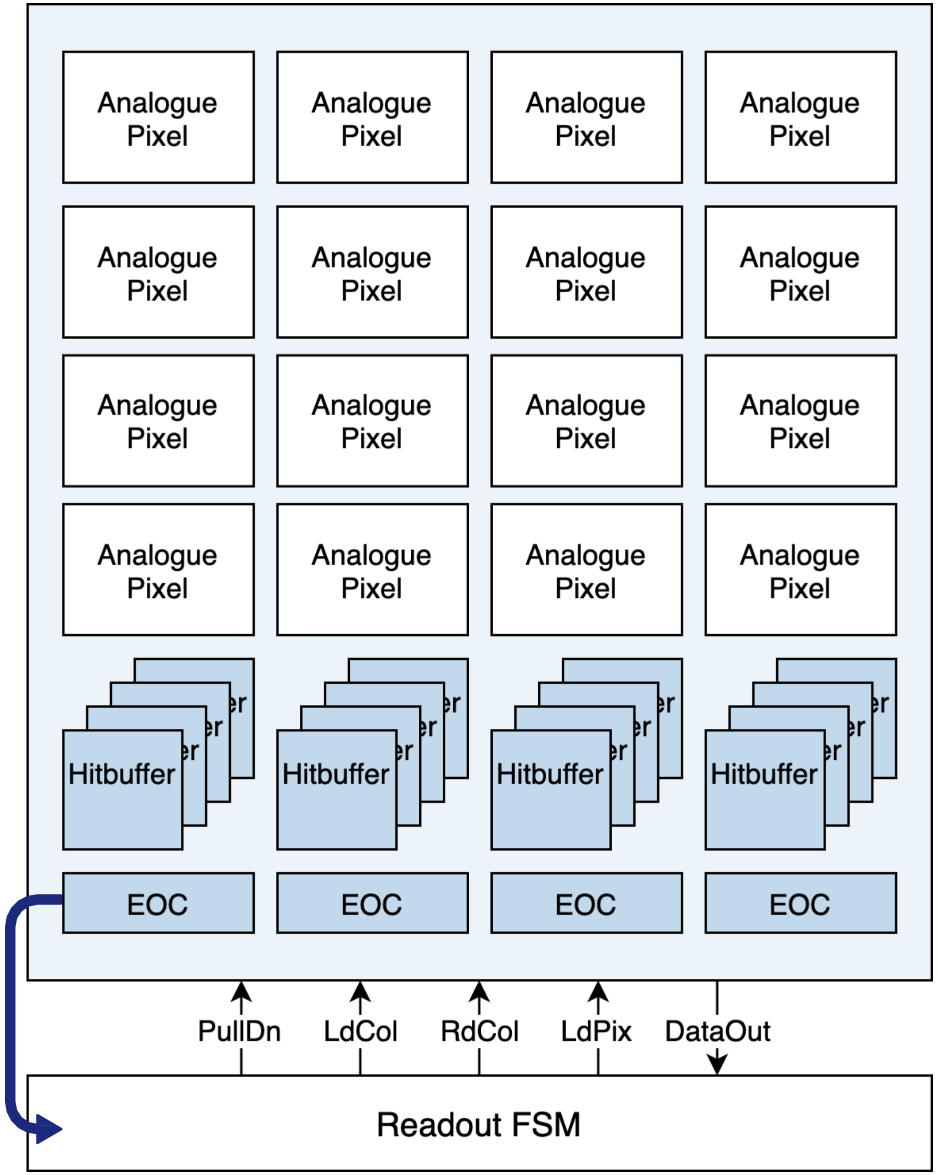

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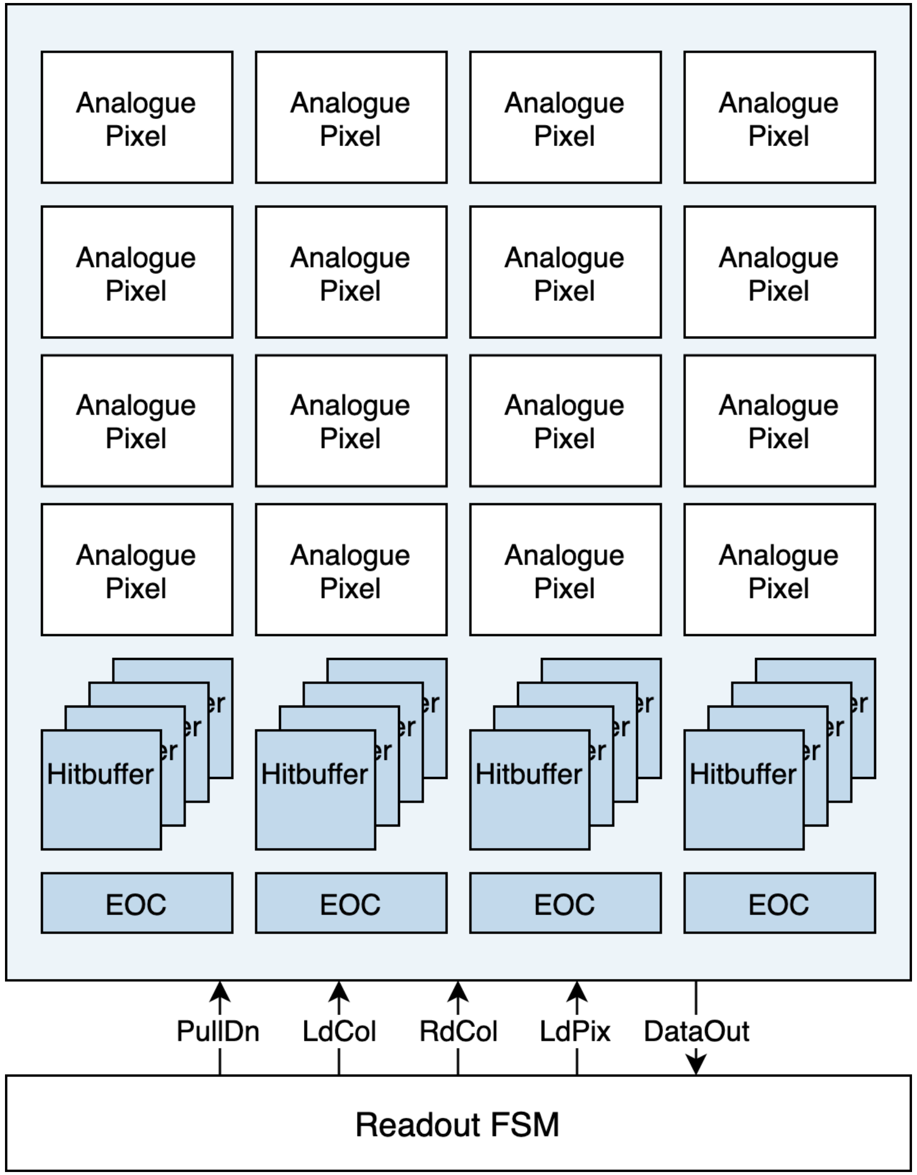

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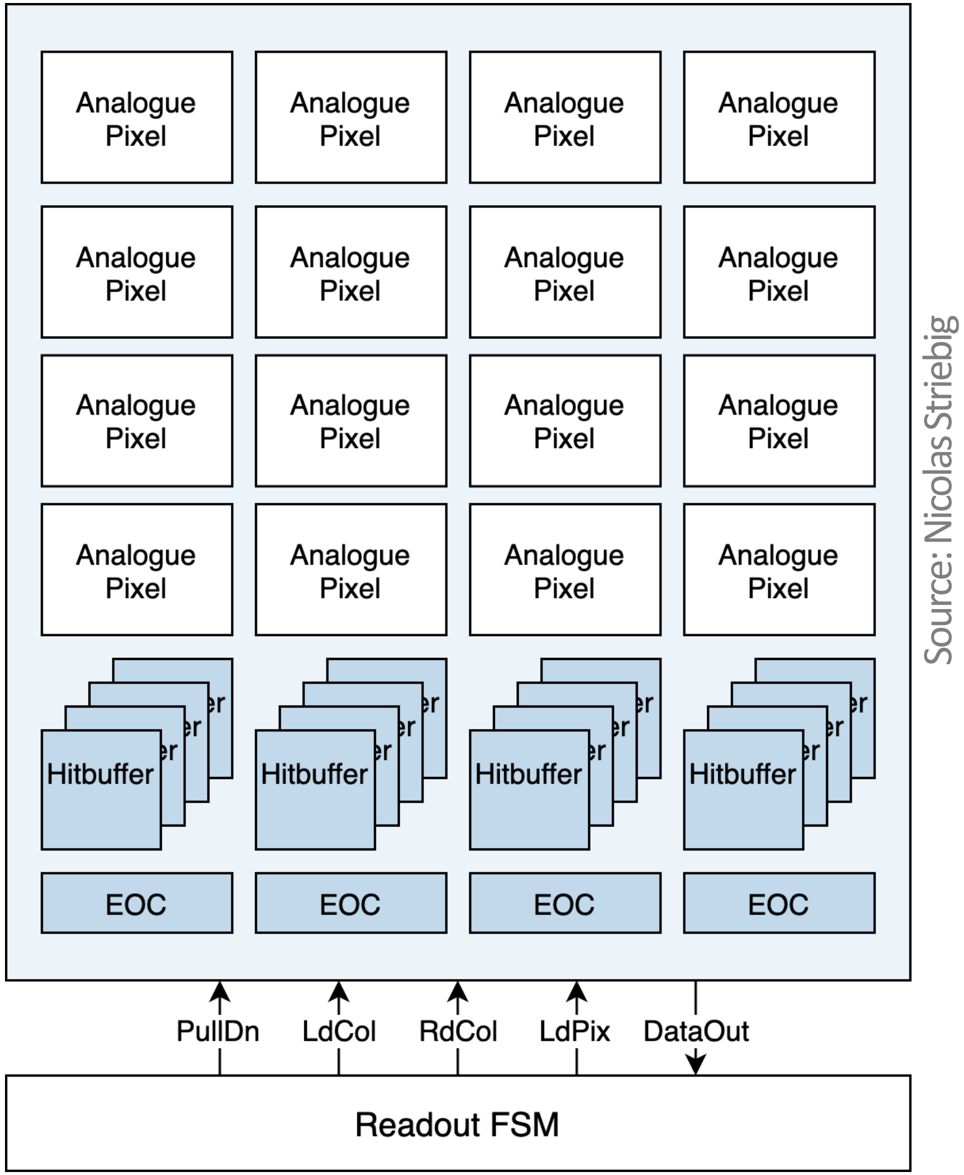

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MightyPix1

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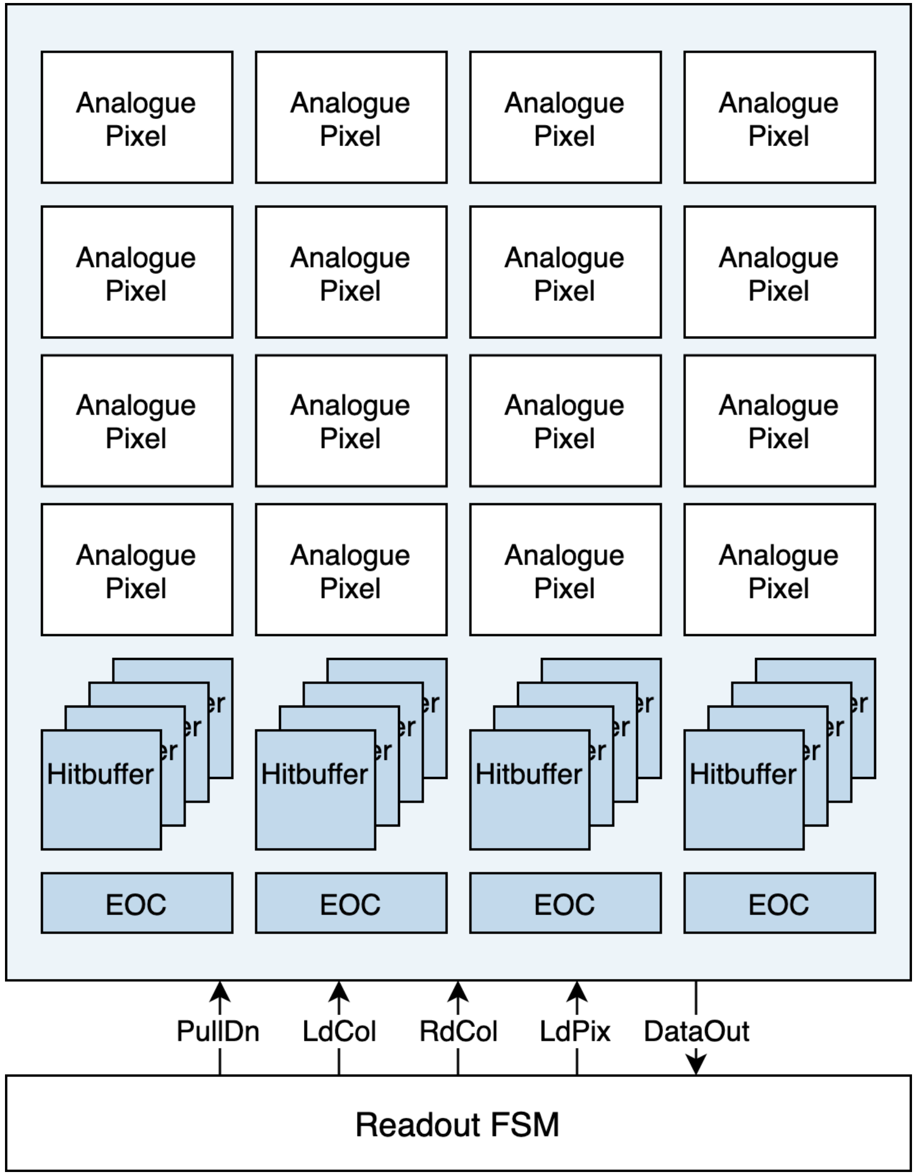
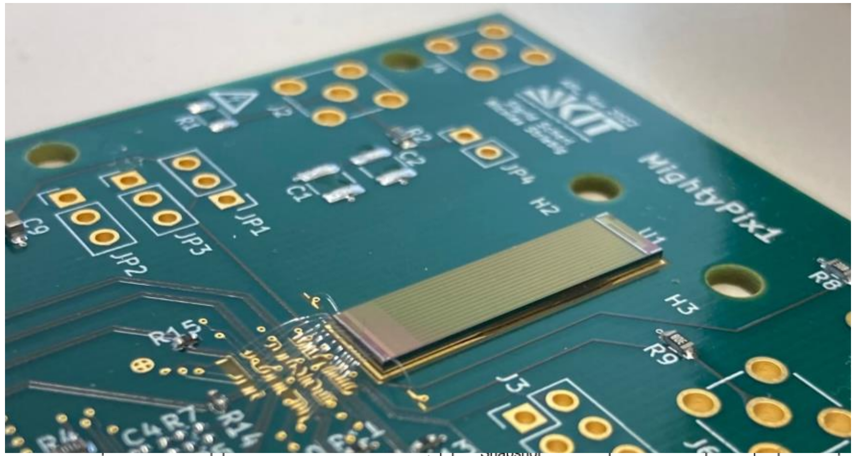


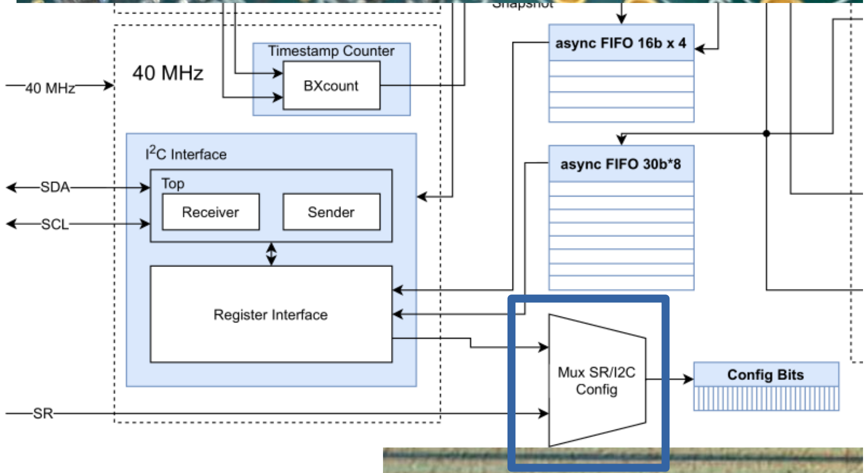
Source: Nicolas Striebig

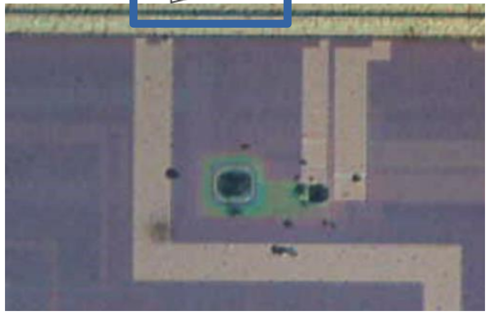
MightyPix1 – Problem and solution

- Design error
  - A load signal for the chip configuration (bias block) was not connected correctly

- Fix idea
  - Do Focused Ion Beam (FIB) to connect the load signal to the appropriate value
  - A few samples have been *repaired*
  - Unfortunately fixed samples have shown no improvement
  - Post-layout simulations, including the bias block with the load signal connected correctly, suggest the chip works ok
  - Currently *repairing* a few more samples with an alternative FIB supplier

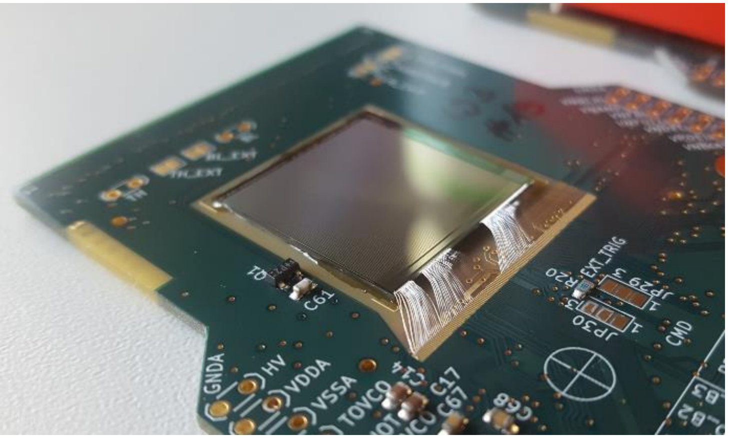




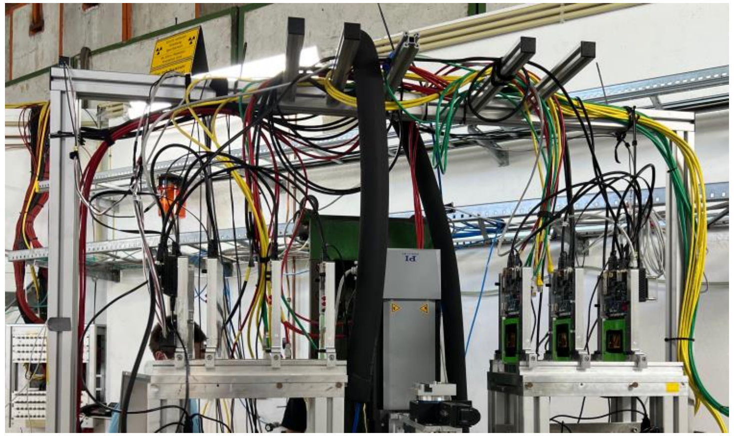


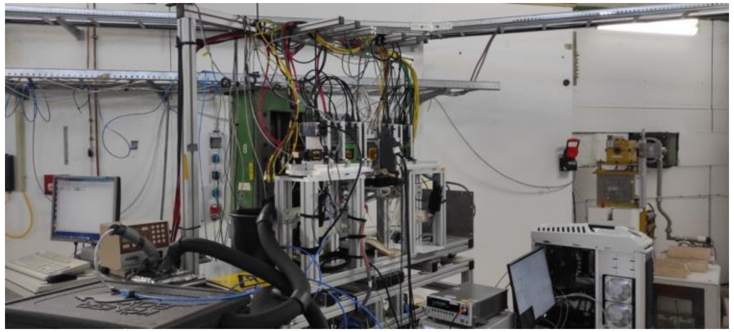
Sensor evaluation

- **ATLASPix3.1**
  - Full-size HV-CMOS pixel chip
  - Very close to MightyPix specifications
  - Analogue front-end is different (amplifier, comparator)
  - Evaluated its radiation tolerance and dependence of time resolution
- **ATLASPix3.1 test beams**
  - DESY (June and December 2022)
  - Non-irradiated chips
  - Irradiated chips up to 3E15 n_{eq}/cm^2
  - At three operating temperatures: -10, 0 and +5 °C
- **TelePix and Run202x chips**
  - Not full-size HV-CMOS pixel chip
  - Same analogue front-end as MightyPix
  - Plan to evaluate them in 2023



Source: Jan Hammerich

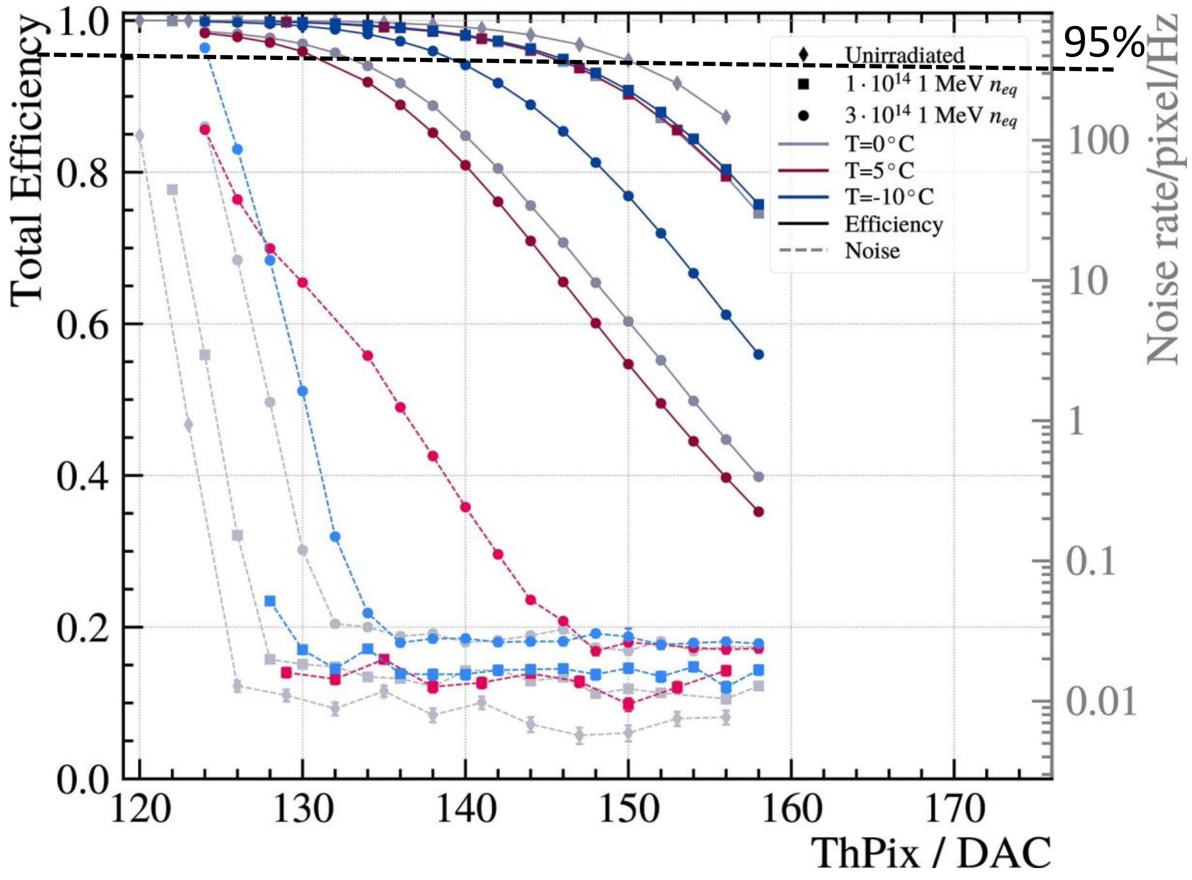




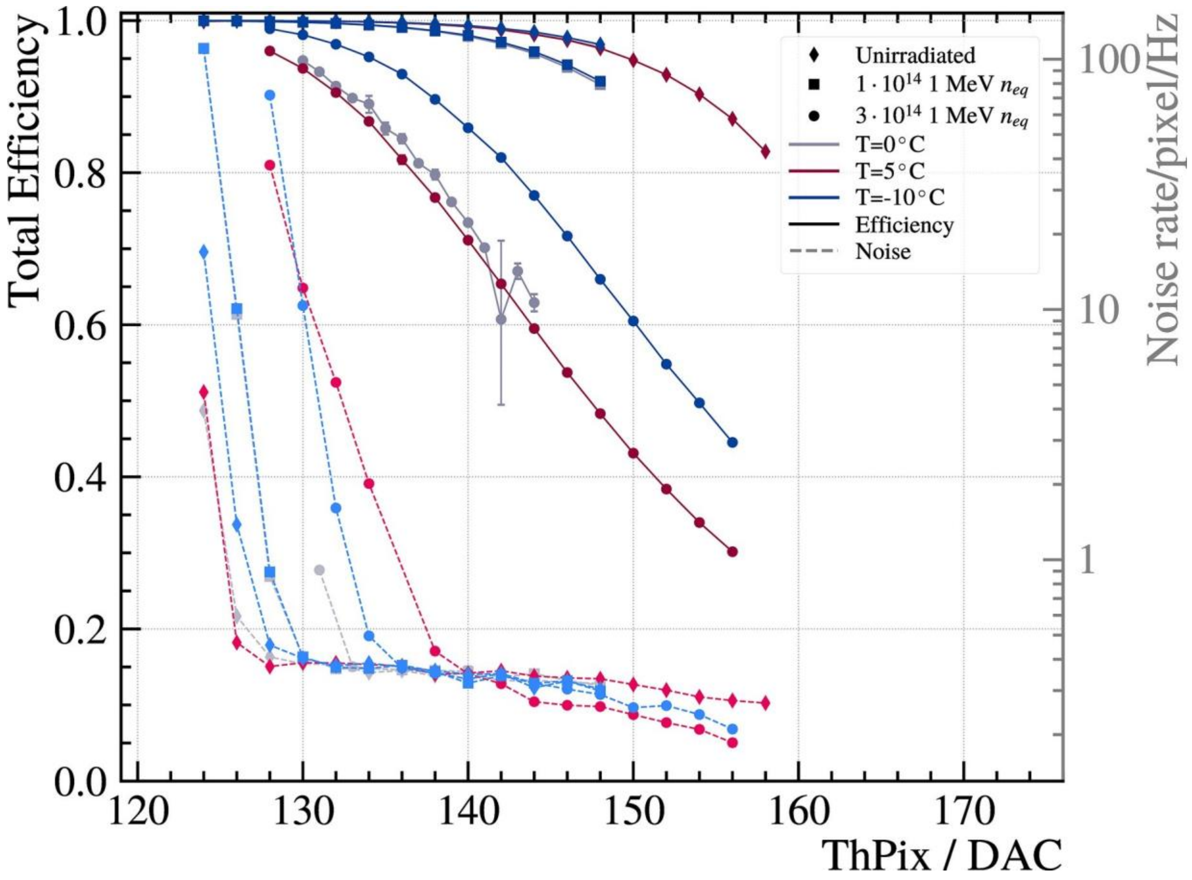
Source: Ryunosuke O'Neil

ATLASPix3.1 – Test beam results

December 2022: with 500 MHz input clock



June 2022: with PLL

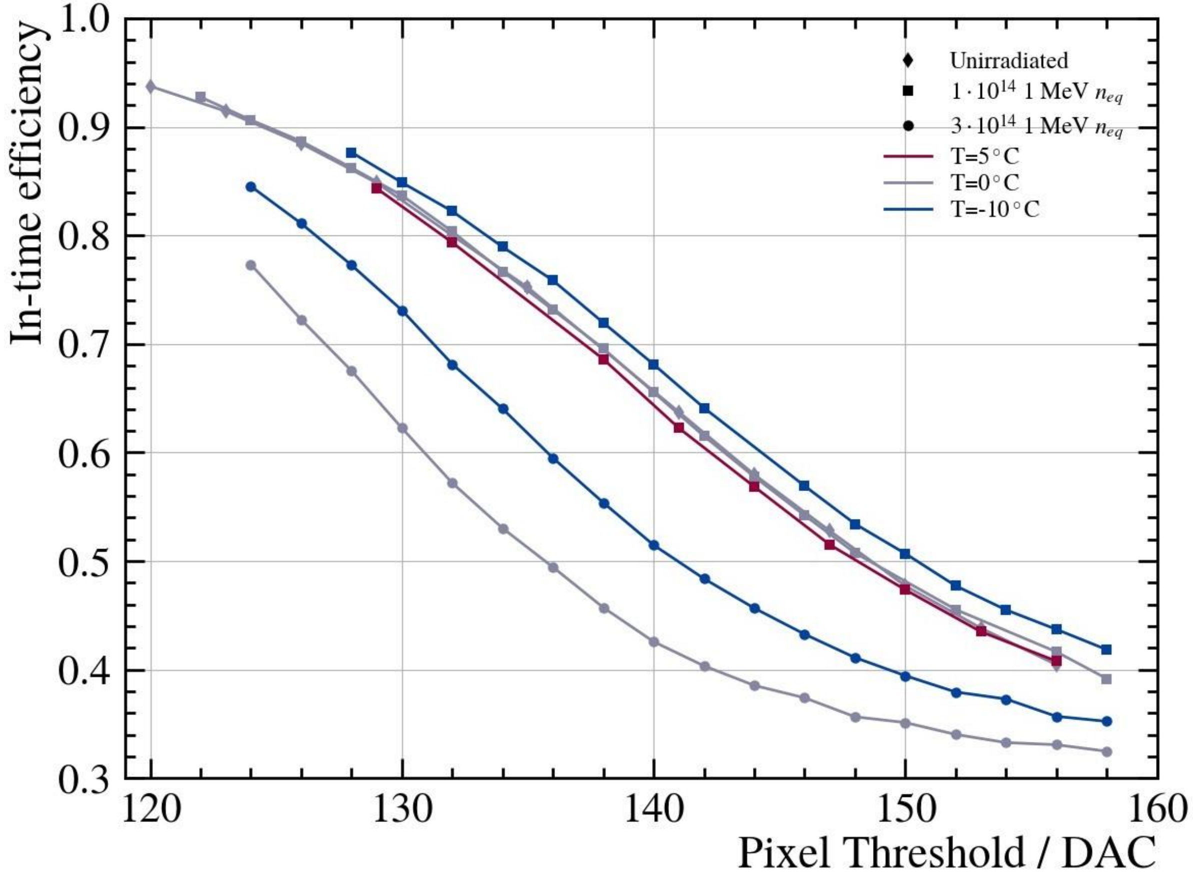


- ATLASPix3.1 shows a short operation range
- Significant decrease in efficiency at 3E14 n_{eq}/cm^2
- External clock improves things, but chip requires cooling

ATLASPix3.1 – Test beam results

In-time efficiency = hit within 25 ns

December 2022: with 500 MHz input clock



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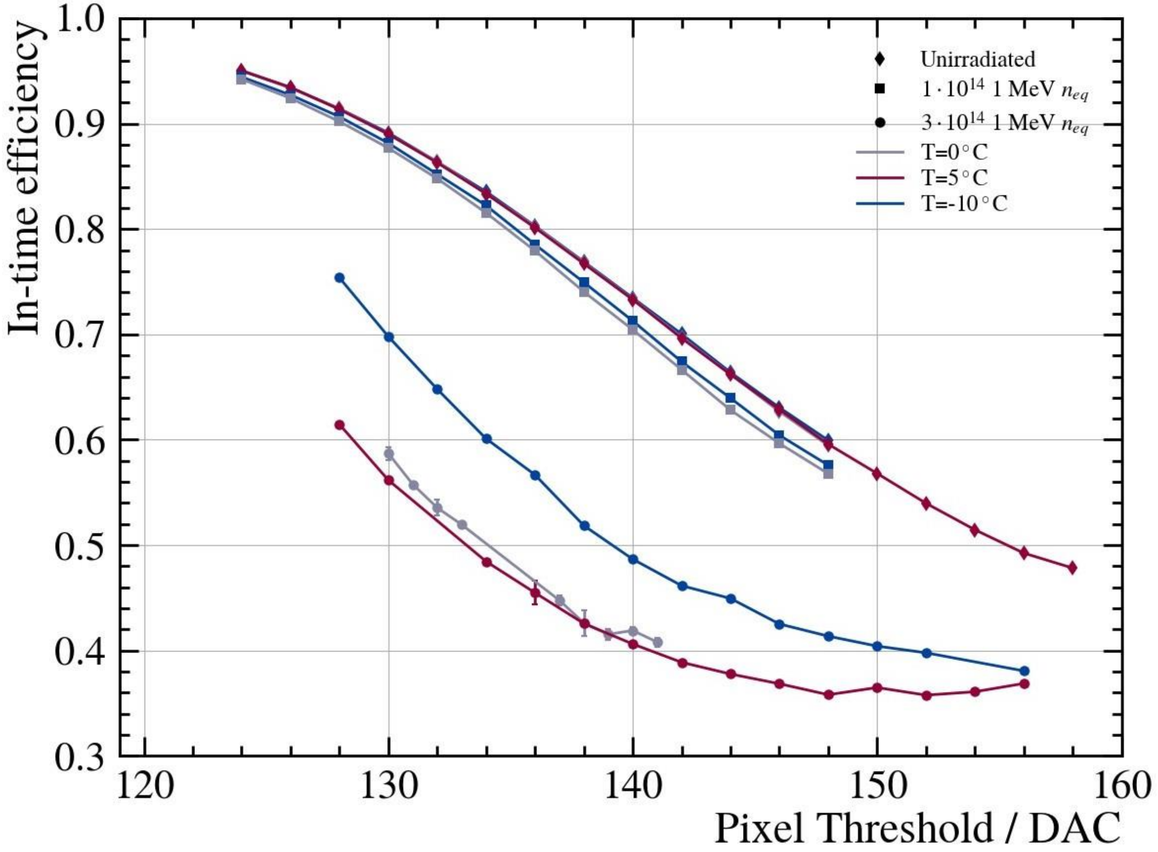

- As expected the time resolution is not good enough (~ 5 ns at best)
- High impact of the radiation for 3E14 MeV n_{eq}/cm^2

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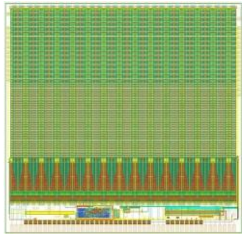
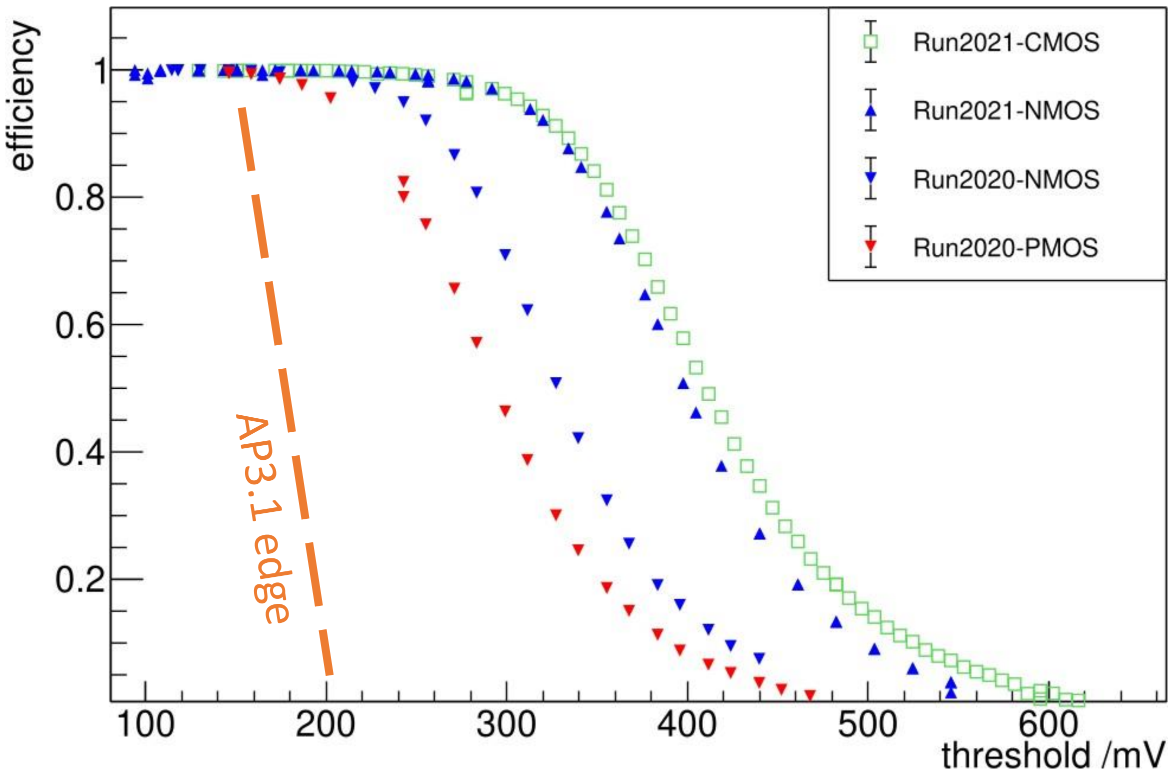
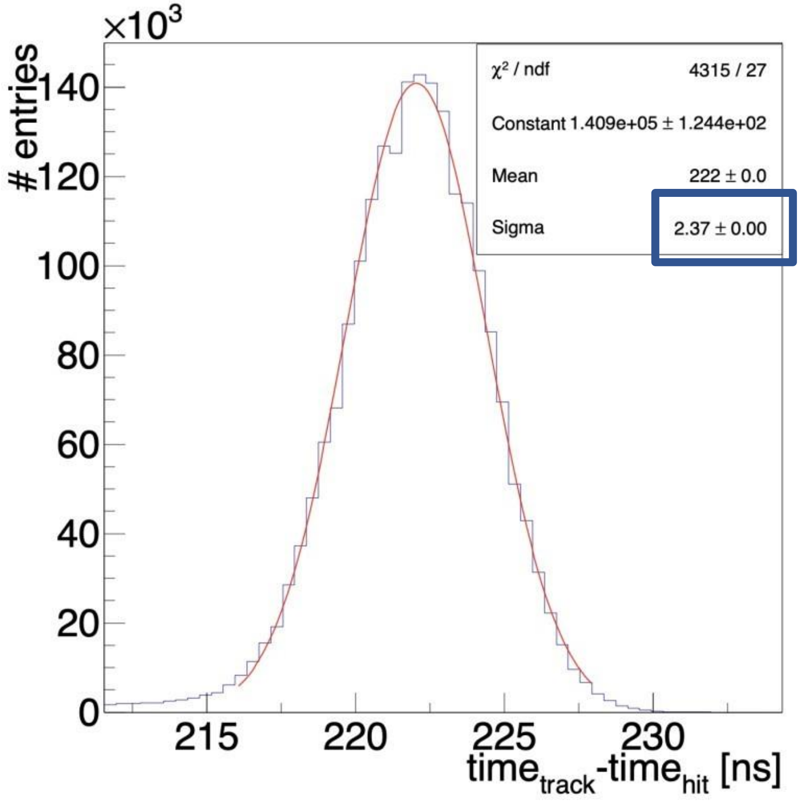
Run202x chips – Test beam results







- Run 2021 has same analogue front-end as MightyPix1 (same amplifier and comparator)
- Half pixel size, and different periphery
- Promising results show the good performance of new analogue front-end

Conclusion and outlook

- **Mighty Tracker is a proposed LHCb upgrade that uses monolithic HV-CMOS sensors**
  - Total silicon area ~ 18 m^2 (minus beam-pipe hole)
- **Dedicated R&D programme to develop an HV-CMOS sensor chip (MightyPix)**
  - Builds on previous designs ATLASPix (ATLAS ITk upgrade) and MuPix (Mu3e)
  - MightyPix1 is first LHCb compatible HV-CMOS sensor chip
  - MightyPix1 fabricated with FIB solution under investigation
  - MightyPix2 design is in progress
- **Currently evaluating other HV-CMOS sensor chips that are available**
  - Radiation tolerance not as expected (several ideas)
  - Timing as expected, but not enough for LHCb
  - Plan to evaluate TelePix and Run2021 chips, which have shown promising results