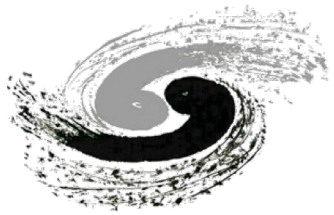
Update on 55nm technology for CEPC Silicon Tracker



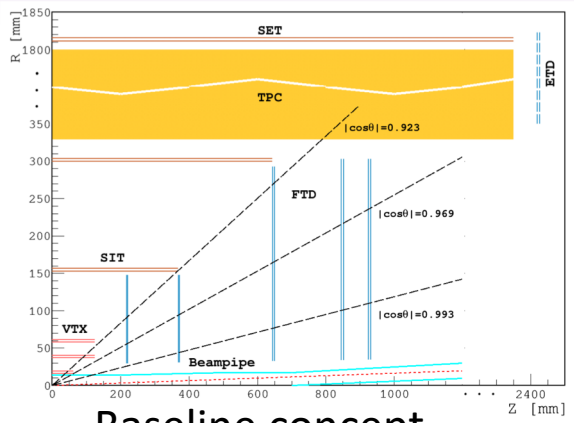
Yiming Li (IHEP, CAS)
On behalf of the CEPC Silicon Tracker team

CEPC Workshop – European Edition @ Edinburgh, 04 Jul 2023

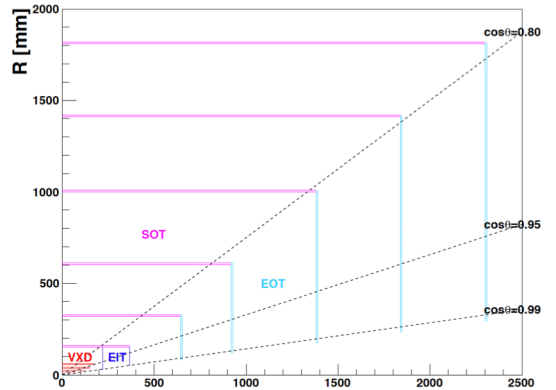
CEPC silicon tracker

- Large area silicon tracker planned
  - ~70 – 140 m^2 depending on detector concept
- Good spatial resolution
- CMOS is a high-performant and cost-effective solution

- Yet more technology options possible compared with vertex detector
  - More tolerant on power consumption (liquid cooling possible)
  - ~10um resolution → increased pixel size



Baseline concept



Full Silicon Tracker

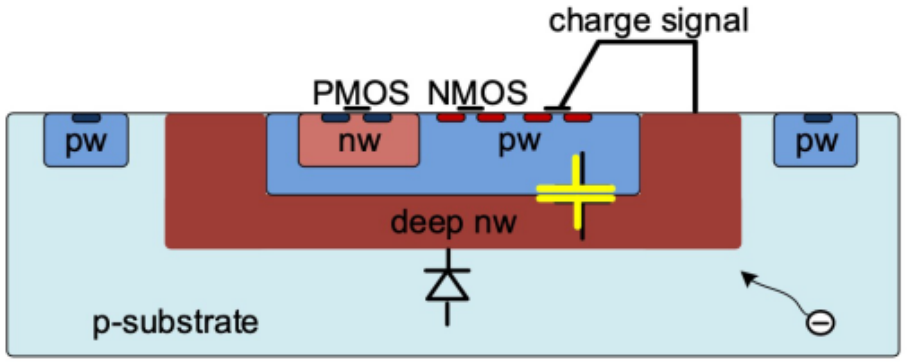
$$\sigma_{1/p_T} = a \oplus \frac{b}{p \sin^{3/2}\theta} \quad [\mathrm{GeV}^{-1}]$$

$a \sim 2 \times 10^{-5}\,\mathrm{GeV}^{-1}$

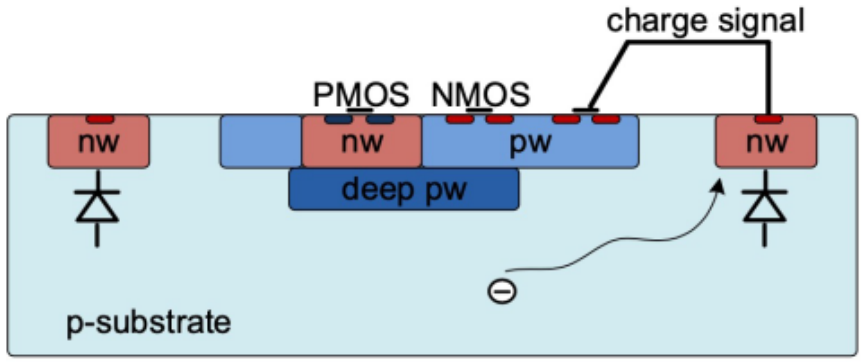
$b \sim 1 \times 10^{-3}$

HVCMOS

- Most CMOS process needs modification to generate sufficient signal
  - Expensive and in most cases not allowed by foundries
- HVCMOS is commercially available process
  - Intrinsically radiation hard
  - Large capacitance → potentially more noise and power
  - Hard for vertex detector but no showstopper for tracker



High Voltage CMOS

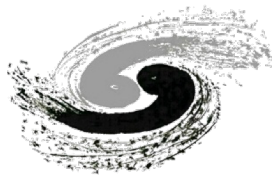


CMOS with small electrode

Towards smaller feature size

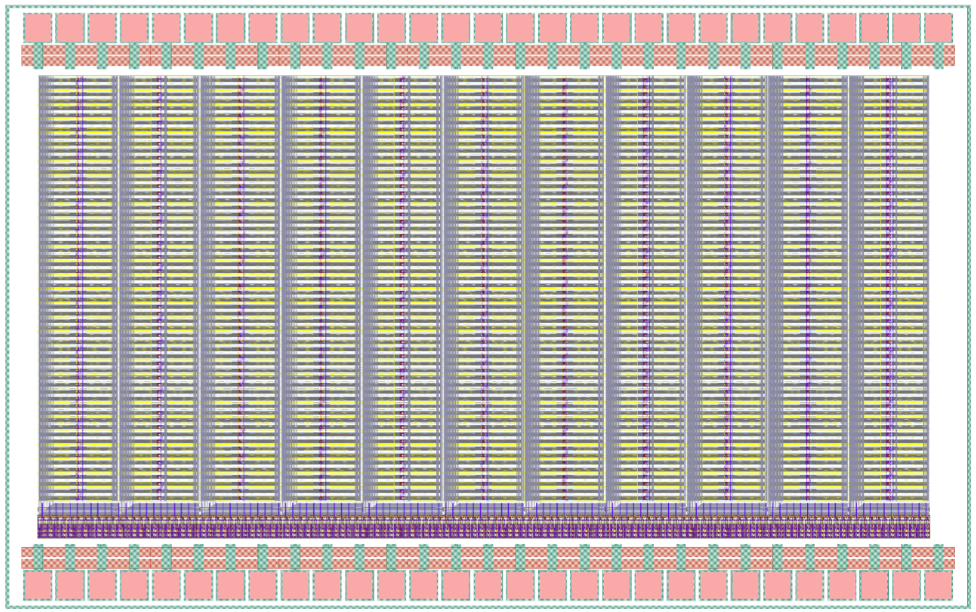
- Main-stream HVCMOS in (HEP) market:
  - AMS/TSI 180nm process: MuPix, ATLASPix, TelePix, MightyPix,⋯
  - LFoundry 150nm process: LF-Monopix, RD50-MPW, ⋯
- Migration into smaller feature size is generally onging process
  - For ASIC design CERN has launched 65nm validation campaign with many European partners, attempts with 28nm also started

- Efforts formed in search of HVCMOS process with 55/65 nm process provided by an alternative foundry
  - Attempts with HLMC 55nm: seeking MPW
  - SMIC 55nm (non-HV): MPW in Oct 2022
  - SMIC 55nm HV: MPW planned in Aug 2023




HLMC

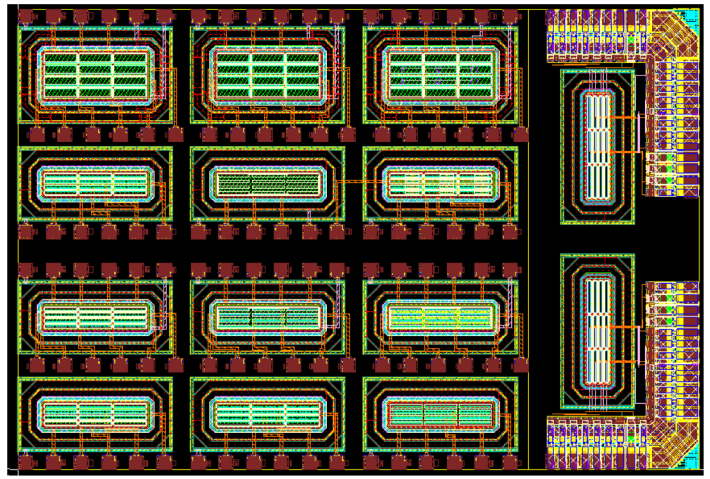
- HLMC 55nm HV process
  - Seeking MPW opportunity with input (pixel-matrix design) from KIT + IHEP
  - Could not catch the 2021 MPW and 2022 MPW was cancelled by foundry
  - Caveat: wafer with high-resistance substrate not yet supported

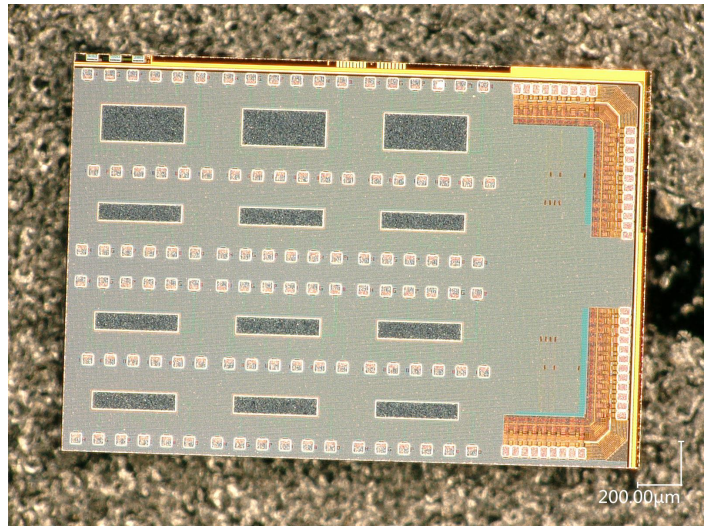


Ivan Peric et al

SMIC 55nm MPW in 2022

- MPW submitted in Oct 2022 with SMIC 55nm Low Leakage process
  - NB: not an HV process! Yet it has similar deep N well separating the transistors and the sensor part
  - 3 × 2 mm^2 in area
  - Variation of passive diode arrays
  - Simple amplifiers added
- 40 chips received in end Apr 2023
  - Tests going on now

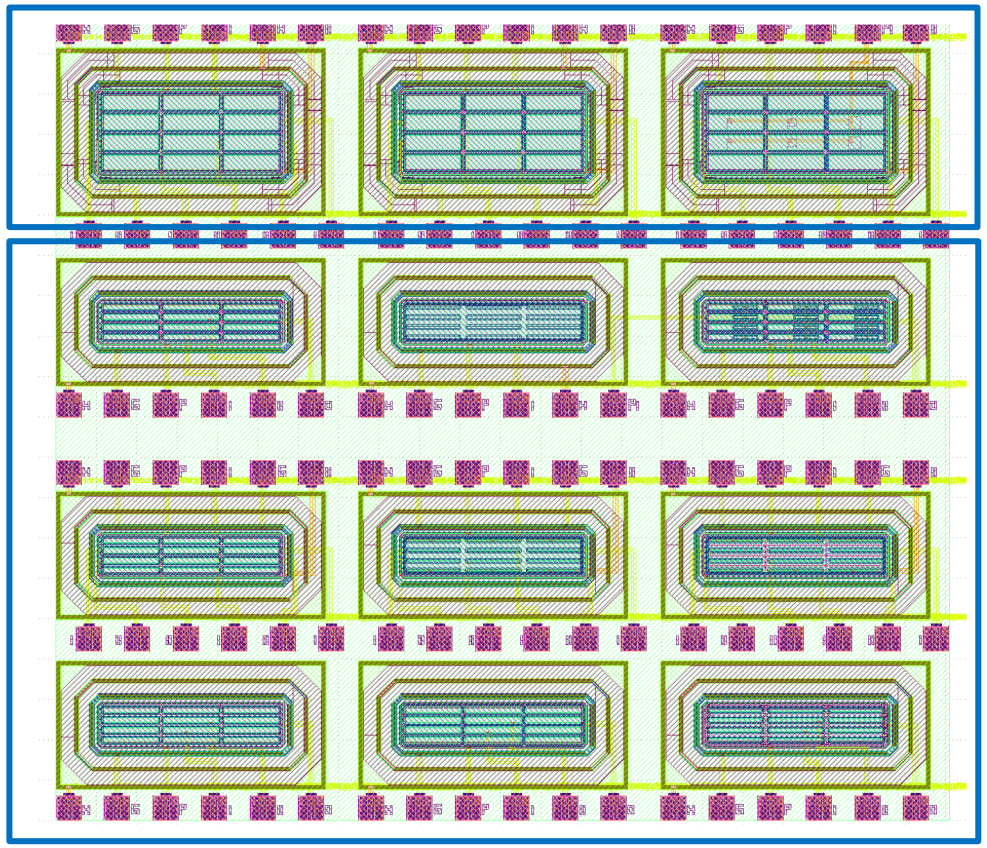




Passive sensor arrays

- NB: no HR substrate
  - Limited charge generation
- 12 layout design
- Pixel size：
  - 25x150um^2, 50x150um^2
- Pixel array： 3x4
  - For charge sharing study
- Different design:
  - With/without P stop between pixels:
  - Space between pixels: 5um, 10um, 15um
  - Connection method
  - Pwell area in Dnwell:
    - Capacitance affect

Pixel size:50x150um



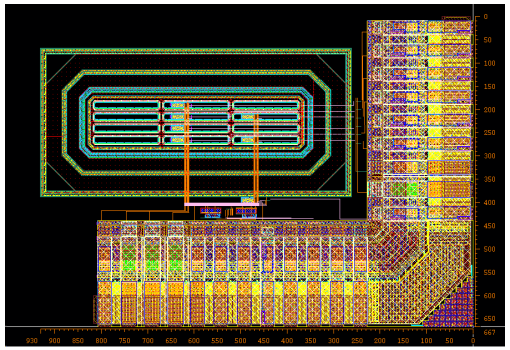
Pixel size:25x150um

Mei Zhao

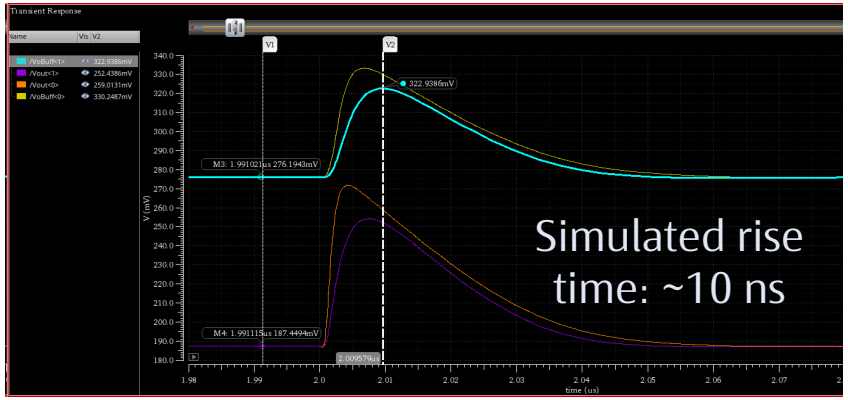
Schematic

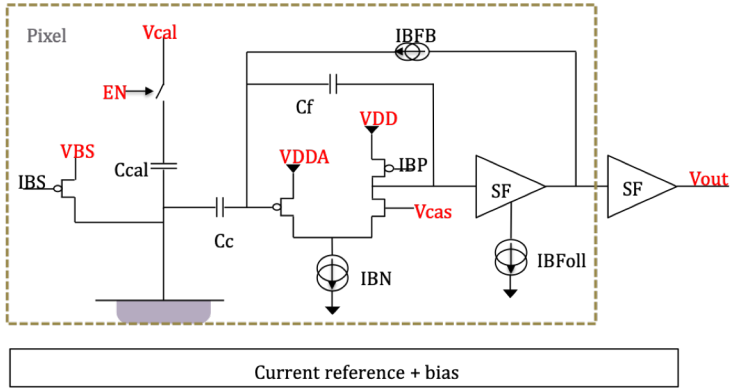
- Sensor biased with active resistor
- Calibration capacitor integrated
- Charge Sensitive Amplifier structure
  - Two power supplies
  - Folded cascode amplification stage
  - Constant feedback current
- Two stage source follower used to drive the signal out

Weiguo Lu



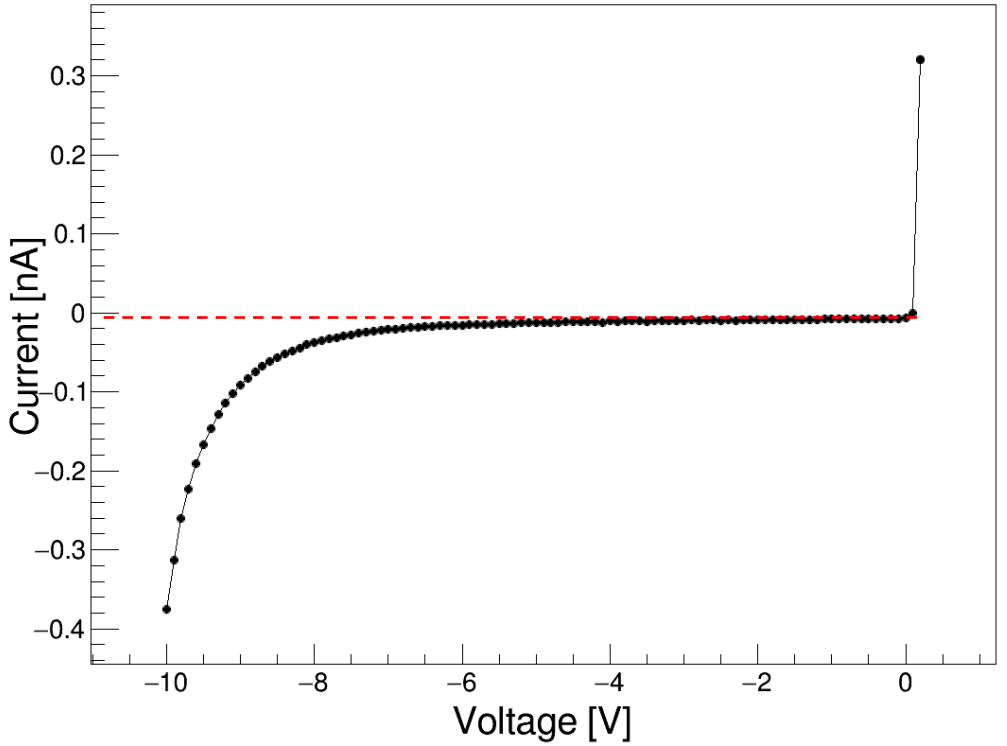
6 channels AC
coupled to sensors





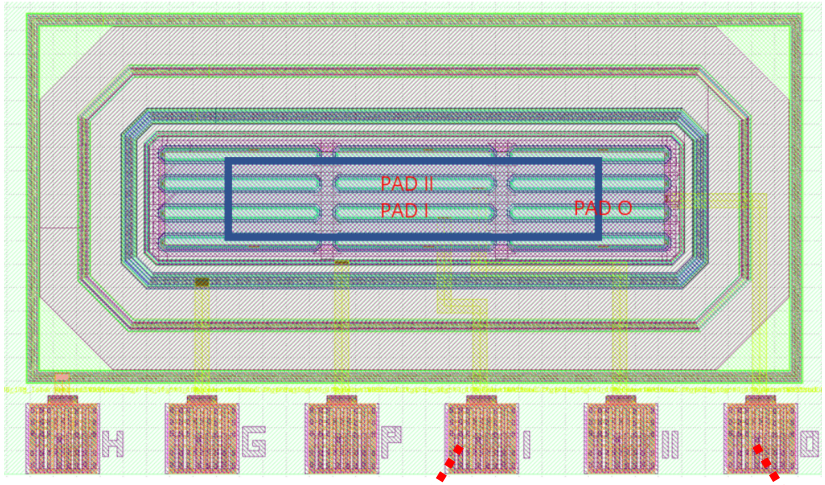
A typical IV

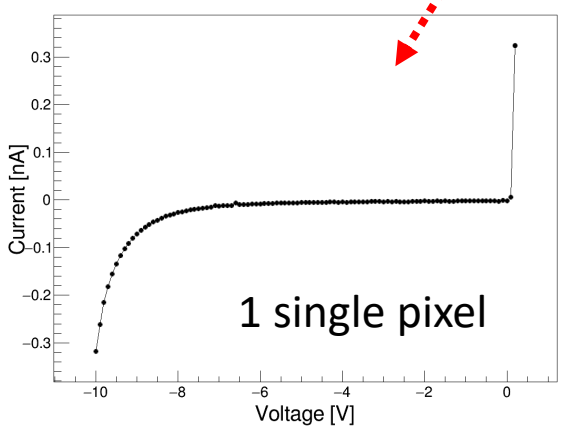
- IV test shows good diode-behavior for all sectors in bias range from -10V to +0.2V :
  - Clear positive conduction
  - Reverse breakdown occurs beyond -8V
  - Leakage is small ~ 10 pA

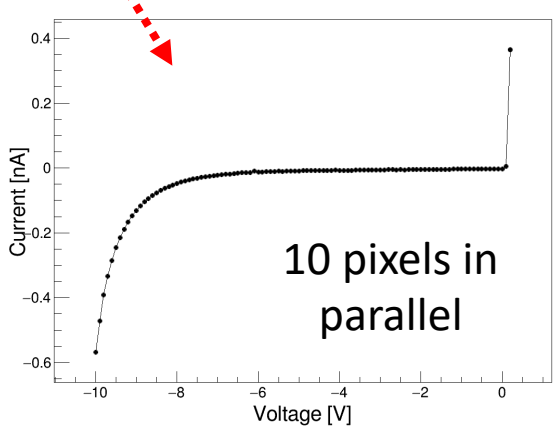


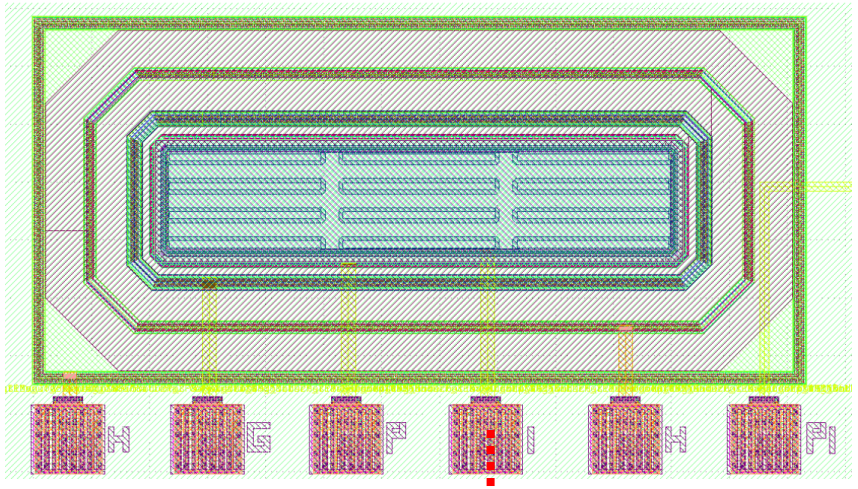
Zhiyu Xiang, Xiaoyu Zhu, Zijun Xu, YL

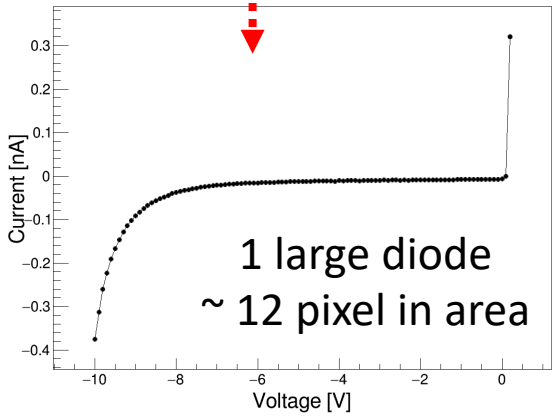
More IV for different diode design







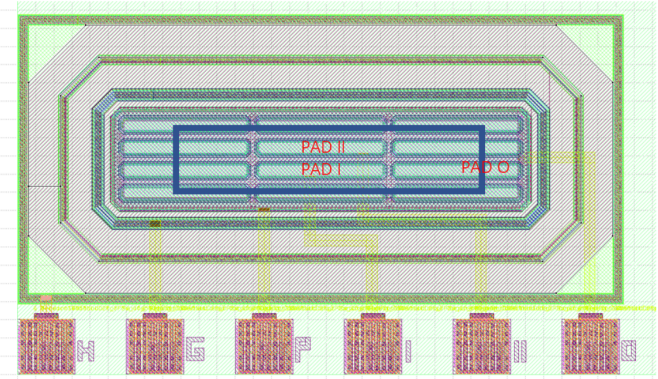


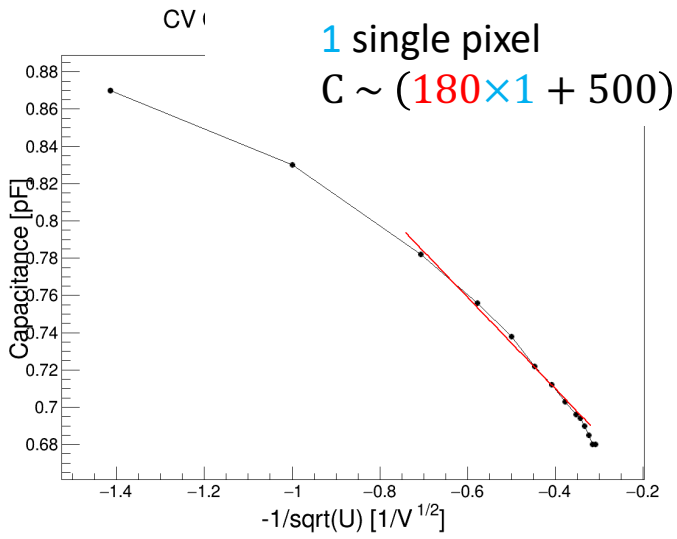


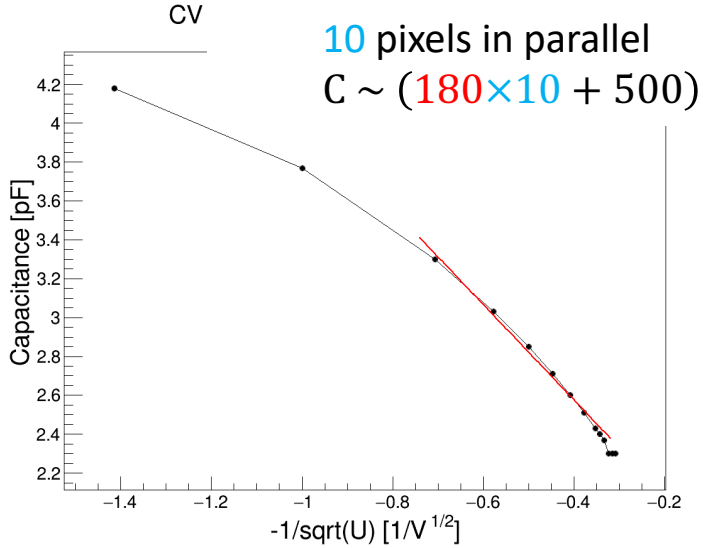
Pixel size: 25 x 150 um^2

CV measurement

- CV test results are comparable for different diode design:
  - Full depletion reached close to ~ −8V
  - Proportional to the sensor area
  - Capacitance of a single small pixel: 100~200 fF as expected
  - External capacitance from system is around 500 fF

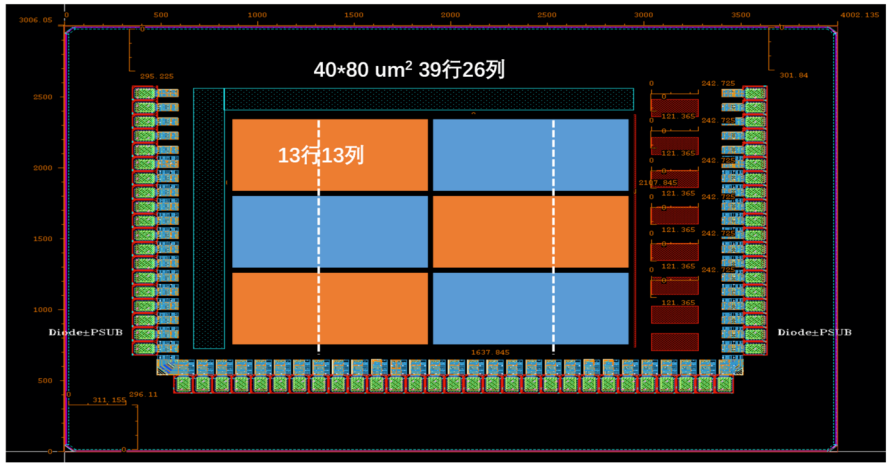






MPW plan

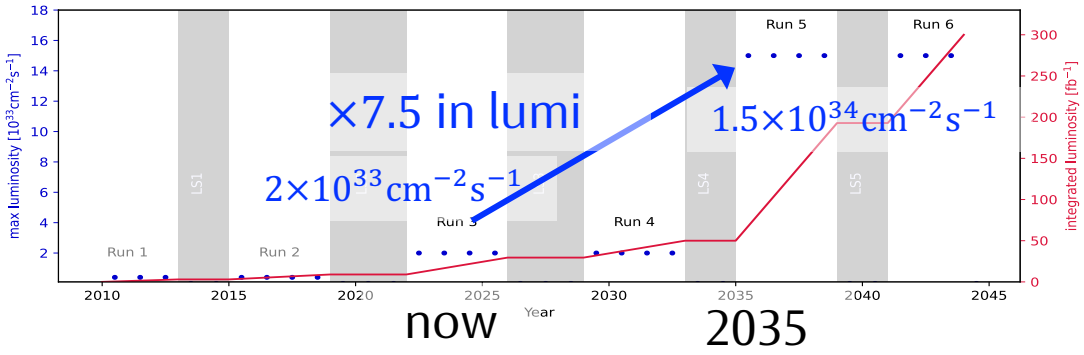
- MPW is planned with SMIC HV 55nm in Aug 2023
  - High-res wafer of 1k or 2k Ωcm available
  - Will be real validation of the sensor
- Design ongoing for:
  - Variation of diode structures
  - Analog amplifier and switch circuit
  - Test structure for small digital circuit

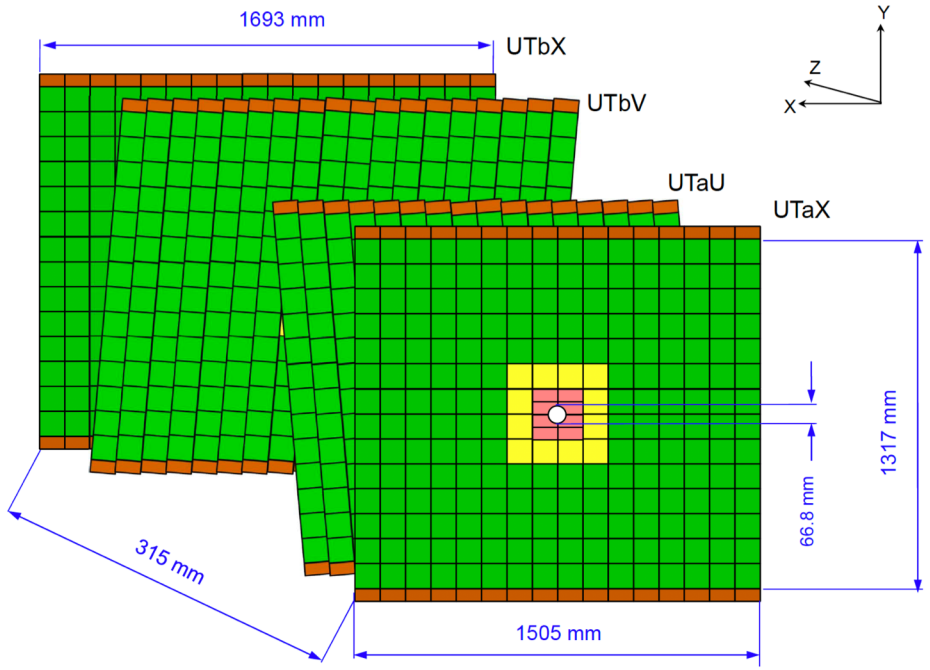


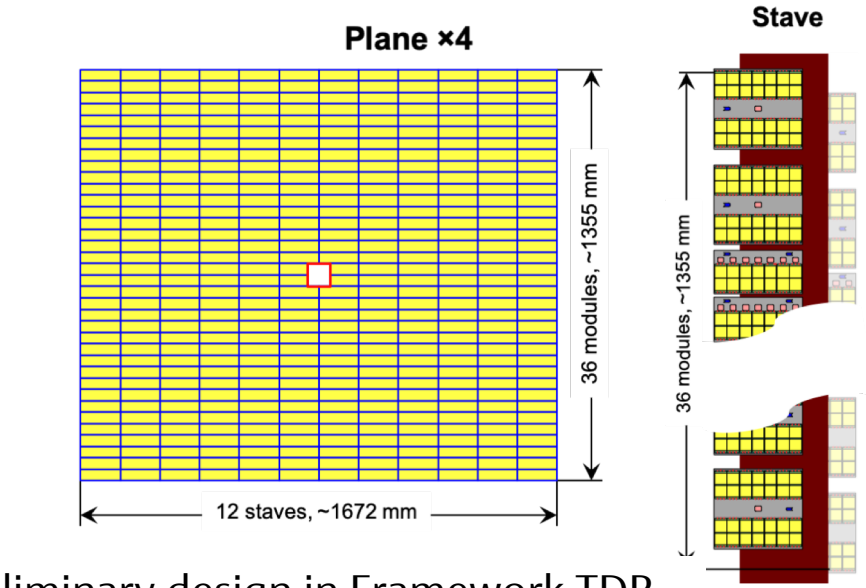
注：仅作为资源利用参考，不代表最终结构

Synergy with LHCb Upgrade II

- LHCb Upgrade II planned in LS4 to enable luminosity increase by a factor of 7.5
- Silicon-strip-based Upstream Tracker will be replaced with a pixel detector with higher granularity and better radiation hardness
- HVCMOS is a promising technology option







Preliminary design in Framework TDR based on ATLASPix-like sensors

Conclusion

- HVCMOS is a promising technology for CEPC silicon tracker
- Search for alternative foundry of smaller feature size for the technical benefit and for risk reduction
- First results from 2022 MPW seems promising
- Preparation for MPW with 55nm HV process is ongoing