中国科学院高能物理研究所
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Status of R&D on the SOI-3D technology for CEPC vertex detector

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Outline

- Introduction
  - Pixel sensor specifications drives by the CEPC vertex detector
  - Motivations of using SOI-3D process
- Design of the CPV-4
  - SOI and 3D process
  - Development of the serial SOI pixel sensors in IHEP
  - Architecture of CPV-4
- Electrical test results
  - Before 3D-integration
  - After 3D-integration
- Summary Outlooks & Acknowledgements

Pixel sensor design specifications derives by the CEPC vertex detector

- Impact parameter resolution $\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\sin^{3/2}\theta} (\mu m)$
- Low occupancy < 1%
- Low material budget 0.15%/ X_0/layer

First detector layer at different colliding modes

Operation mode	H (240)	W(160)	Z (91)
Hit density (hits · cm^{-2} · BX^{-1})	2.4	2.3	0.25
Bunching spacing (μs)	0.68	0.21	0.025
Occupancy (%) (at 10 us)	0.08	0.25	0.23

Baseline design parameters

	R(mm)	| Z |(mm)	$\sigma(\mu m)$	material budget
Layer 1	16	62.5	2.8	$0.15\%/X_0$
Layer 2	18	62.5	6	$0.15\%/X_0$
Layer 3	37	125.0	4	$0.15\%/X_0$
Layer 4	39	125.0	4	$0.15\%/X_0$
Layer 5	58	125.0	4	$0.15\%/X_0$
Layer 6	60	125.0	4	$0.15\%/X_0$

Physics driven requirements	Running constraints	Sensor specifications
$\sigma_{s.p.}$ 2.8um		Small pixel ~16 μm
Material budget 0.15% X_0/layer		Thinning to 50 μm
	Air cooling	low power 50 mW/cm^2
r of Inner most layer 16mm	beam-related background	fast readout ~1 μs
	radiation damage	radiation tolerance ≤3.4 Mrad/ year, ≤$6.2\times10^{12} n_{eq}$/ (cm^2 year)

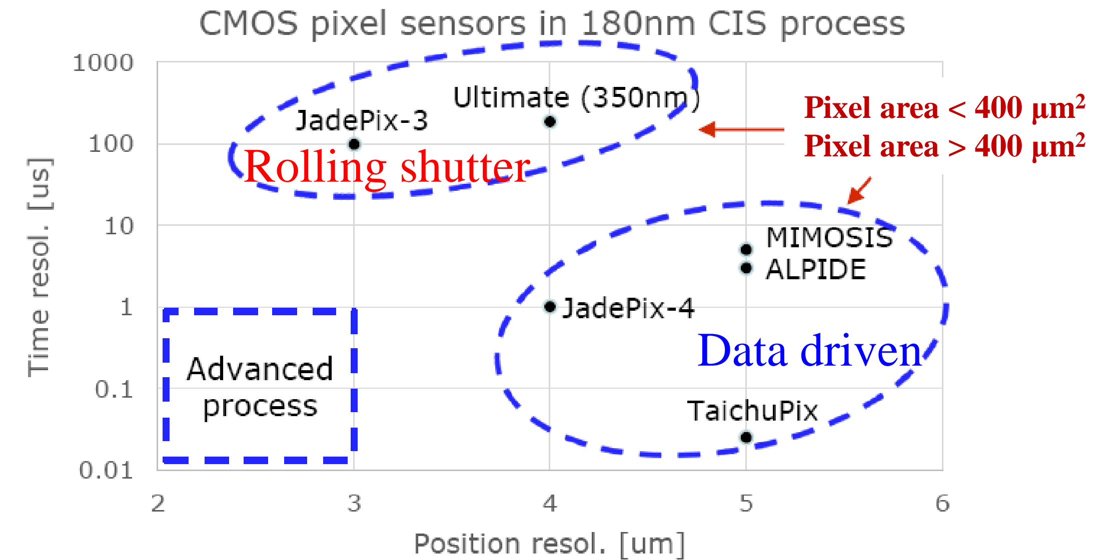
Pixel design: **contradictory** optimize direction

Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector, http://cepc.ihep.ac.cn/

Motivation of using SOI-3D process: Position resolution & Time resolution

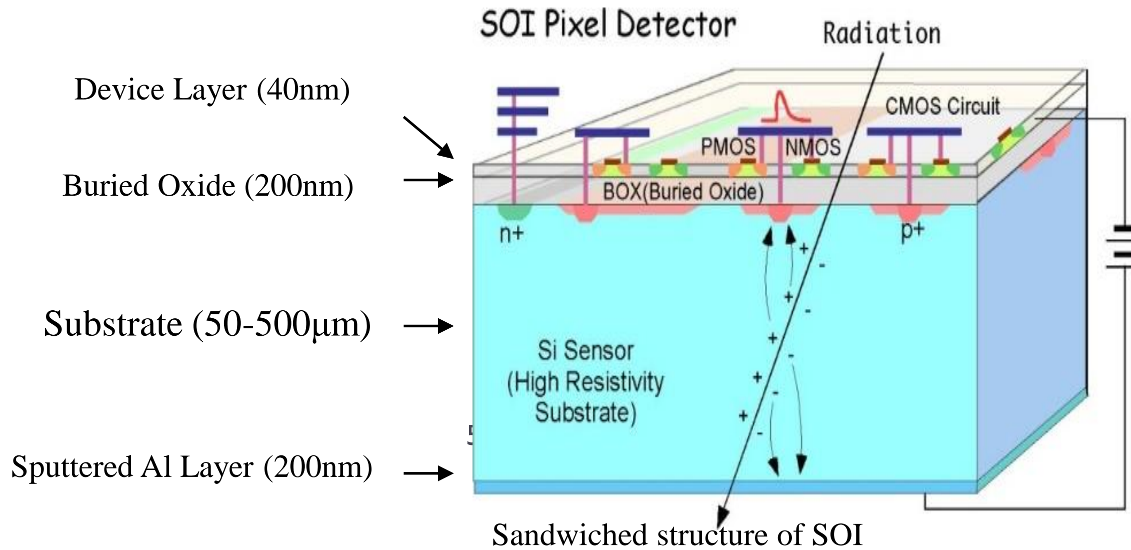
Some performances of MAPS for vertex detector

Name	Pixel size [um²]	Position Resol. [um]	Time Resol. [us]	Readout scheme	Pixel area
MIMOSIS	26.88x30.24	5	5	Data driving	812
ALPIDE	28x28	5	3	Data driving	784
TaichuPix	25x25	5	0.025	Data driving	625
JadePix4	20X29	4	1	Data driving	580
Ultimate	20.7x20.7	4	186	Rolling shutter	428
JadePix3	16x23.11	3	98.3	Rolling shuter	370



- More advanced process or new techniques to accommodate **more transistors (more functionalities)** within a pixel area < 400 μm² (e.g. 16×25)
  - 65nm CIS process
  - **200nm SOI + 3D integration**

SOI Pixel Detector



Sandwiched structure of SOI

SOI: Silicon-on-Insulator technology

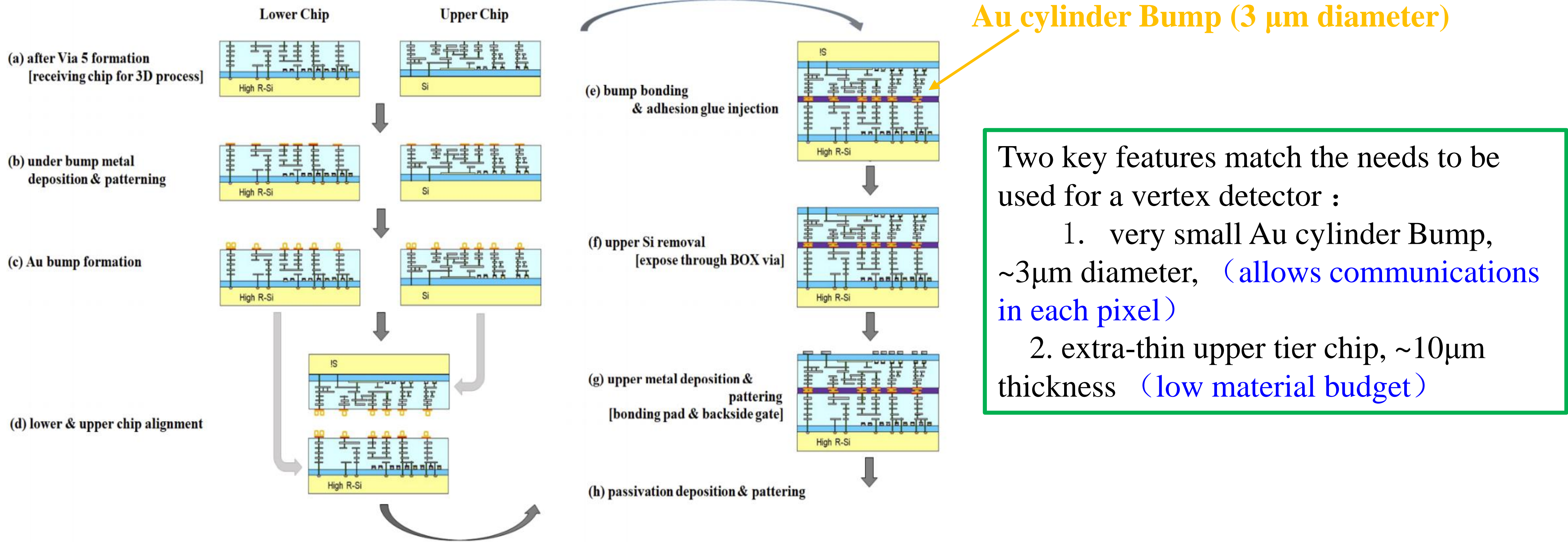
- Utilize 0.2μm FD-SOI CMOS process by lapis Semiconductor Co. Ltd.

SOI pixel detector: monolithic type detector

- **High resistivity** （>1 kΩ·cm）， **thick** (50-500 μm) **sensitive layer**; *more signal charges, low material budget possible;*
- **Fully depleted** (high basing voltage > 100V possible); *fast collection*
- **Low power dissipation**
- **Almost no single event effects (SEE) probability**; *radiation tolerance*
- **Low cost**

A promising candidate to be used in high energy particle detection

3D technique compatible with existing SOI pixel sensor process



Two key features match the needs to be used for a vertex detector：

1. very small Au cylinder Bump, ~3µm diameter, （allows communications in each pixel）
2. extra-thin upper tier chip, ~10µm thickness （low material budget）

SOI-3D process step by step

*@*Ikuo Kurachi，et all, Oct.7, Vertex 2020*

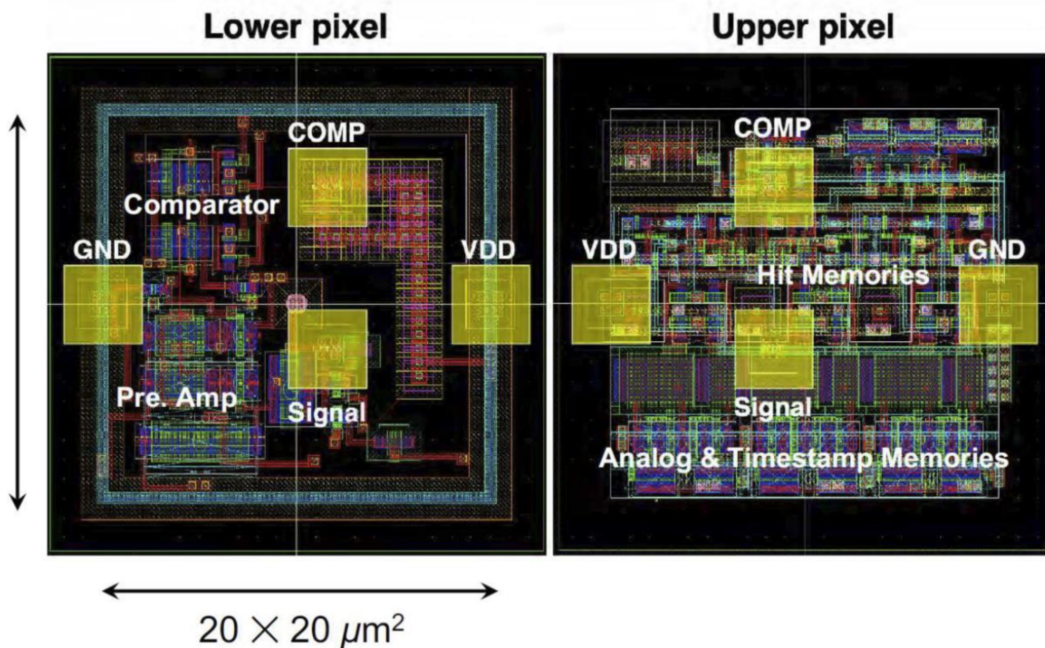
Tape-out at LAPIS, Chip-On-Chip 3D-bonding at T-Micro

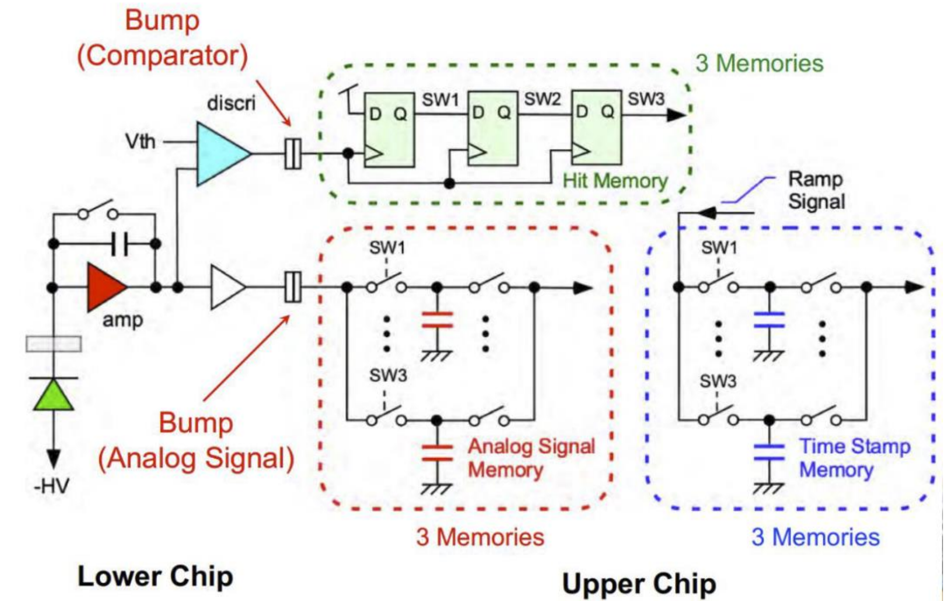
Pioneered work in SOI-3D process

The development of SOFIST sensor for the ILC experiment:

- Yasuo Arai, Miho Yamada, et al.
- Shrunk the pixel layout dramatically: 30×30 μm^2(SOFIST-3) --> 20×20 μm^2 (SOFIST-4, 3D)
- 4 connections in each pixel: one for analogue, one for digital, and a pair of power/gnd

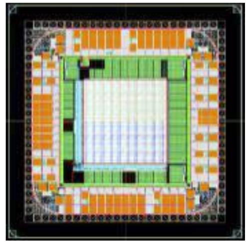
Layout and block diagram of SOFIST-4

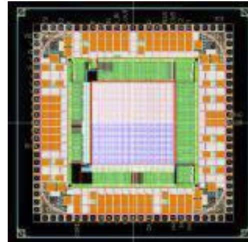




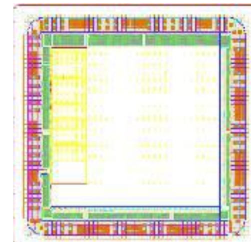
Development of serial SOI pixel sensors in IHEP

2015 2017 2019 2023

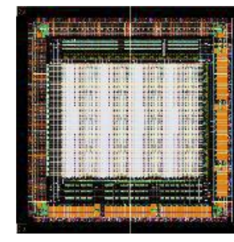

CPV-1

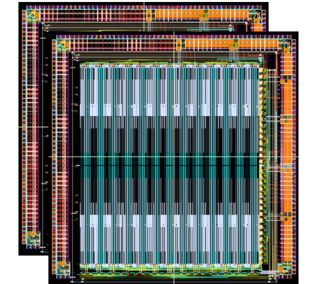

CPV-2

Investigation of Spatial resolution


CPV-3

PDD diode study


CPV-4


CPV-5

Investigation of 3D-integration

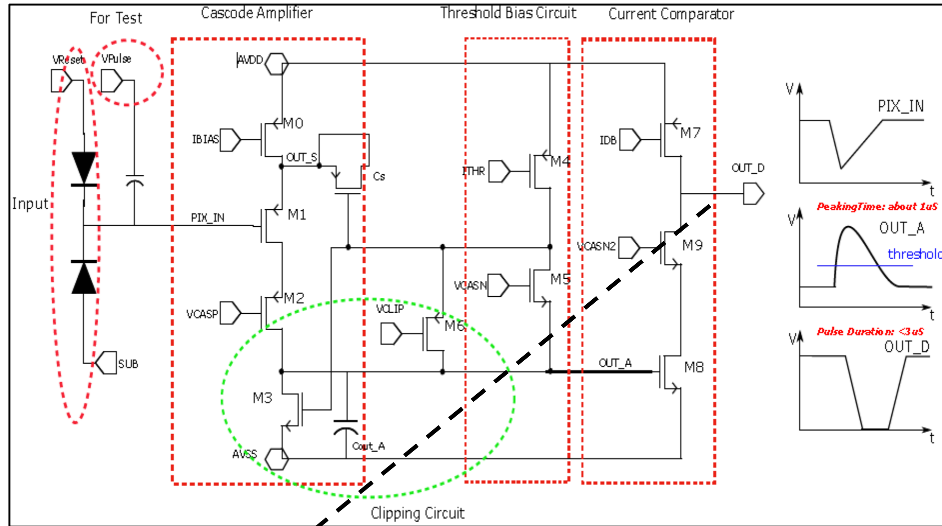
To be submitted at the end of this week.

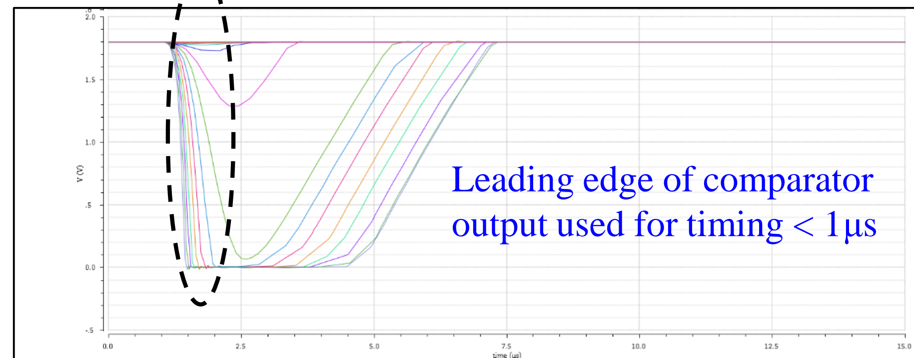
CPV series sensors developed by IHEP group

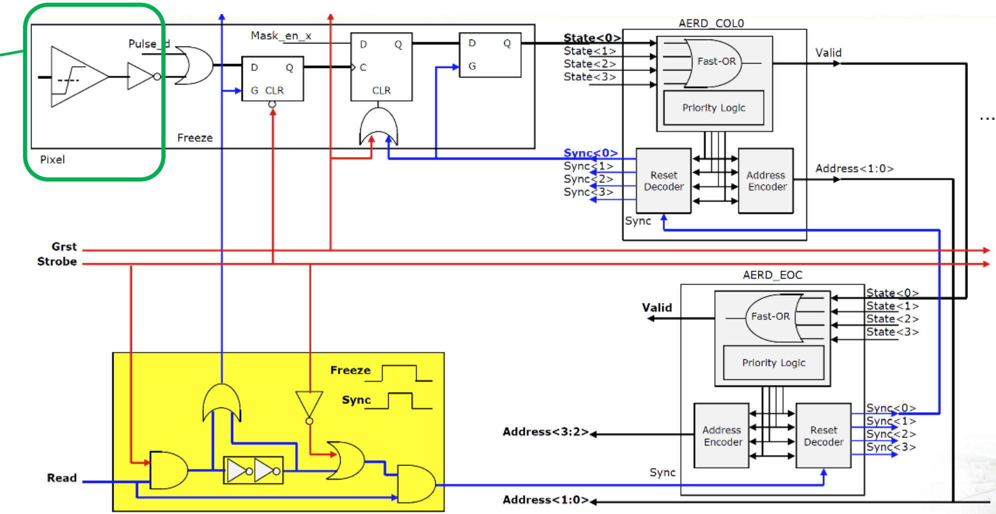
SOI activities for the CEPC:

- CPV-1&2 for the study of position resolution of small pixels with binary readout
- CPV-3 for the study of diode structure (PDD, NIMA 1040 (2022) 167204);
- CPV-4 for the 3D integration; (this talk)

CPV-4 architecture







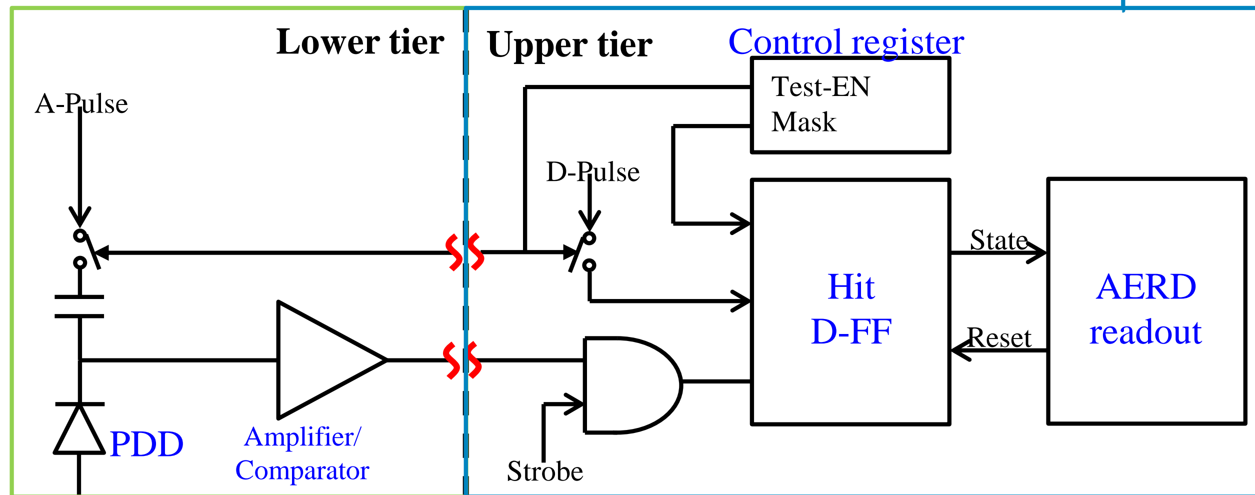
Data readout structure (simplified) of CPV4

- Low power front-end:
  - architecture same as ALPIDE (originally from ALPIDE@ CERN);
  - Using the leading edge of OUT_D pulse for timing;
- Data-driven readout (Asynchronous Encode Reset Decode*)
  - Targeting time resolution < 1μs
- Pixel area targeting < 400 μm^2

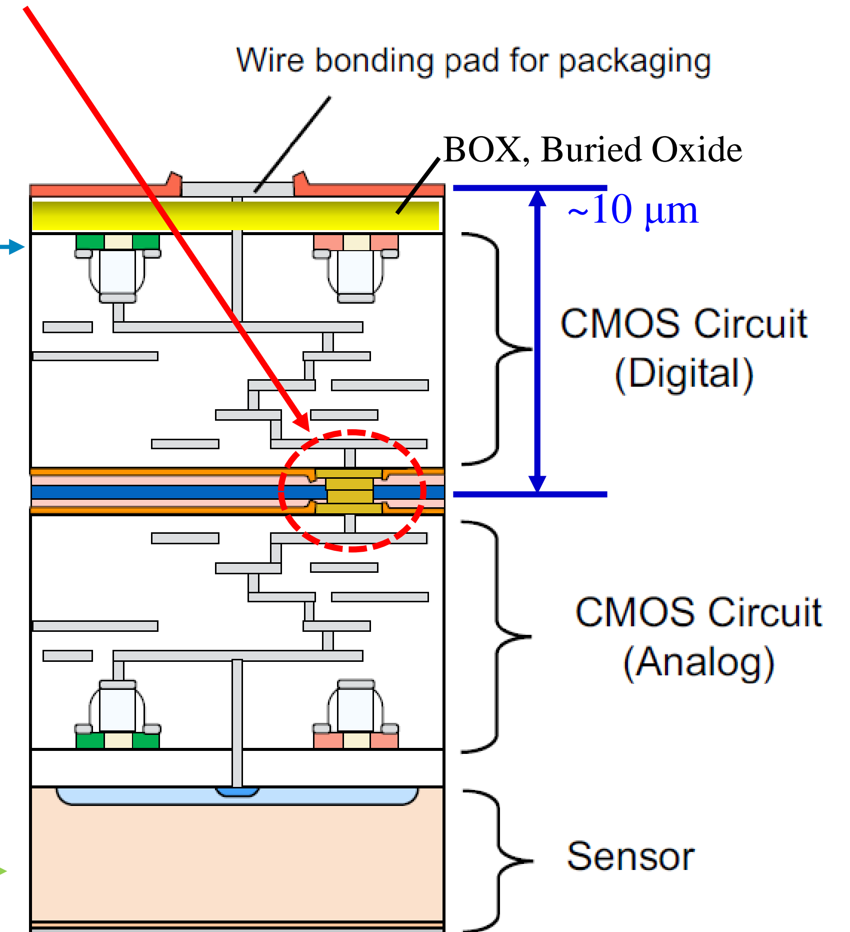
*Ping Yang et al., NIMA 785 (2015) 61-69

CPV-4: 3D implementation

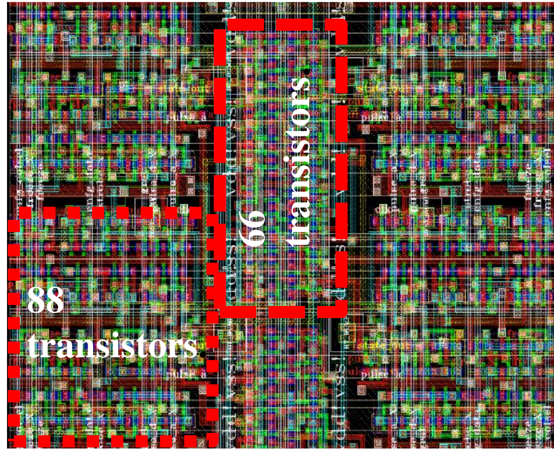
- Vertical integration of
  - Lower tier: PDD sensing diode + amplifier/comparator;
  - Upper tier: Hit D-Flipflop + Control registers + AERD readout;
  - 2 Vertical connections in each pixel: comparator output and test switch control;
- Pixel size: 17.2×21 = 361 μm^2
  - Resources of layout area and metal layers for routing ×2
- Thickness of the upper tier: ~ 10 um



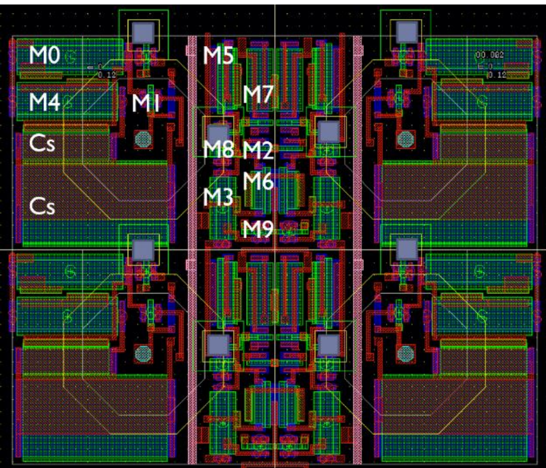
Division of upper and lower functionalities



CPV-4 layout implementation

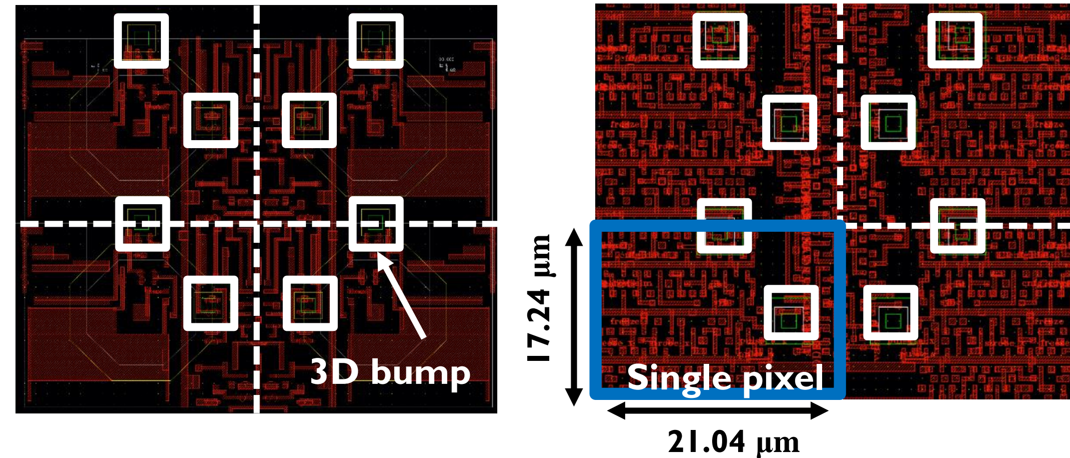


2*2 pixel layout in upper tier



2*2 pixel layout in lower tier

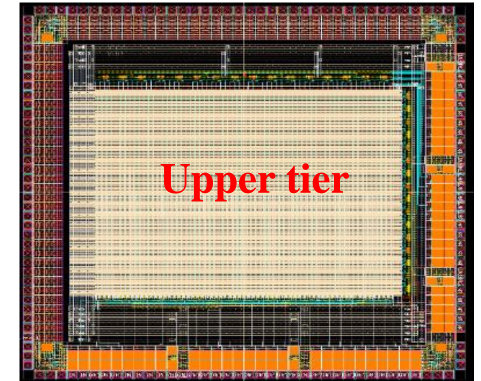
- Pixel size: 21.04 μm × 17.24 μm (resources in pixel×2)
- 2 connections in each pixel：comparator output & test switch control

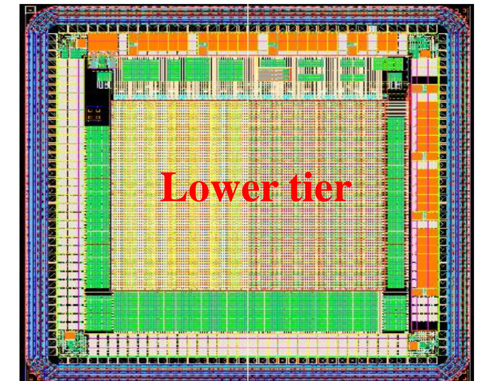


3D bump positions in 2*2 pixels of upper and lower tier (Metal_1 only)

CPV4-3D design specifications

Pixel size	17.24×21.04 μm^2
Time resolution	~1 μs or ~3 μs for different operation mode
Pixel array	128×128
Chip size	4.5mm×4.5mm

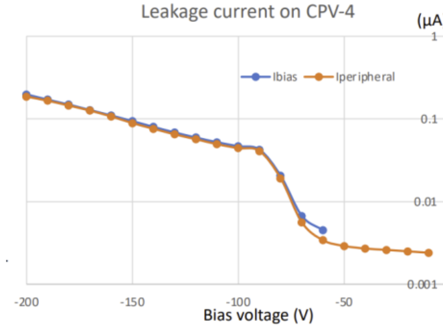




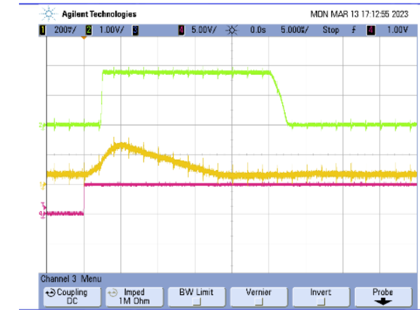
CPV4 layout of upper & lower chips

Separately tests of the upper & lower chips before 3D integration

- A test system including DAQ has been set up;
- Lower & upper chips were tested and verified separately:
  - I-V curves indicate the sensor could be biased up to -200V ;
  - Analogue and digital functionalities and responses are all work as expected from the charge or pulse injected tests;

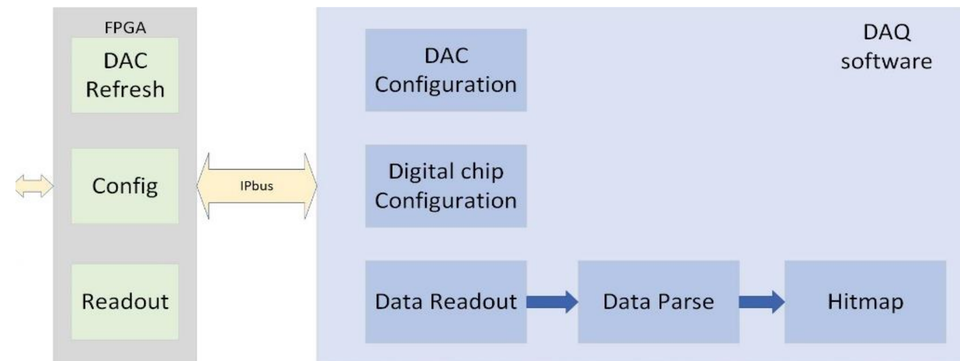


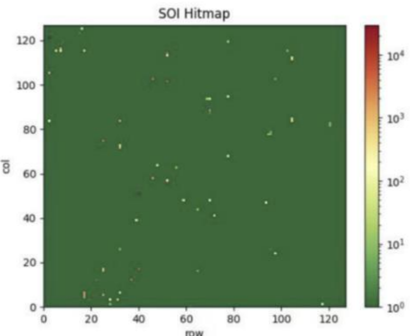
I-V curves of the sensor (test result)



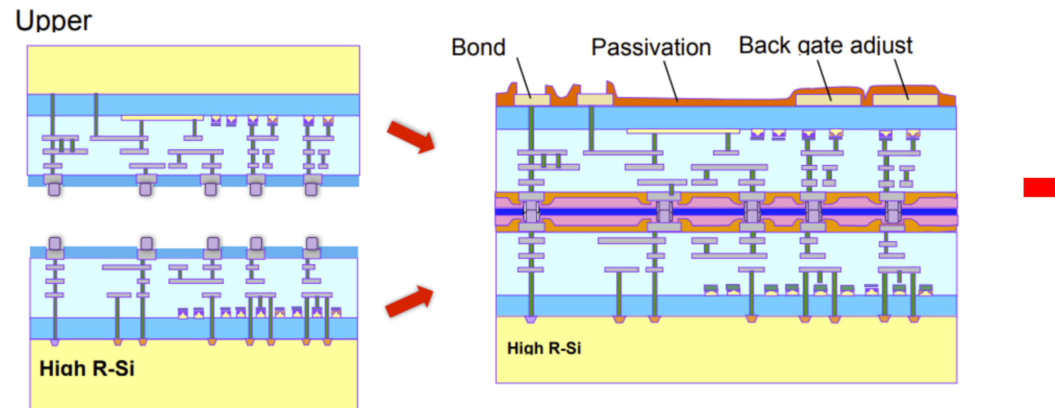
Analogue response with pulse inject test

Oscilloscope cross validation

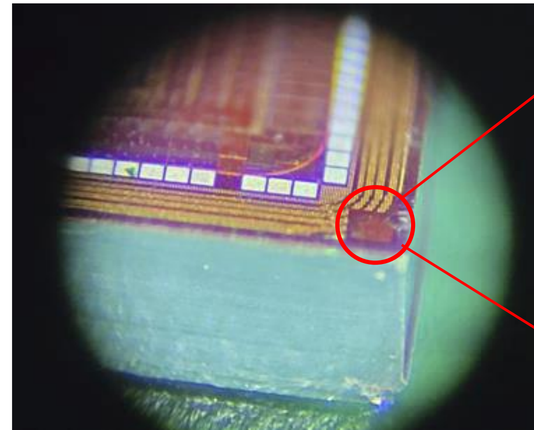


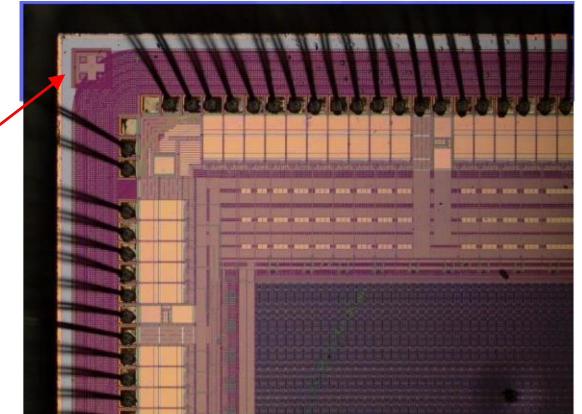


CPV-4: chip to chip 3D implementation

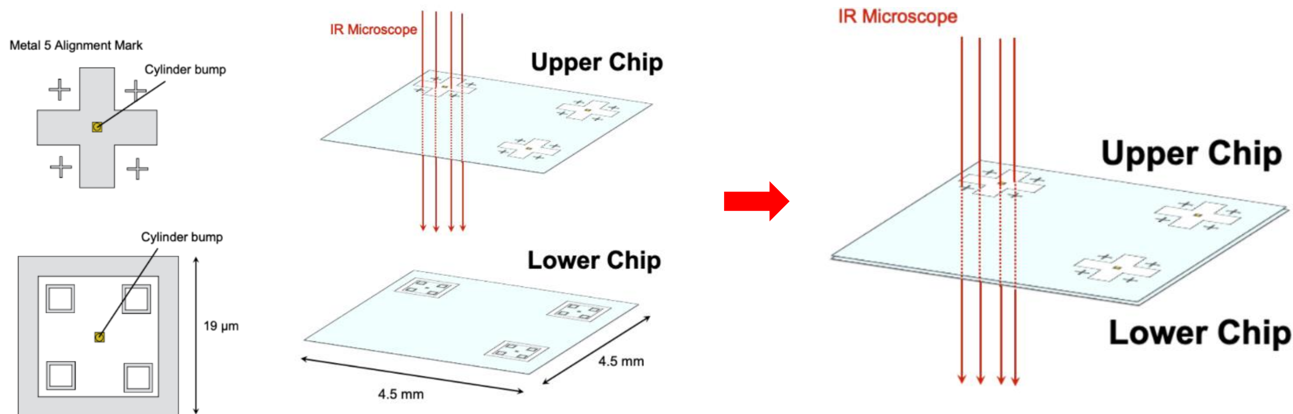


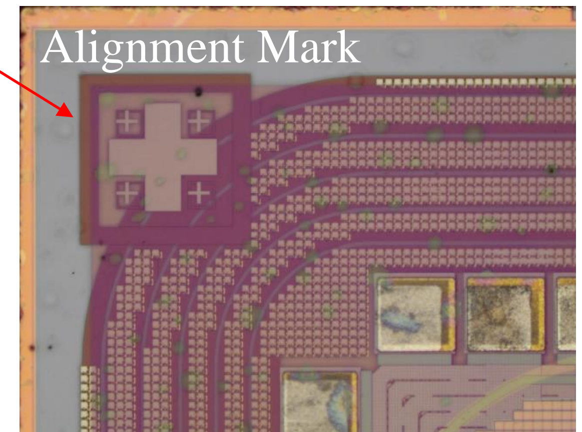
Photograph of a CPV4-3D chip.





Chip to Chip alignment

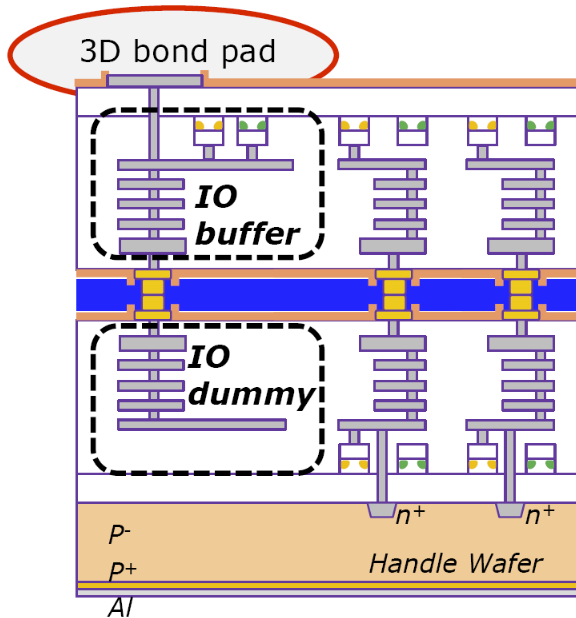


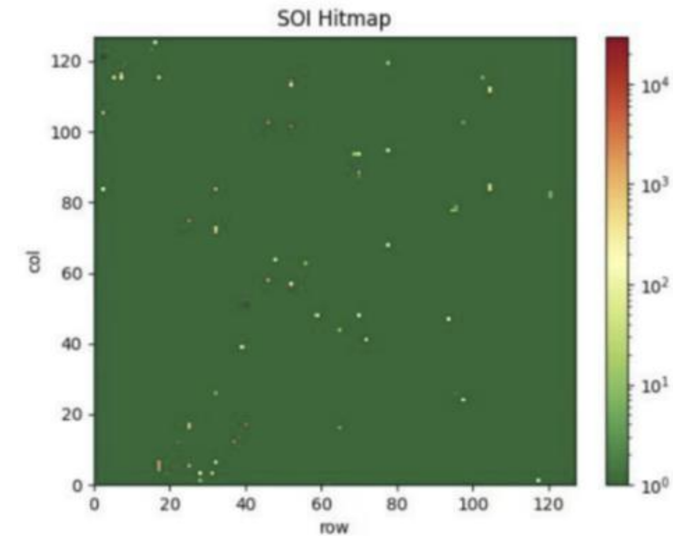


Alignment mark used to monitor the bonding results

Tests on the upper chips after 3D integration

- Same tests repeated on the upper tier after 3D integration: write to pixel configuration, injection of digital test pulse and hit readout
  - There is one chip with fully functional upper tier, so far (3D chip #009)
  - A couple more chips partially functional
- Bond pad connections to the upper tier established

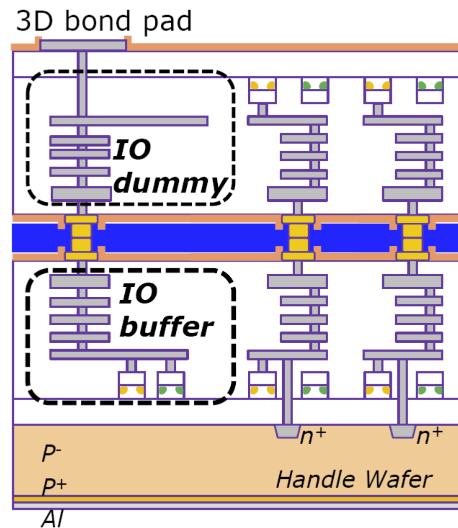




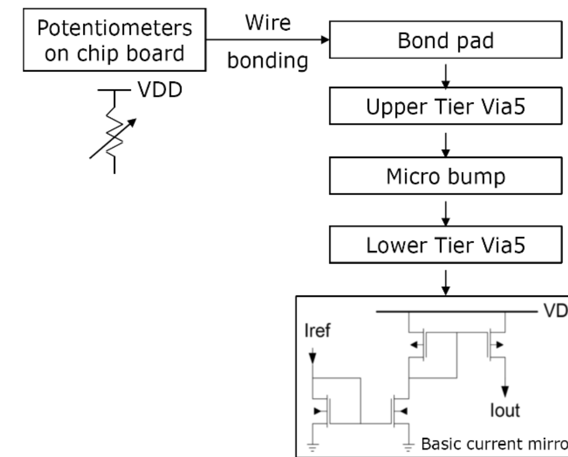
Hit map of the full matrix in digital pulse test, with masked pixels and noisy pixels visible

Tests on the lower chips after 3D integration

- Verification of the vertical connection to the lower tier:
  - The bias current on **sensing diode** responded to light illumination
  - Current mirrors in **Lower tier** worked properly
  - Multiplexer logic in **Lower tier** worked properly
- Bond pad connections to the lower tier established



Electrical connection to the current mirror in lower tier

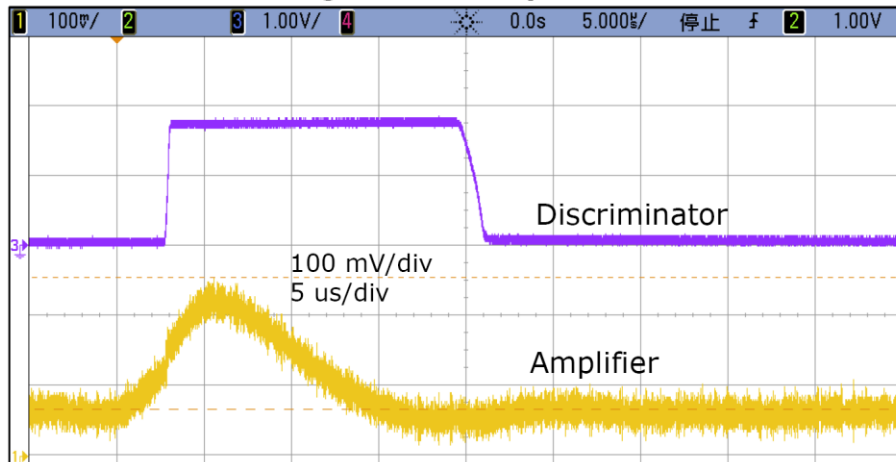


Current source channels of single lower chip vs 3D chip

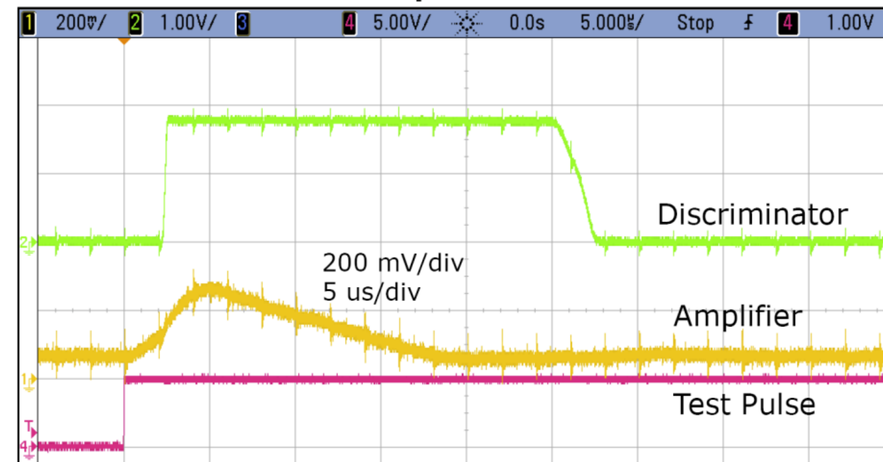
Current source channels	Single lower chip #008	3D chip #018
NSF	+24.3 uA	+23.9 uA
IOB	+73.0 uA	+70.8 uA
IDB	-0.86 uA	-0.75 uA
ITHR	-0.88 uA	-0.85 uA
IBIAS	-0.81 uA	-0.77 uA

Tests on the lower chips after 3D integration

- Observed waveforms of amplifier and discriminator on the lower tier of 3D chips:
  - There is also one chip with fully functional lower tier, so far (3D chip #004)
  - Pulse test of equivalent input charge ~160 e-



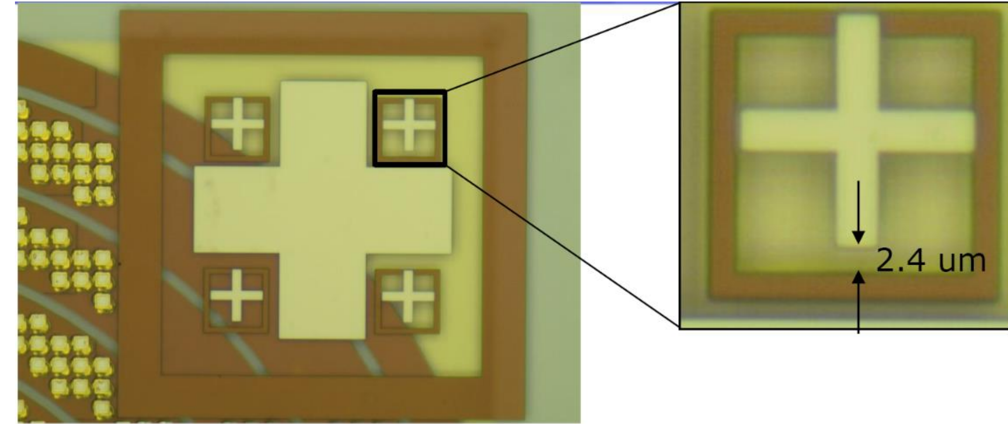
Test charge injected ~ 100 e^-

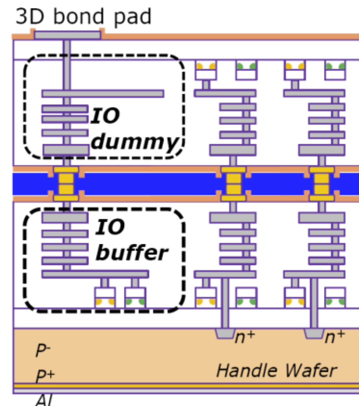


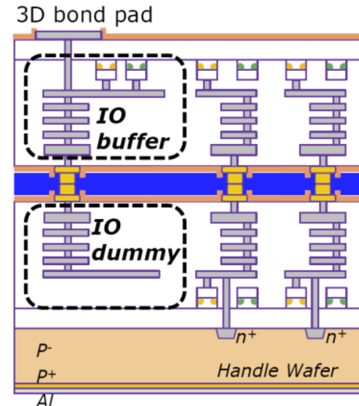
Test charge injected ~ 160 e^-

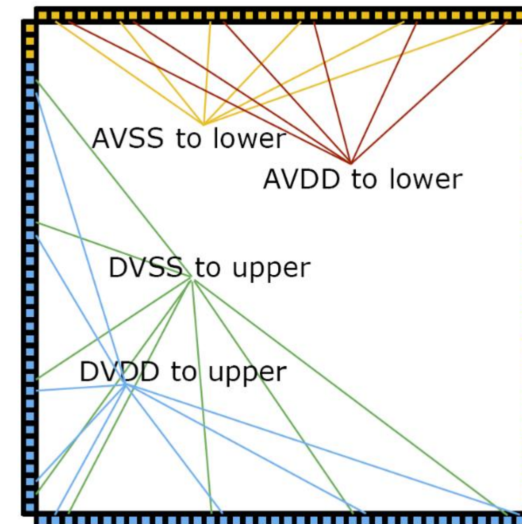
Further verification of various connections

- From bond pad to the upper tier
  - Resistance between two DVDD pads or DVSS pads
  - Good yield, 2~6 Ohm
- From bond pad to the lower tier
  - Resistance between two AVDD pads or AVSS pads
  - Low yield to be understood
- Pixel to Pixel connections
  - May be indicated by the misalignment of marks

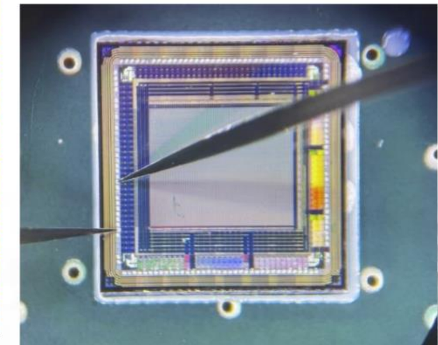








Probed pads on
3D chip #020



Summary and Outlooks

- For the innermost layer of CEPC vertex detector, it requires a position resolution < 3 μm, along with
  - Fast readout (< 1μs time resolution) for low occupancy;
  - Thin (several tens of μm thick) and low power consumption (< 50mW/cm^2) for low material;
- A 3D chip-to-chip bonding Compatible with existing SOI pixel sensor process is being pursued for high granularity of pixel with complex functionalities

  Resources of Layout area and metal layers for routing ×2

  - The extra small Micro bump pitch (~3μm diameter), allows vertical connections in each pixel;
  - Only ~10 μm thick up tier thickness, limited contribution for material;
- First trial of CPV-4 finished with encouraging results
  - A few samples identified with lower and upper tier operational
- Investigation of 3D connection yield will continue on a second wafer
  - Process tuning with T-micro is critical

Acknowledgements

- The SOI pixel detector and 3D bonding process have been developed in the framework of SOIPIX collaboration. The authors thank all the collaborators, especially Yasuo Arai, Ikuo Kurachi, Makoto Motoyoshi and Miho Yamada.

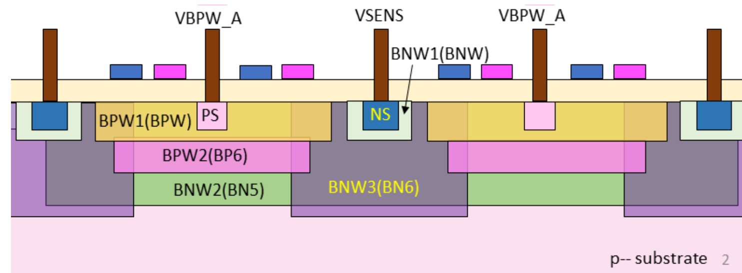
- This work is supported by
  - The National Natural Science Foundation of China (11935019, 11575220, 11375226);
  - The State Key Laboratory of Particle Detection and Electronic, IHEP;

Thank you for your attention!

Backups

CPV4-3D: PDD sensing diode system

CPV4-3D employs the PDD (Pinned Depleted Diode) sensing diode system for charge collection



Schematic view of PDD diode structure.

Composed of several layers of doped structures with different depths interface:

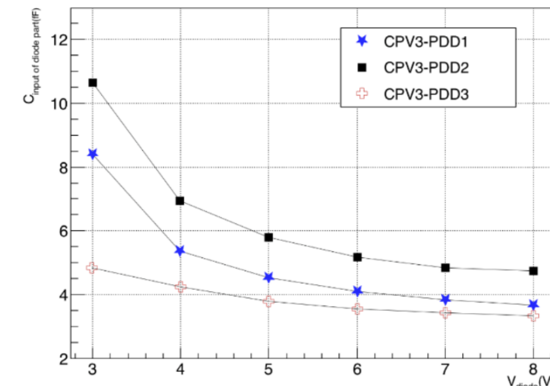
- Sensing node (NS) and the buried n-well (BNW1) form a charge collector;
- BPW1:shielding layer between circuits and the charge collector;
- BNW2, BPW2, BNW3 form a lateral gradient electrical field, benefit to charge collection efficiency;
- High negative voltage is backside applied to obtain a fully depleted substrate.

◆ Not 3D-specific, but the most active part of study in SOI pixel **sensor** technology

- Evolution of years' development: BPW, Nested-wells, Double SOI, and PDD (Pinned Depleted Diode)

◆ **All-in-one solution** in the sensor part:

- Control back-gate of transistors
- Maximize charge collection efficiency
- Suppress leakage current of Si-SiO_2 interface
- Minimize the capacitance of electrode (Cd)
- Shield the capacitive coupling between the sensor and pixel circuit



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