THE UNIVERSITY *of* EDINBURGH
School of Physics
& Astronomy

IOP
Institute of Physics

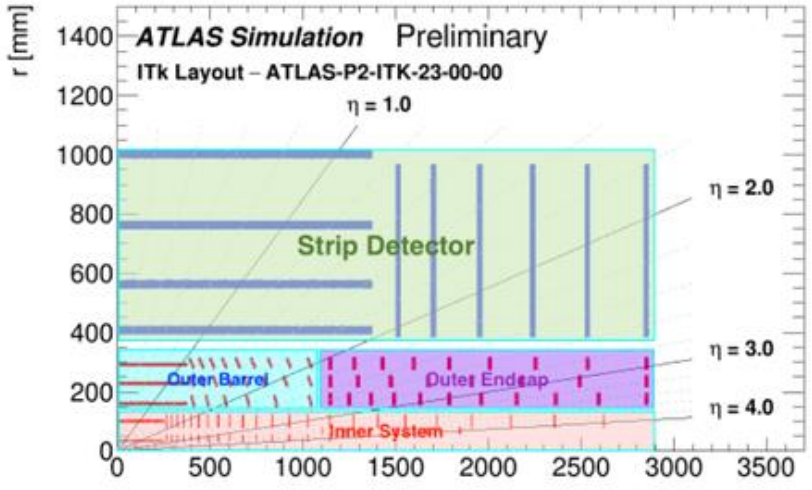
Pixel Detector Development for Future Collider-Based Particle Physics Experiments

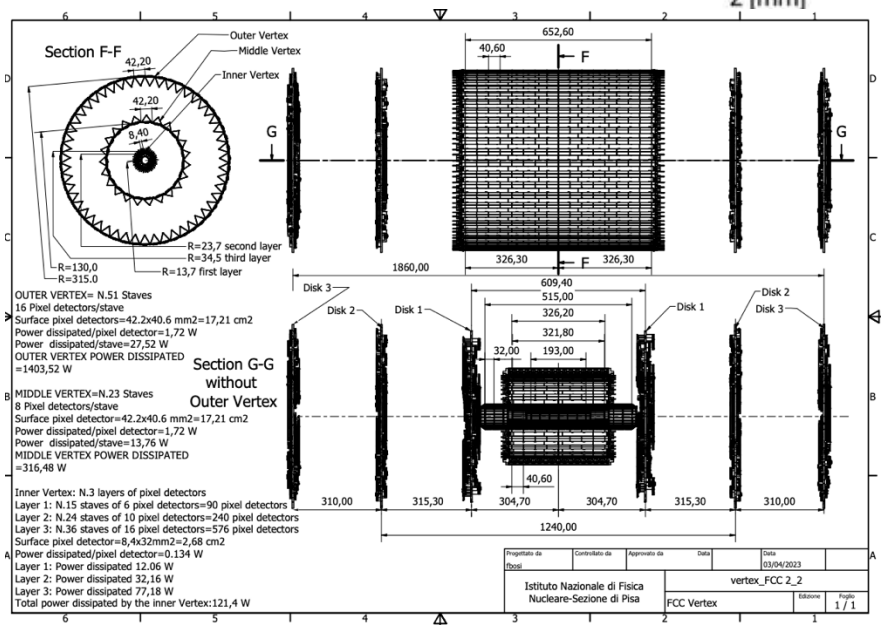
Fuat Ustuner

09.04.2025

IOP Joint APP and HEPP Annual Conference, April 2025

Silicon as a Tracking Device



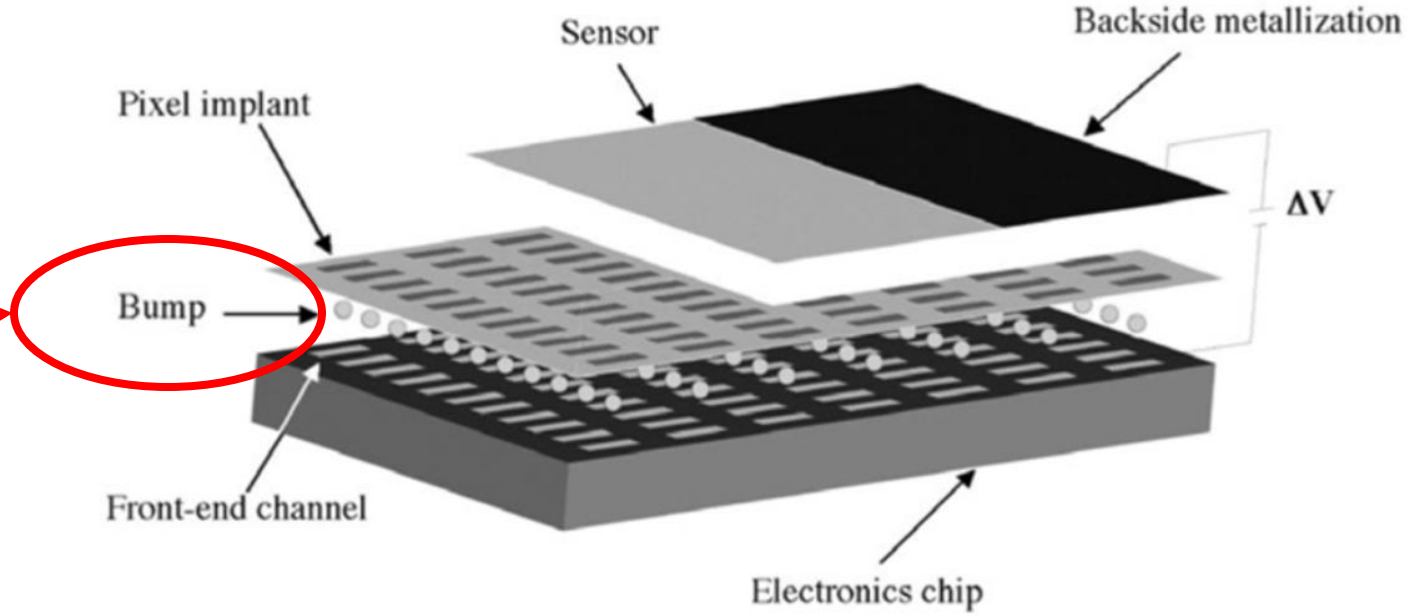


IDEA Study Group, The IDEA detector concept for FCC-ee, 2025

- Silicon is the most common material for collider-based experiments as a tracking detector.
- The combination of well-suitable properties for charged particle detection.
  - **small band gap**
  - well-established industrial production processes
  - relatively **low production costs**
- Two examples of silicon-based tracking detectors from,
  - **ATLAS ITk (top)**
  - **Proposal of vertex detector layout for FCC-ee (bottom)**

Pixel Detectors in Particle Physics

- Standard silicon-based technologies for particle tracking are strip- and **hybrid-pixel detectors.** (ITk upgrade)
- The sensor and readout chips are connected by a method called **flip-chip bonding**.
- However, some disadvantages:
  - **Cost (High):**
    - Readout chip
    - Sensor
    - Assembly
  - **Construction process is complex**
  - **Potential thermal behaviour**



ATLAS ITk, pixel detector area is ~10m^2 = ~25.000 sensor

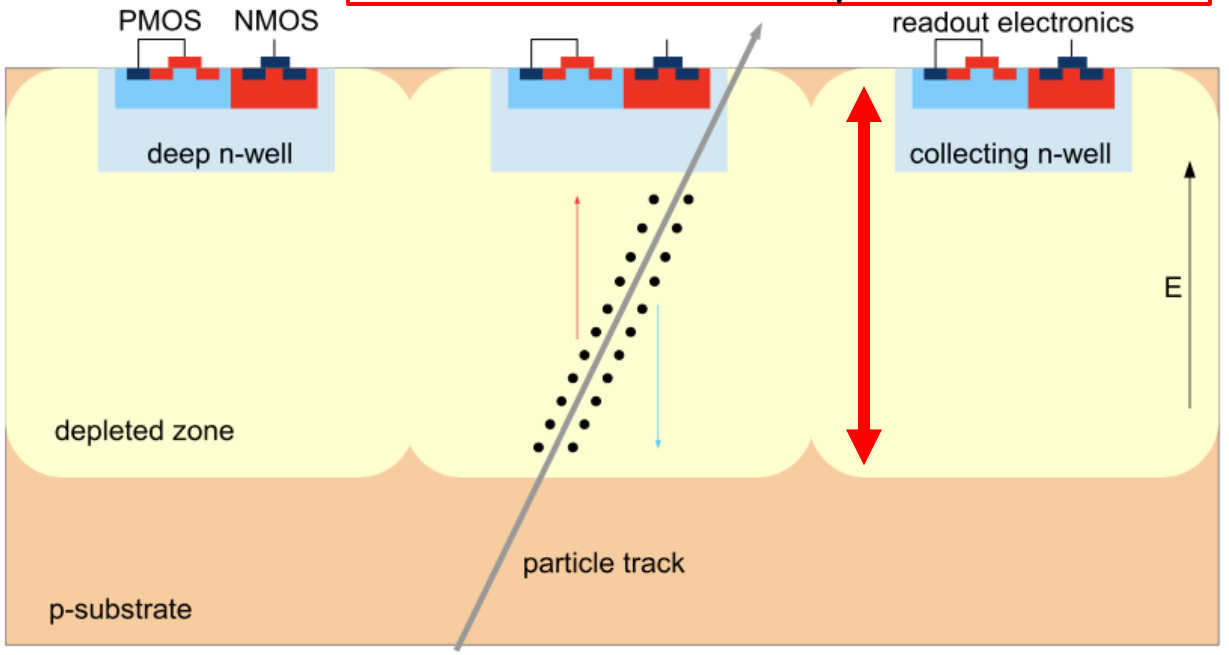
If we increase this area to 50-100m^2 ?

High Voltage Complementary Metal-Oxide Semiconductor (HV-CMOS)

- **HV-CMOS** technology offers **solutions** to address some of the limitations.
- HV-CMOS sensors are active pixel sensors for ionizing particles, produced with commercial CMOS processes.
- The electronic readout and active area are in **the same silicon die**. (monolithic).
  - Production cost (low) → No hybridisation
  - A much simpler assembly procedure

- Multiple-well structure model:
  - **Deep n-well**: charge collection electrode and protect readout from high radiation.
  - P and n-well and p-substrate.
- Fast charge collection via **drift** in depleted volume via E-field.
- **High-time resolution**.

$$Depletion\ depth \propto \sqrt{\rho_{substrate}.Uext}$$

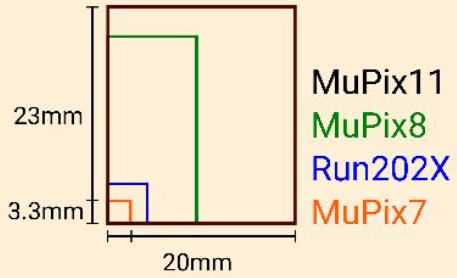


HV-CMOS Technology on Silicon Tracker Development

R&D Series

ATLASPix Series

MuPix Series

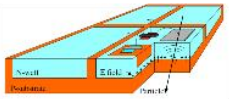


MuPix11
MuPix8
Run202X
MuPix7

AMS AG ah18

TSI Semiconductors h18

HV-MAPS Concept



2007

[I. Peric, P. Fischer et al., NIM A 582 (2007) 876]

Proof-of-Principle

MuPix1

42x36 Pixel
39x30 µm²

2011/2012

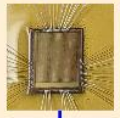
MuPix2

MuPix3

42x32 Pixel
92x80 µm²

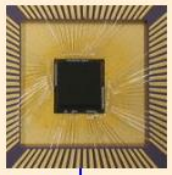
2013

Digital Readout



MuPix4

Fully Monolithic



MuPix7

MuPix6

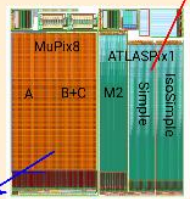
42x32 Pixel
103x80 µm²

2014

MuPix8

128x200 Pixel
81x80 µm²

1st Large-Scale Prototypes

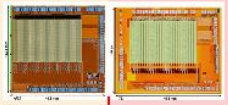


2017

ATLASPix1

25x400 Pixel
130x40 µm²

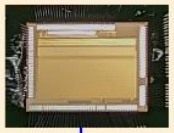
ATLASPix2



2017
24x36 Pixel
110x45 µm²

Mu3e Slow Control

MuPix9

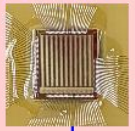


128x200 Pixel
81x80 µm²

2017

Fab Validation

MuPix7.1



42x32 Pixel
103x80 µm²

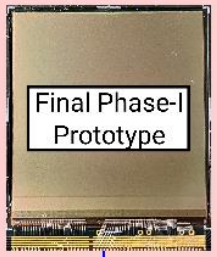
2018

1st Full-Scale Prototype

ATLASPix3

2019
132x372 Pixel
150x50 µm²

MuPix10



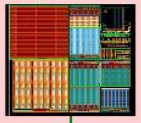
Final Phase-I Prototype

256x250 Pixel
80x80 µm²

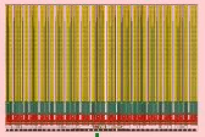
2020

Run2020

Run2021

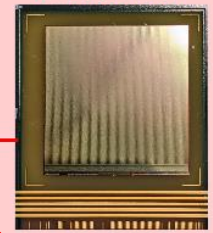


TelePix2



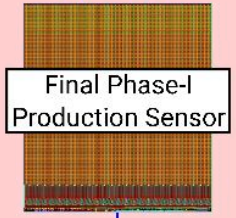
2020
2021
2022
120x400 Pixel
165x25 µm²

ATLASPix3.1



2021

MuPix11



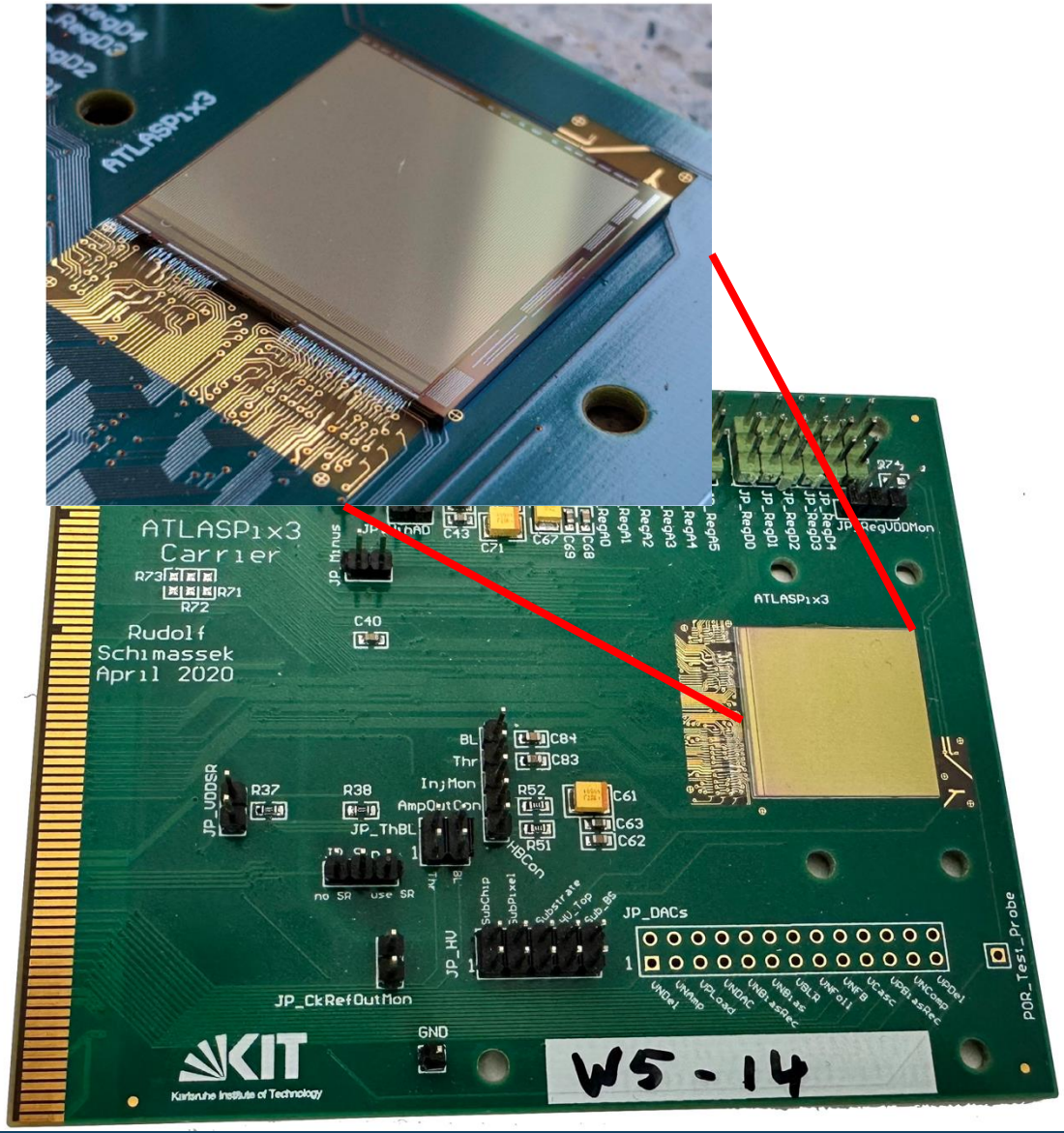
Final Phase-I Production Sensor

256x250 Pixel
80x80 µm²

2022

D.M. Immig, Straggling with Ultra-Thin HV-MAPS

ATLASPix3.1



HV-CMOS Technology	TSI 180nm
Substrate [Ωcm]	200
Matrix [pixel]	132x372 (~49000 pixels)
Pixel Pitch [µm^2]	50x150
Sensor size [mm^2]	20.2x21

- The first full size monolithic HV-CMOS sensor including two fully functional **shunt low-dropout regulators**. → Serial Powering
- The breakdown voltage is ~-65 V (unirradiated)
- Each pixel has its own readout electronics and insensitive periphery where the digital processing is confined.

GECCO DAQ

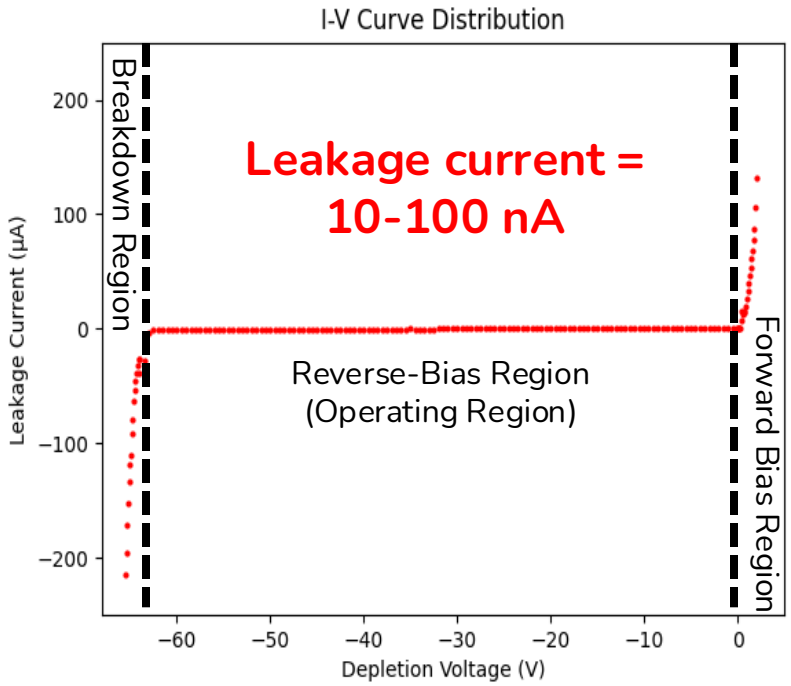
FPGA: Nexys Video Artrix-7

Generic Configuration and Control (GECCO) System (developed by **KIT**)

Single Chip Carrier (SCC) Board and ATLASPix3.1 chip

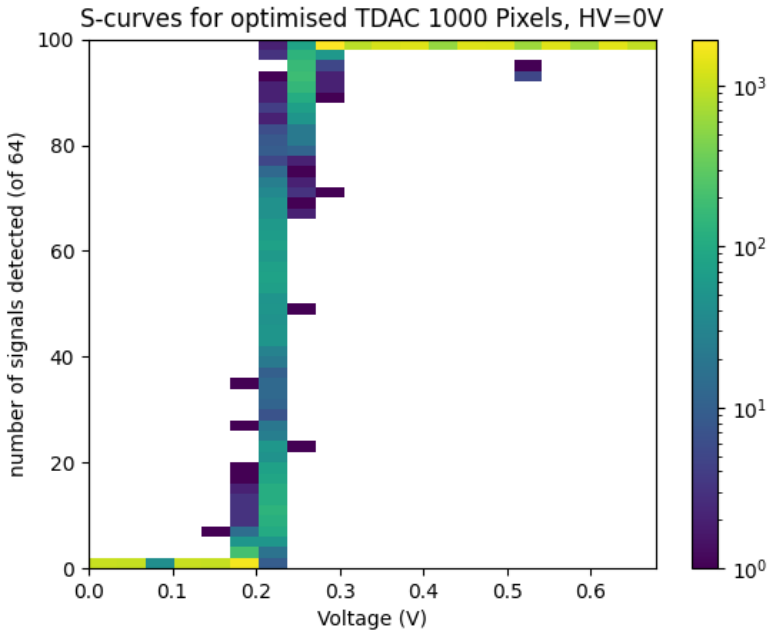
Single Chip Characterisation

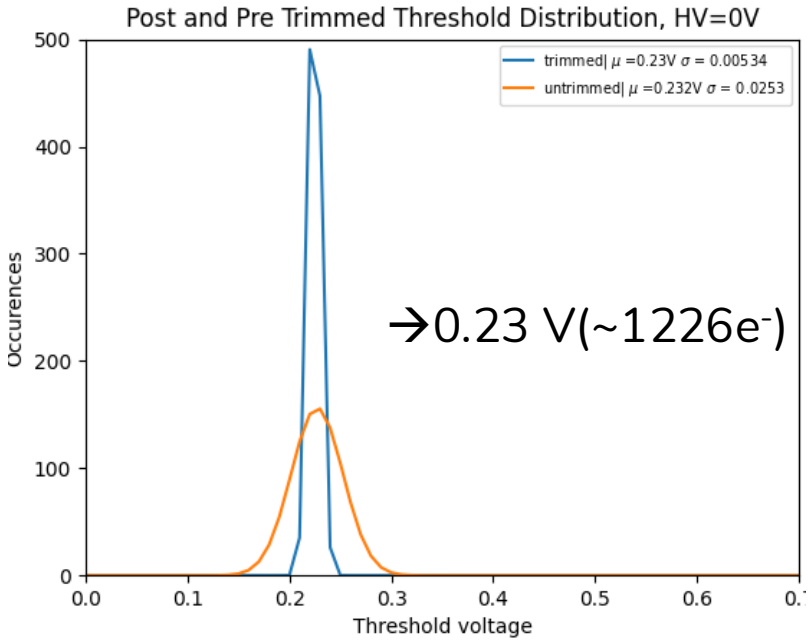
- **IV Curve**



- To evaluate **pixel resistivity, leakage current, breakdown voltage** and **diode quality**.
- The breakdown voltage is **~-65V**.

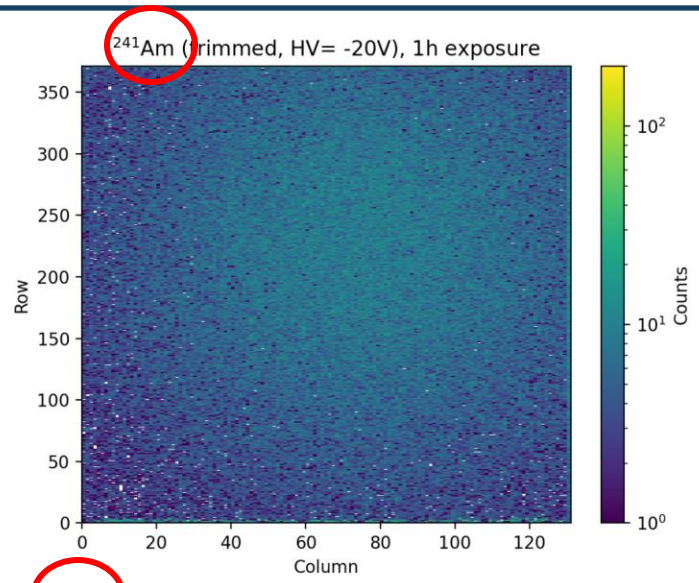
- **S-Curve & Threshold Tuning**

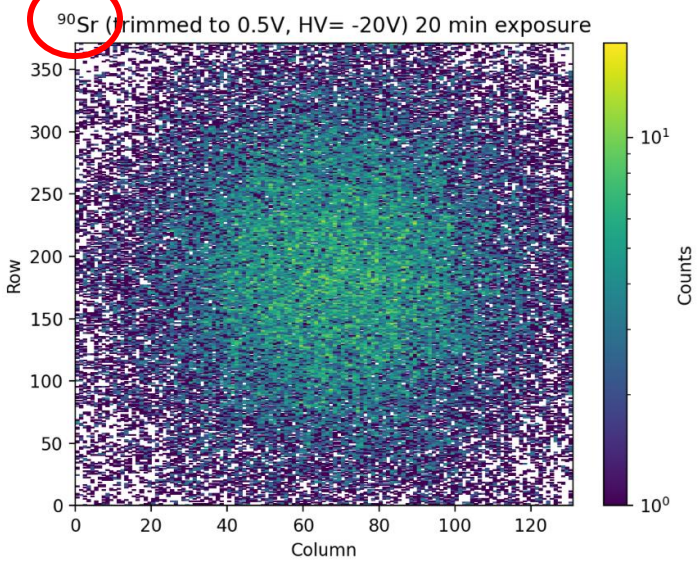


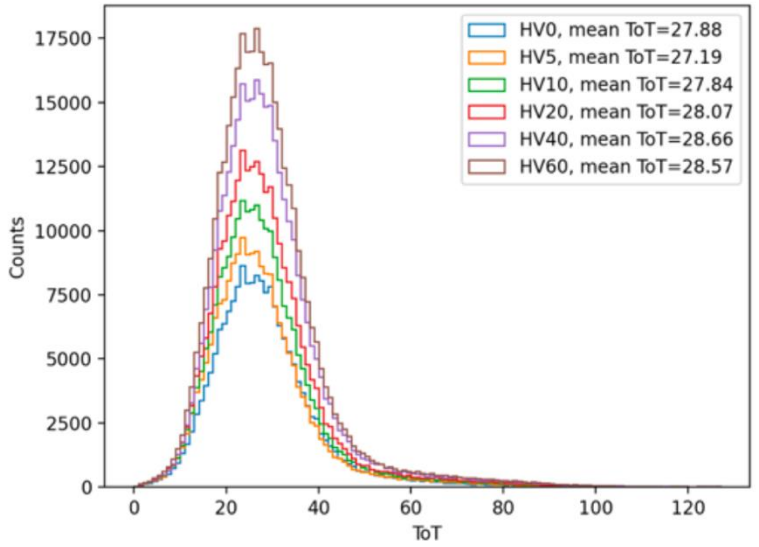


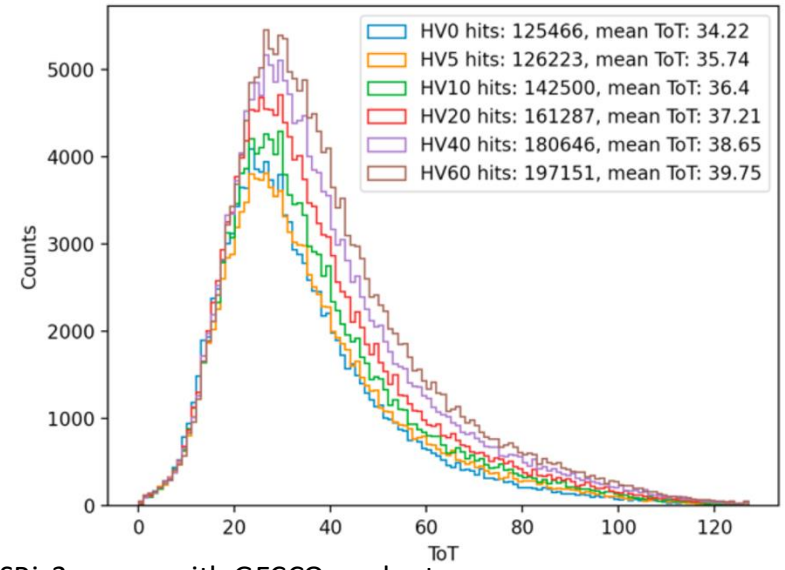
- The same **1000 pixels** are operated for threshold scans
- The target threshold is **~0.2V** for tuning.
- The S-curve (left) and threshold distribution (right) show the tuning is provided to the target.

ATLASPix3.1 Radiative Source Tests







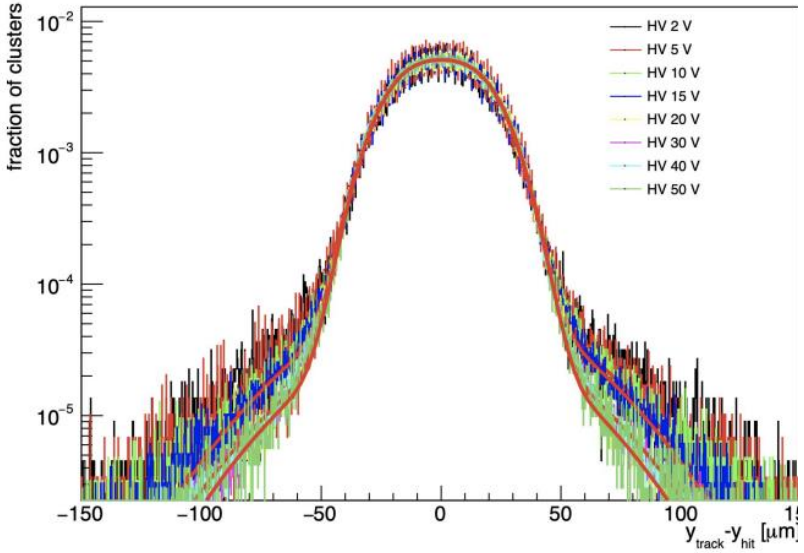


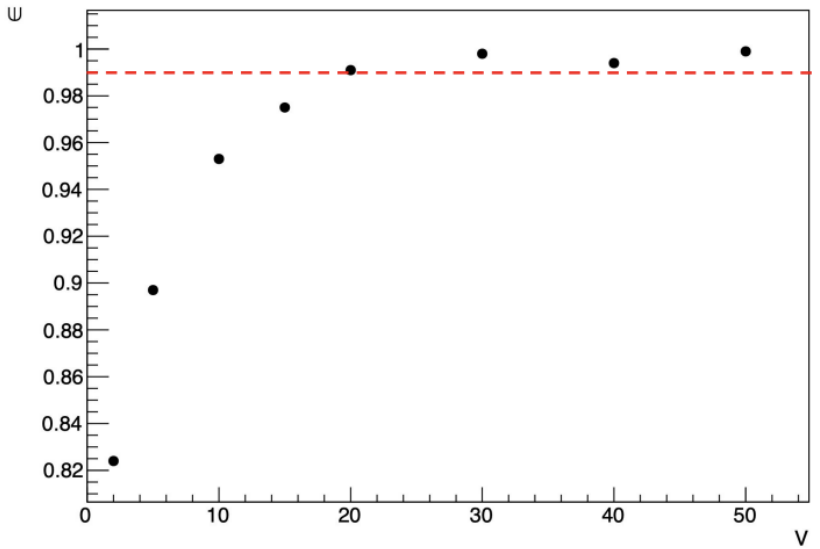
- An exposure of ATLASPix3.1 to the **^{241}Am** (top) and **^{90}Sr** (bottom) sources.
- Responsive to incident **photons from the alpha decay of ^{241}Am.**
- The **^{241}Am** ToTs are almost the same at different HVs**.**
- The emission of **^{90}Sr** is **beta particles (as they are e^-)**
- ToT & HV bias has linear relationship.

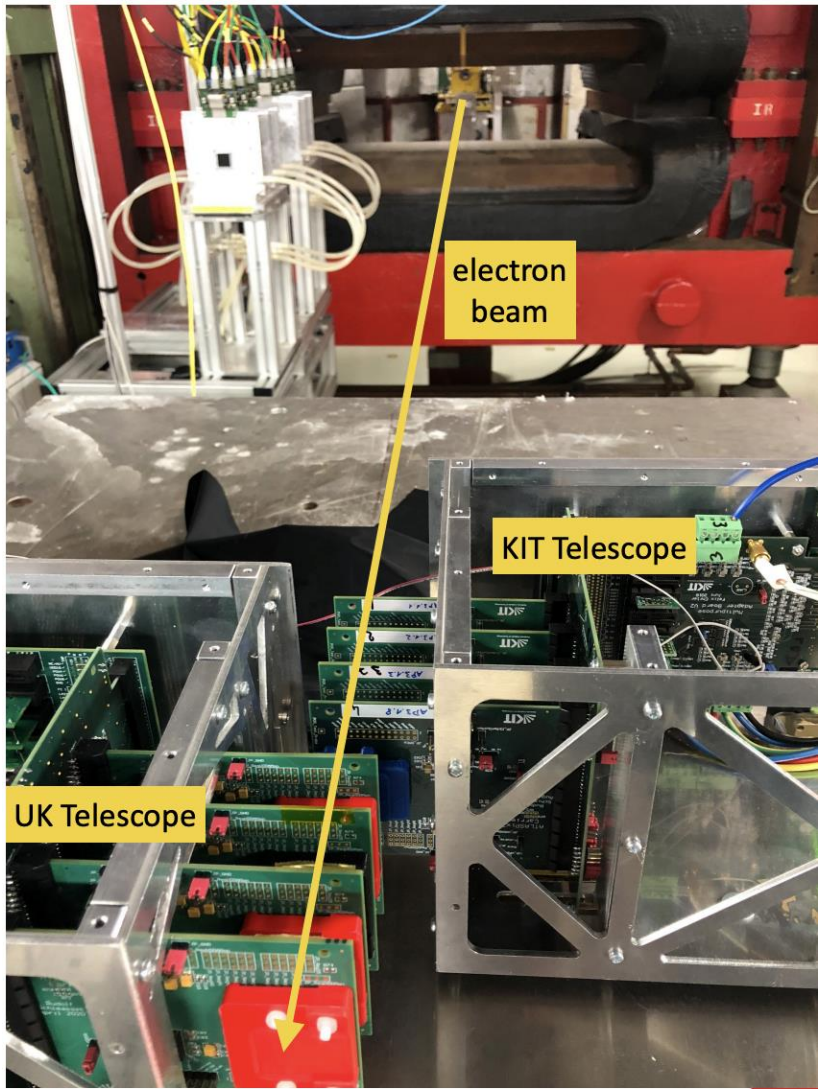
J. Martin, Characterisation of the HV-CMOS based ATLASPix3 sensor with GECCO readout

ATLASPix3.1 Beam Test

- Up to 6 GeV e^- beam at DESY in 2022
- Two 4-layer telescopes from (KIT and UK)
- Reconstruction with Corryvreckan
- The track residuals in y, with increasing 0-50V HV(depletion voltage).
- The efficiency reaches **99.8%** at 50V.



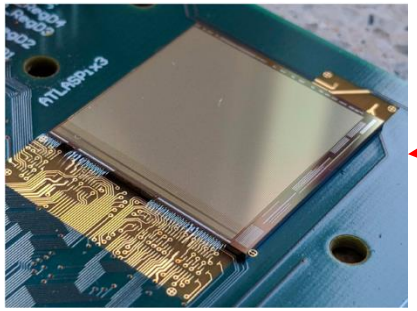


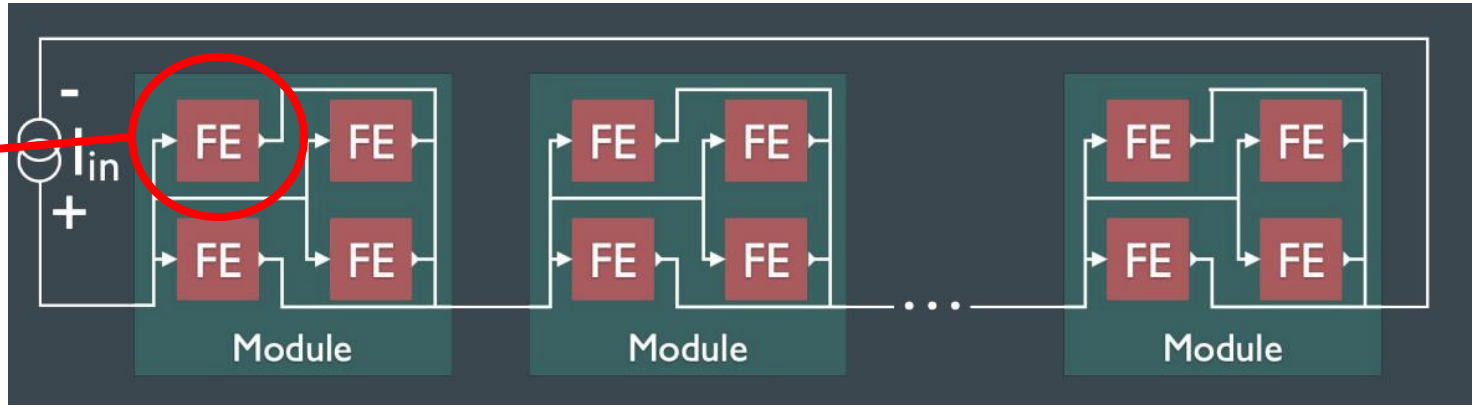


R.Zanzottera, The ATLASPIX3 CMOS pixel sensor performance, ICHEP 2024

System scale and Serial Powering (SP)

- System readout challenge: scale 1 -> $2x10^5$ sensors
  - Data aggregation is usually implemented to minimize services (power/data lines)
    - Leads to multi-chip modules (e.g. quad module in ITk) usually powered in parallel
  - To minimise the multi-module system power consumption, it is desirable to use Serial Powering, where all modules in a local structure are powered via **constant current**
- SP is developed and verified for **ATLAS and CMS** pixel upgrade LS3 using **hybrid pixel detectors**.
- **However, none has been done for HV-CMOS-based pixel detectors.**

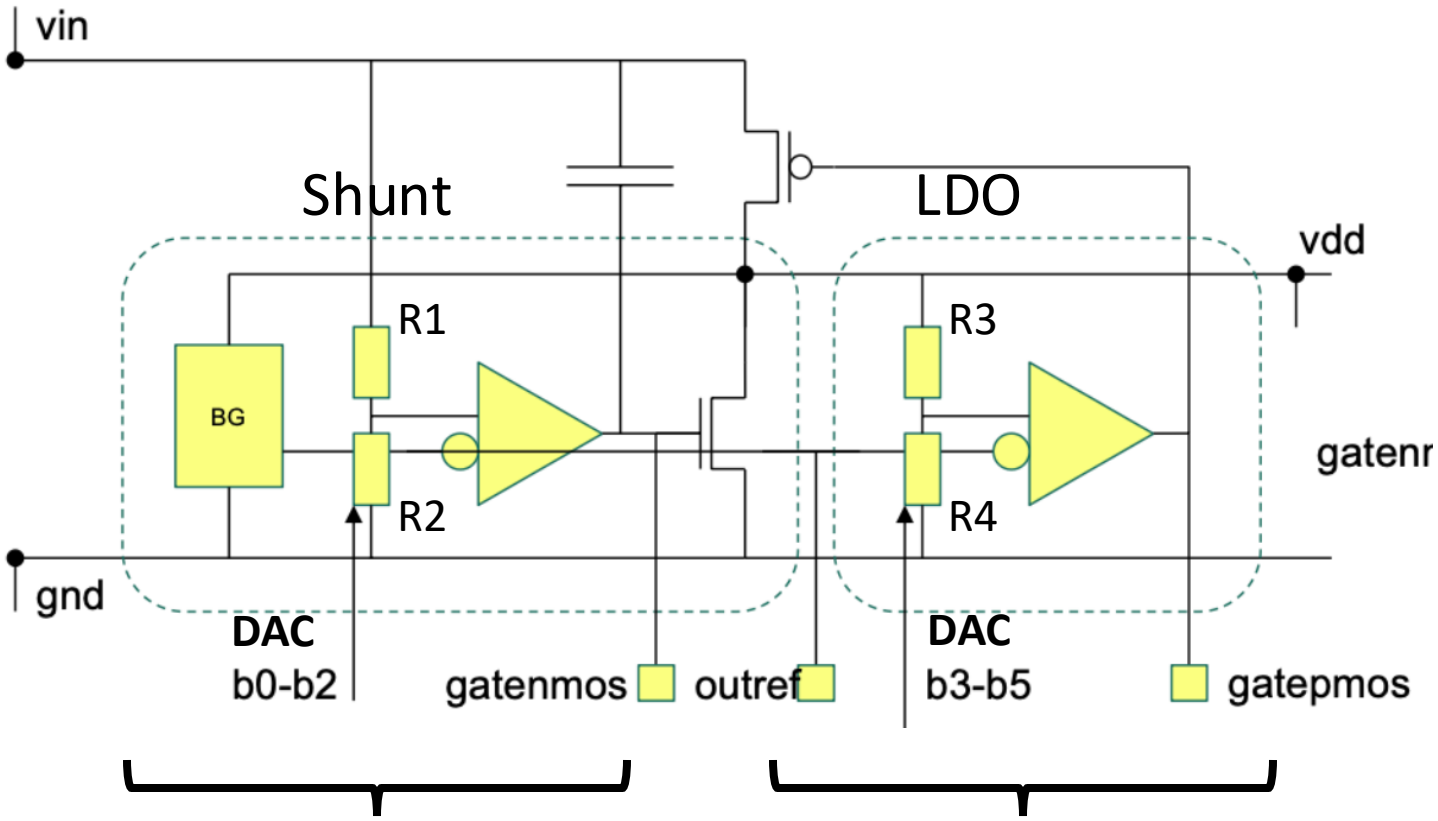




J. Chan, Serial Powering of ATLAS ITk Pixel Modules

Shunt-LDO Regulators on ATLASPix3.1

- Serial Powering requires **shunt-low dropout regulators at the chip level**
- **Shunt:** gives ohmic behaviour and allows for the constant current operation.
- **Low dropout:** performs a second round of regulation (minimal voltage drop from Vin to Vdd, **the margin: ~0.5V**)
- ATLASPix3.1 can be powered via a **single constant current** with two shunt-low dropout regulators.
  - **Vin** is created from constant current via regulators.
  - **VDDD/A** presents the **regulated voltage** (output of the shunt-LDOs) to use the chip for operation.

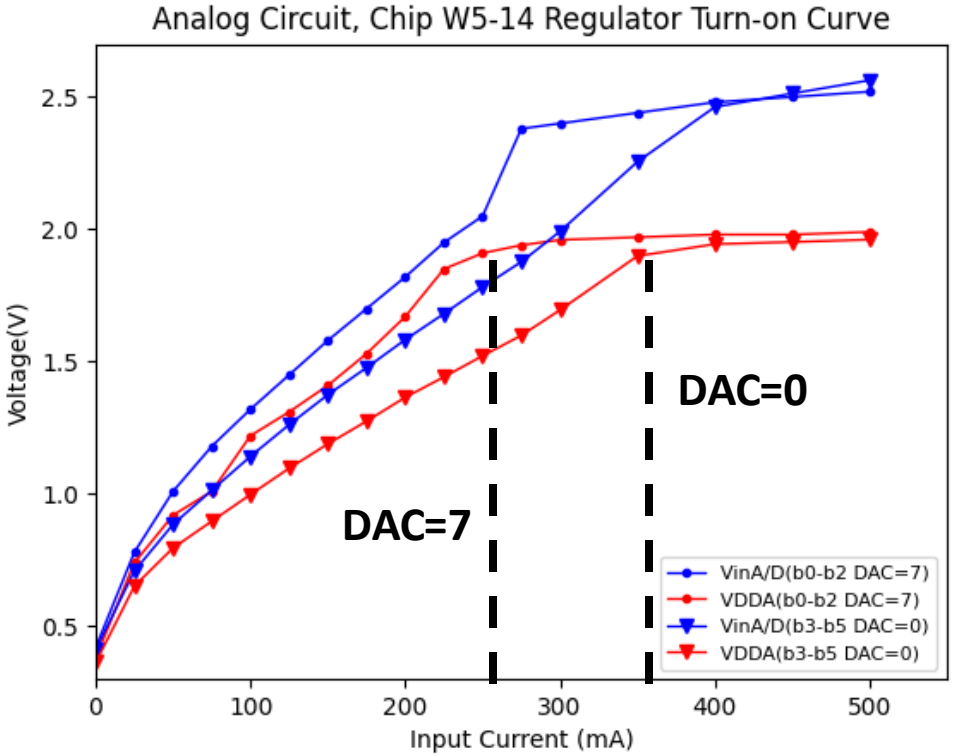


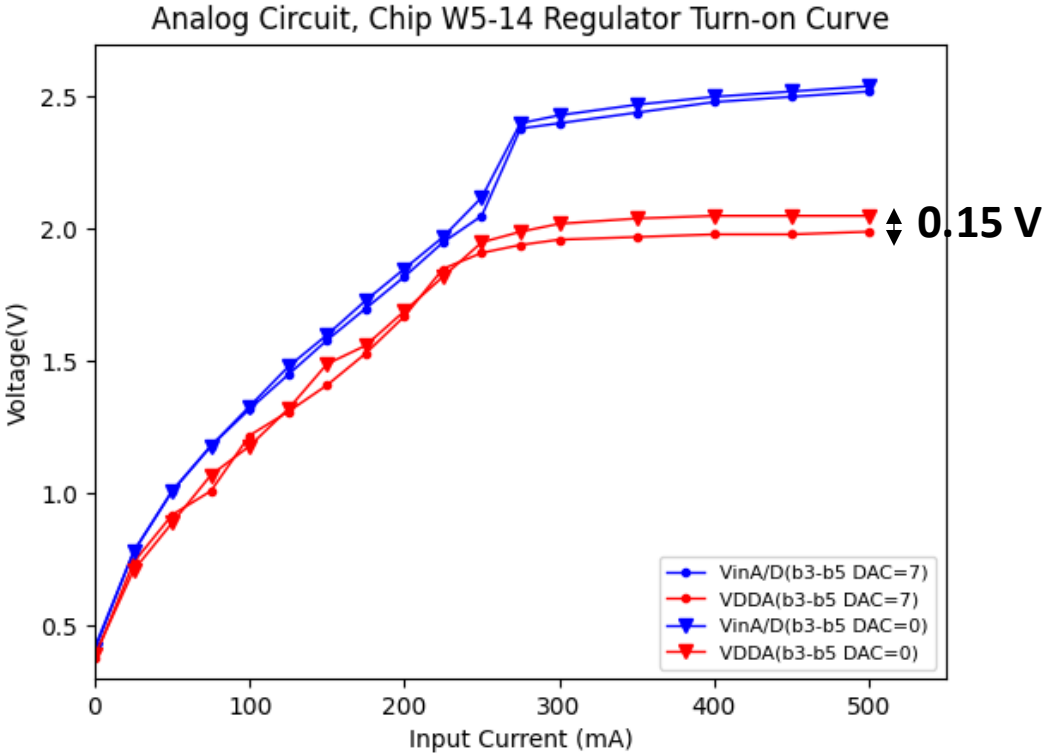
$$V_{in} = \frac{V_{ref}}{\alpha_1} \quad \alpha_1 = \frac{R2}{R1 + R2}$$

$$V_{dd} = \frac{V_{ref}}{\alpha_2} \quad \alpha_2 = \frac{R4}{R3 + R4}$$

Shunt-LDO Regulators Characterisation (Single-Chip)

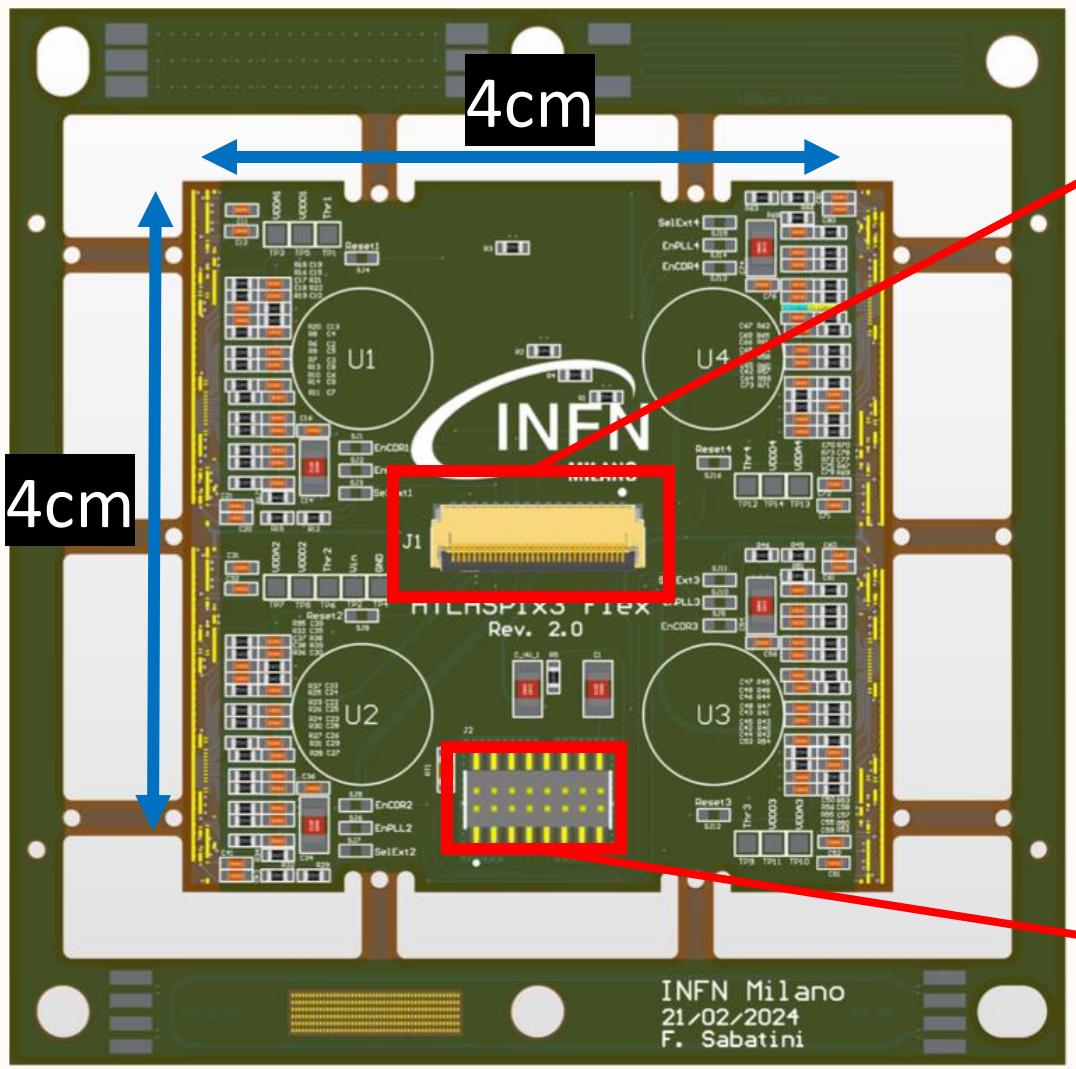
- **3-bit DAC b0-b2** for threshold of the shunt regulator.
  - VDDD/A voltages are regulated when input current ~**250-300mA** DAC=7, **~350-400mA** DAC=0
- **3-bit DAC b3-b5** allows small amount of tuning in VDDA/D outputs
  - The turn-on value is ~**250-300mA**
  - VDDD/A output regulated to **~1.8-2V**.
  - These are consistent with the current consumed using direct powering supplying similar VDDD/A.





F. Ustuner *et al,* The ATLASPix3.1 CMOS Pixel Sensor Performance and System Level Design 2025 *JINST* **20** C02036

ATLASPix3.1 Quad Flex

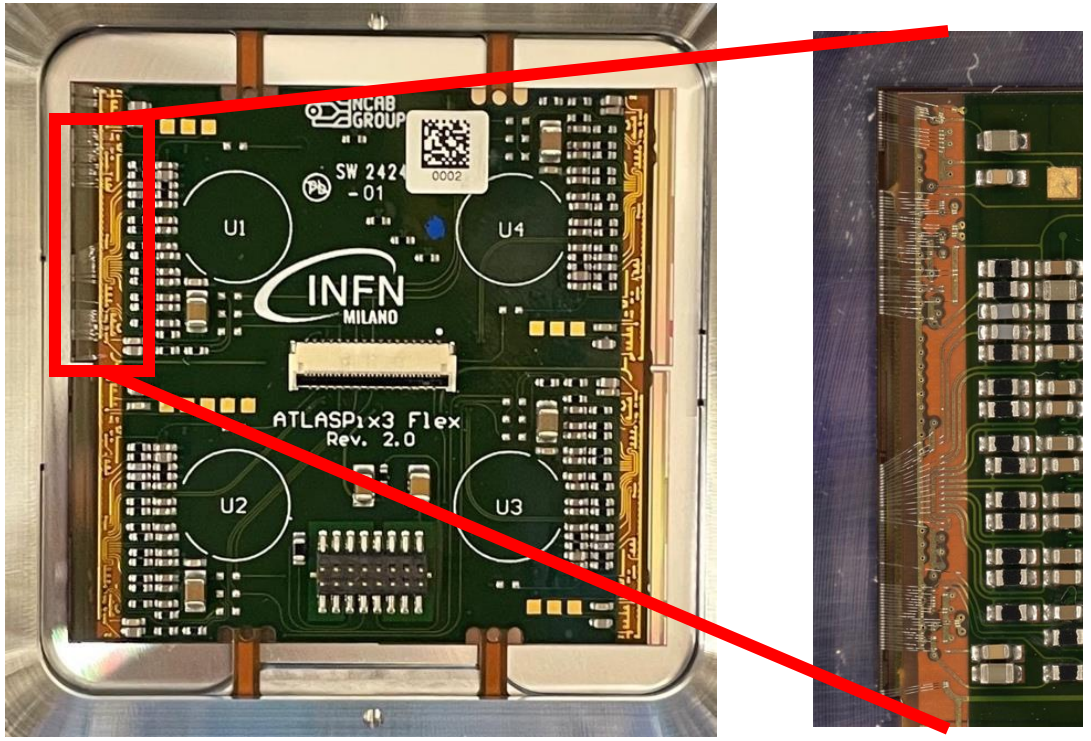


Molex, Data Connector

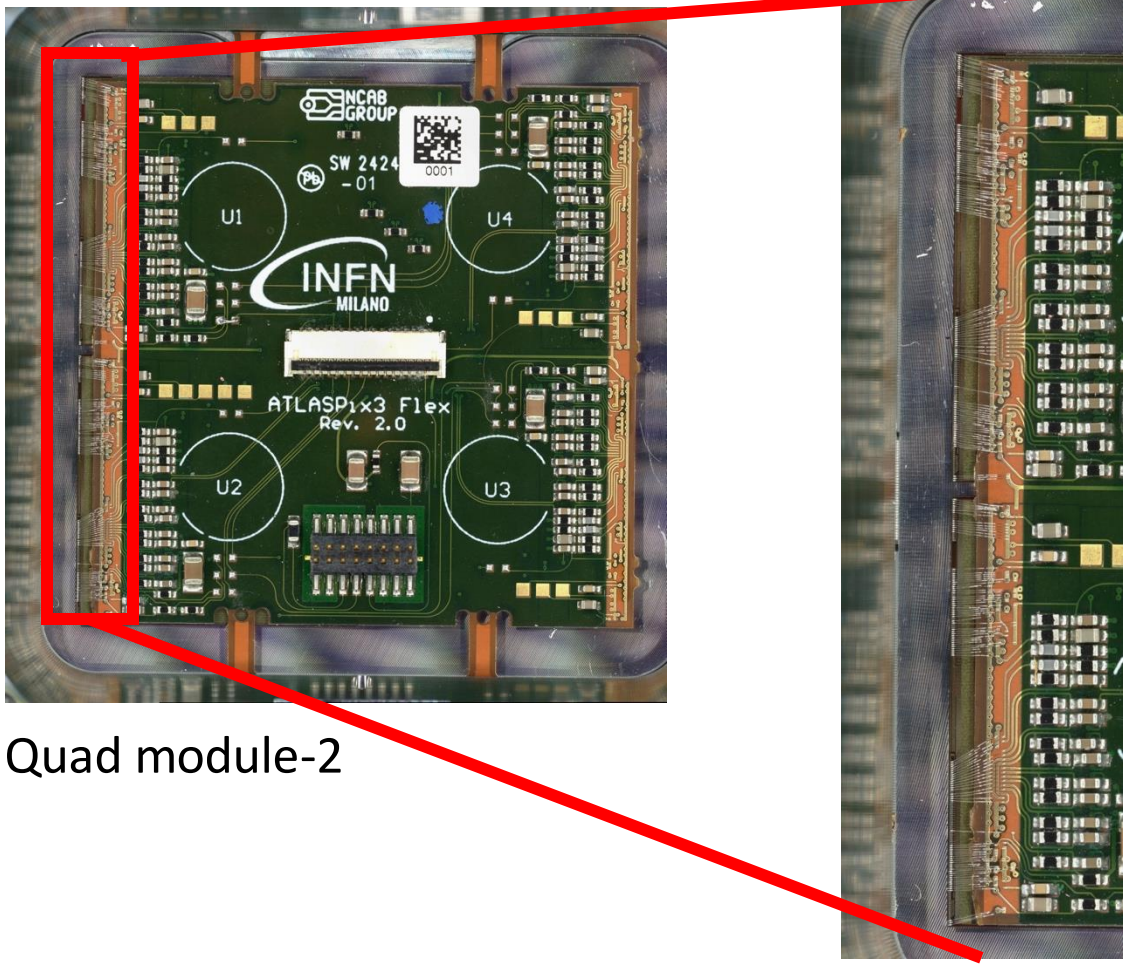
- The multi-chip quad module system, comprising four ATLASPix3.1 chips within a **4x4 cm²** area.
- Facilitates shared powering and data transmission.
- The chips are all connected in **parallel** in the module.
- The quad module, **serial powering integration** make it ideal for large-scale applications.

FTM-108, Power Connector

ATLASPix3.1 Quad Module



Quad module-1

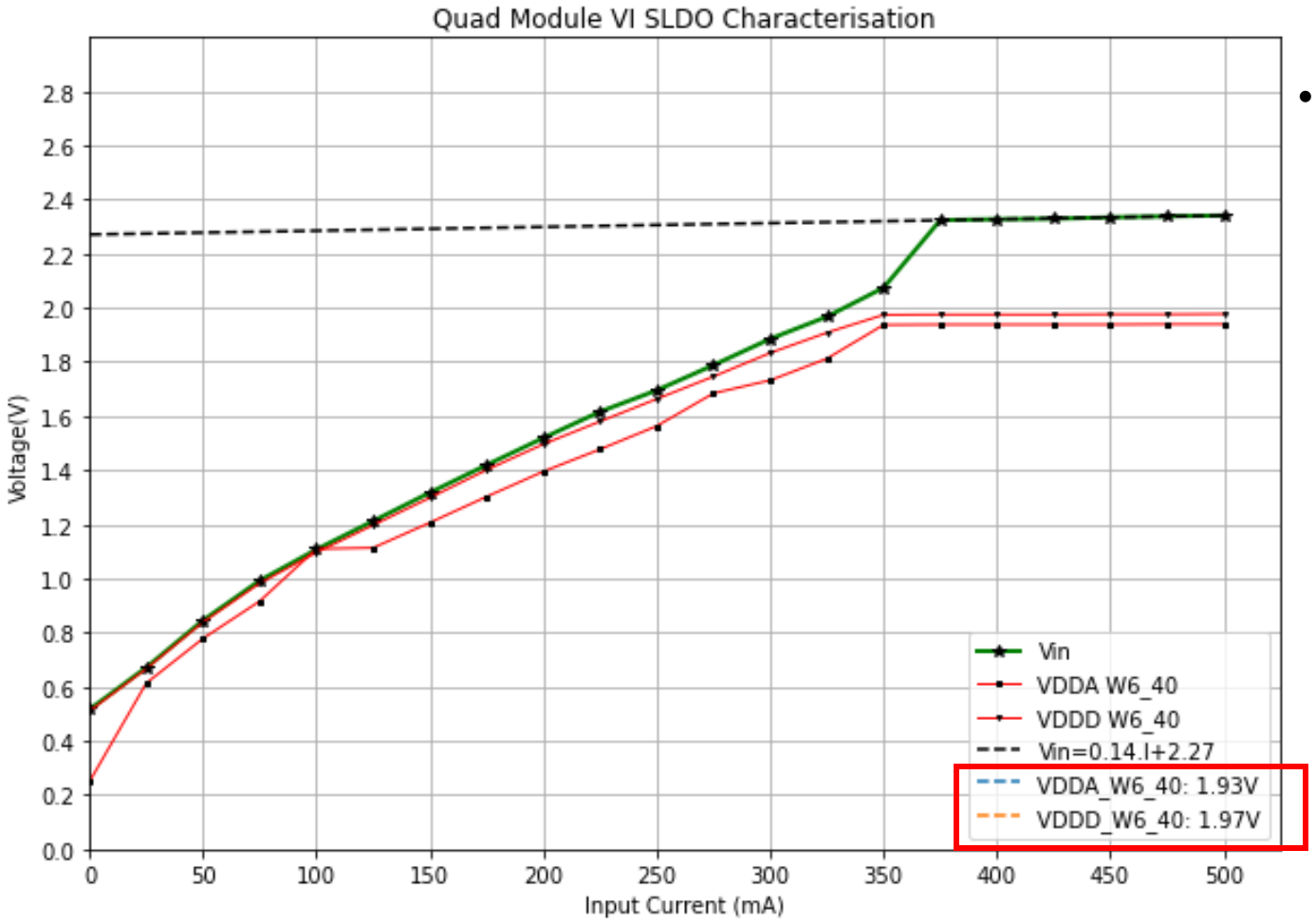


Quad module-2

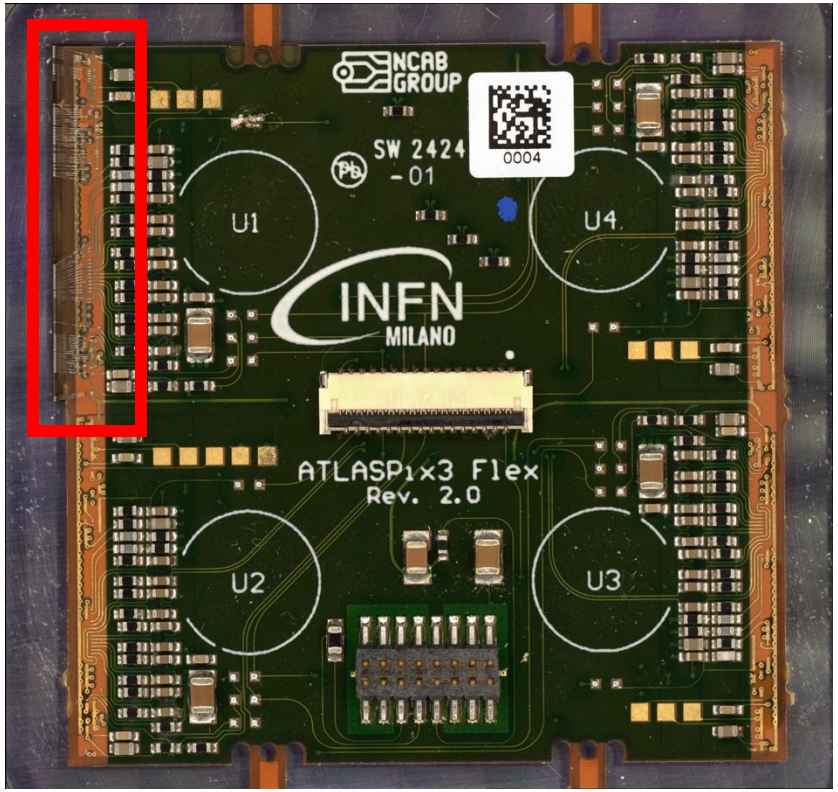
- Two quad modules are wirebonded:
  - Quad Module-1: **Chip1 - W6-40**
  - Quad Module-2: **Chip1 - W6-28** and **Chip2 - W6-29**

Quad Module-1 (IV Characteristics)

- The quad module-1 includes one wirebonded chip (**W6-40)**.
- The input current is **349 mA** as the regulation starts.

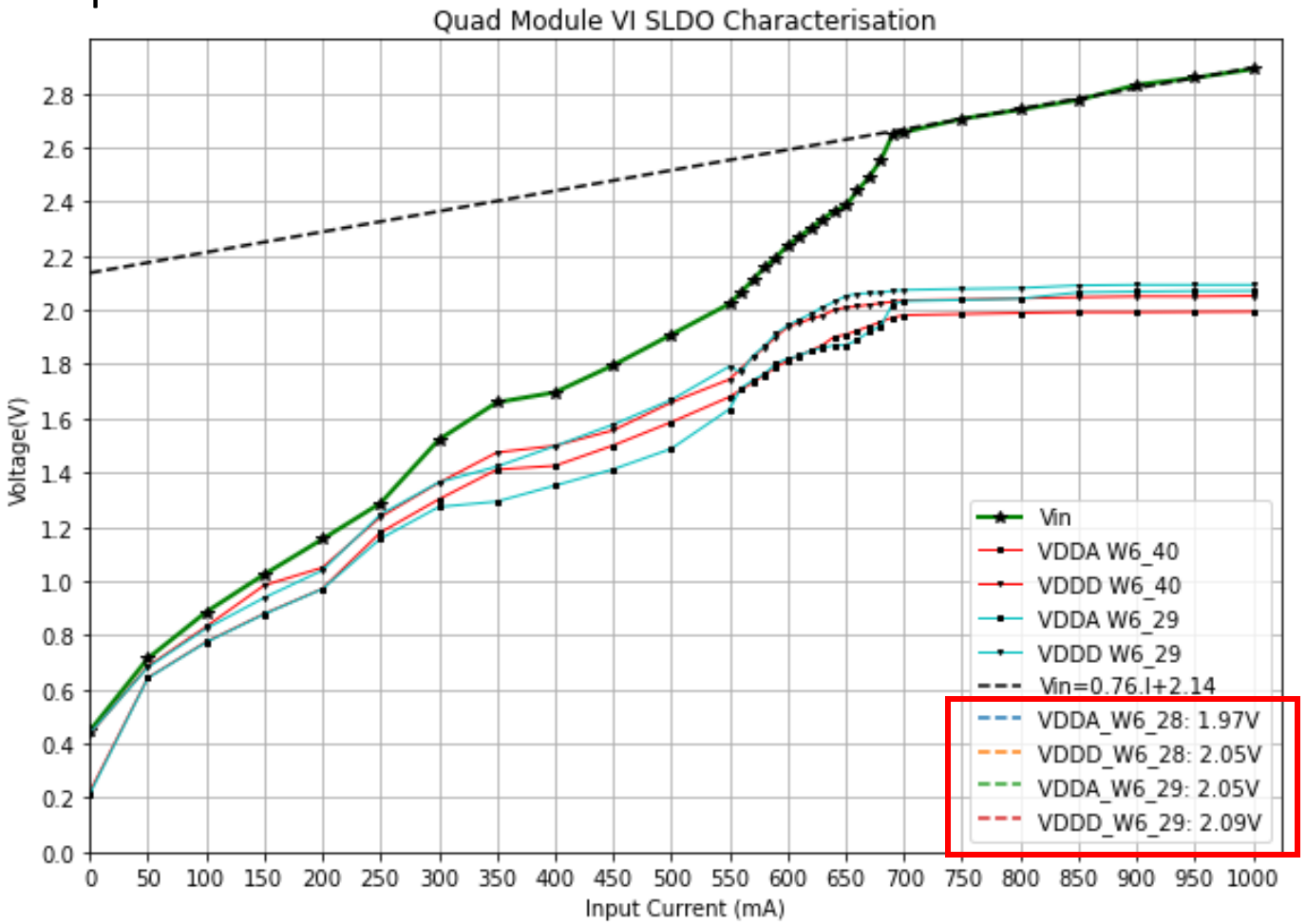


- Ohmic behaviour is seen after regulation starts.
- $\mathbf{V_{offset}}$ (the minimum required voltage to run the regulators) **2.27 V.**
- **Parasitic** resistance is **0.14 Ohm**.

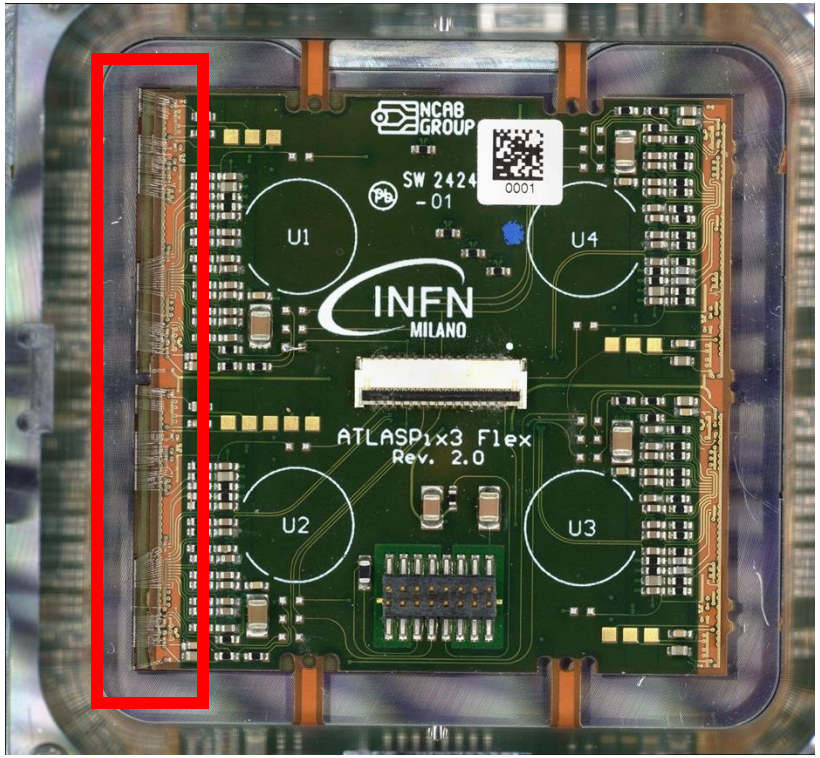


Quad Module-2 (IV Characteristics)

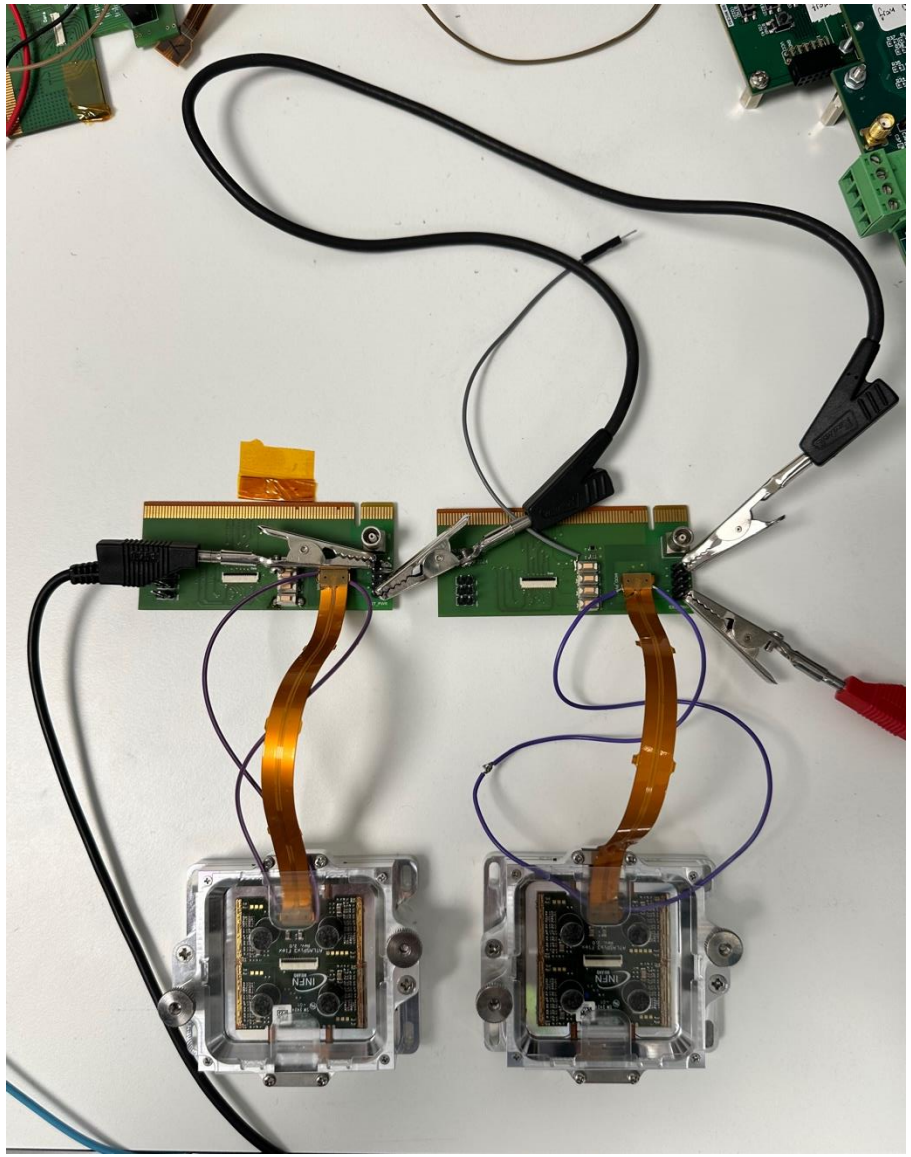
- The quad module-2 includes two wirebonded chips (**W6-28 & W6-29).**
- The input currents change between **640.75 mA and 703.96mA** as the regulation starts for each regulators on the chips.

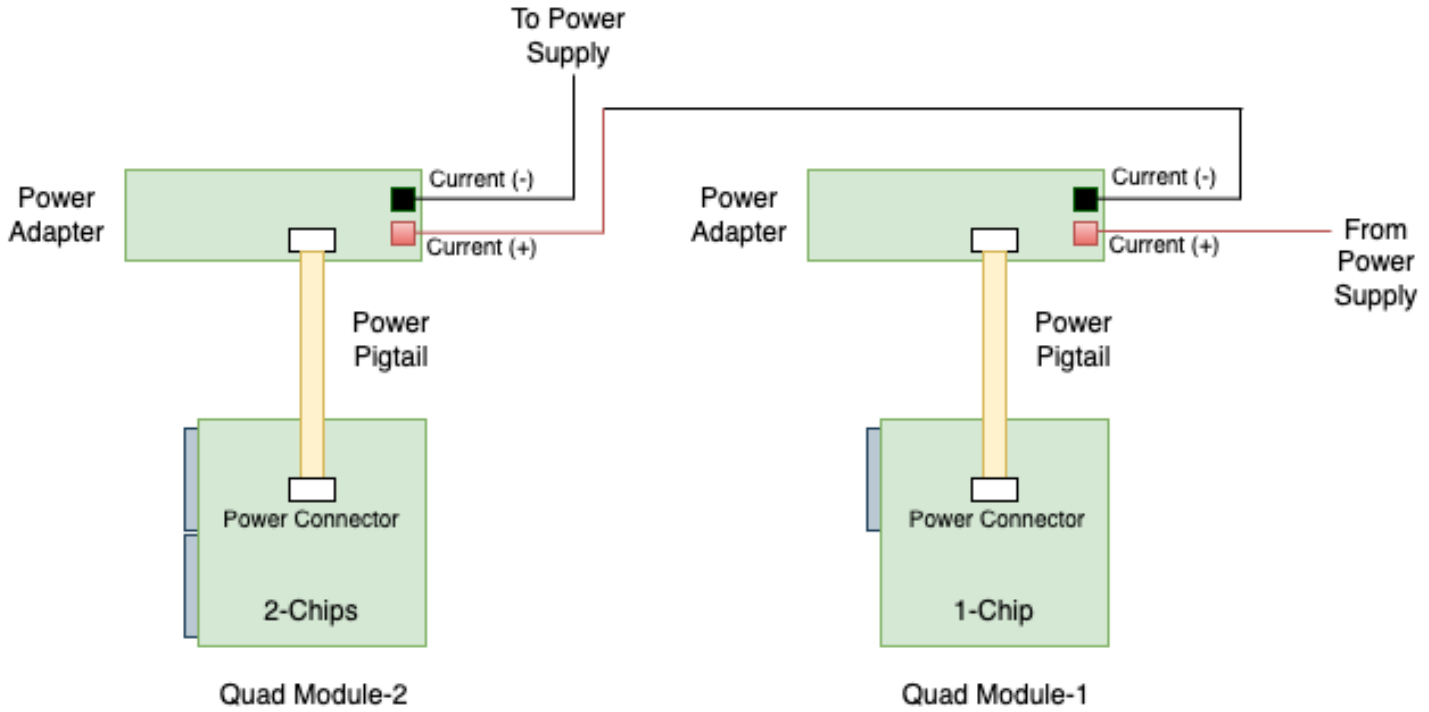


- Ohmic behaviour is seen after regulation starts.
- V_{offset} (the minimum required voltage to run the regulators) is **2.14V.**
- **Parasitic** resistance is **0.76 Ohm**.



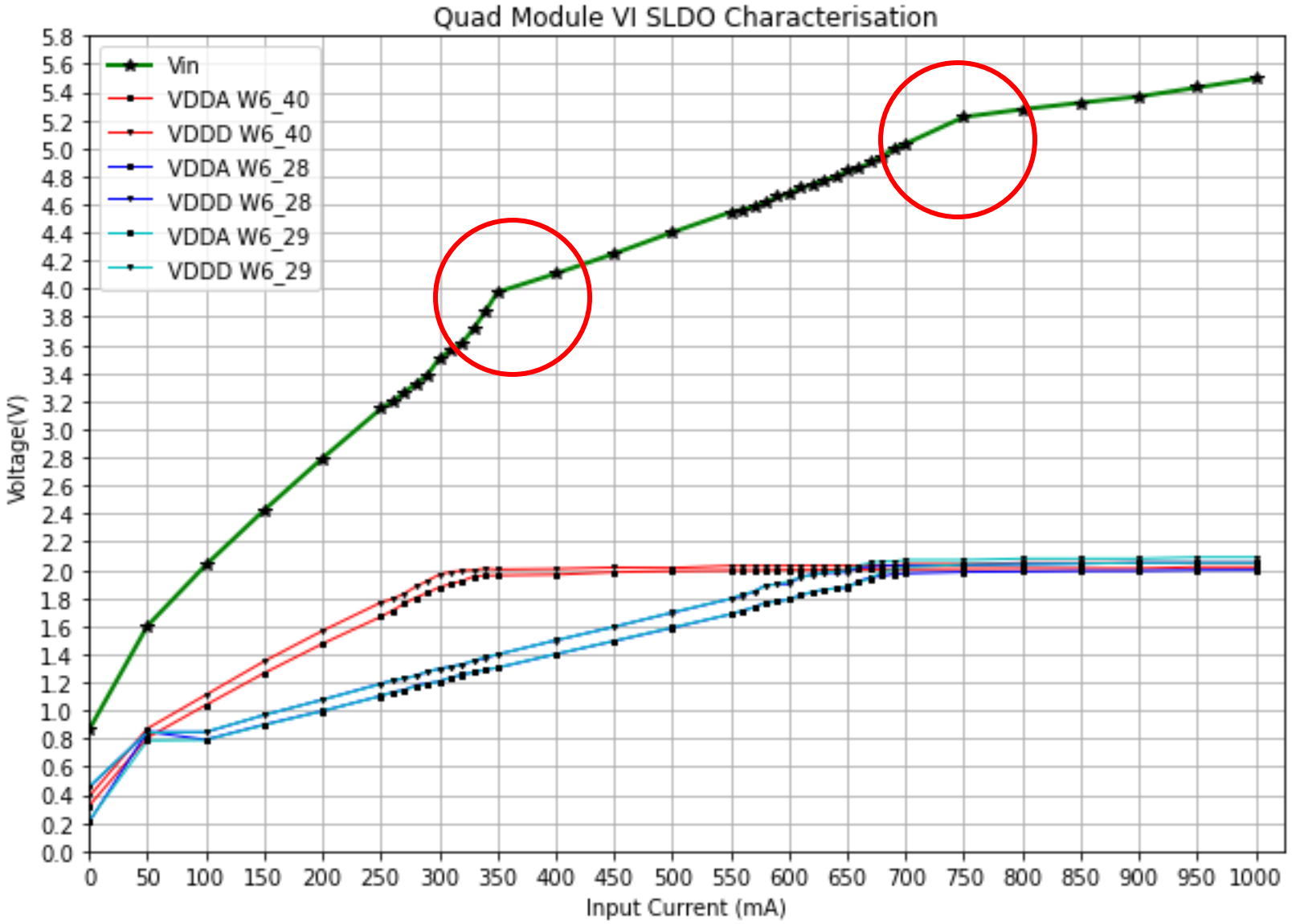
Serial Powering Chain with 2 Quad Modules





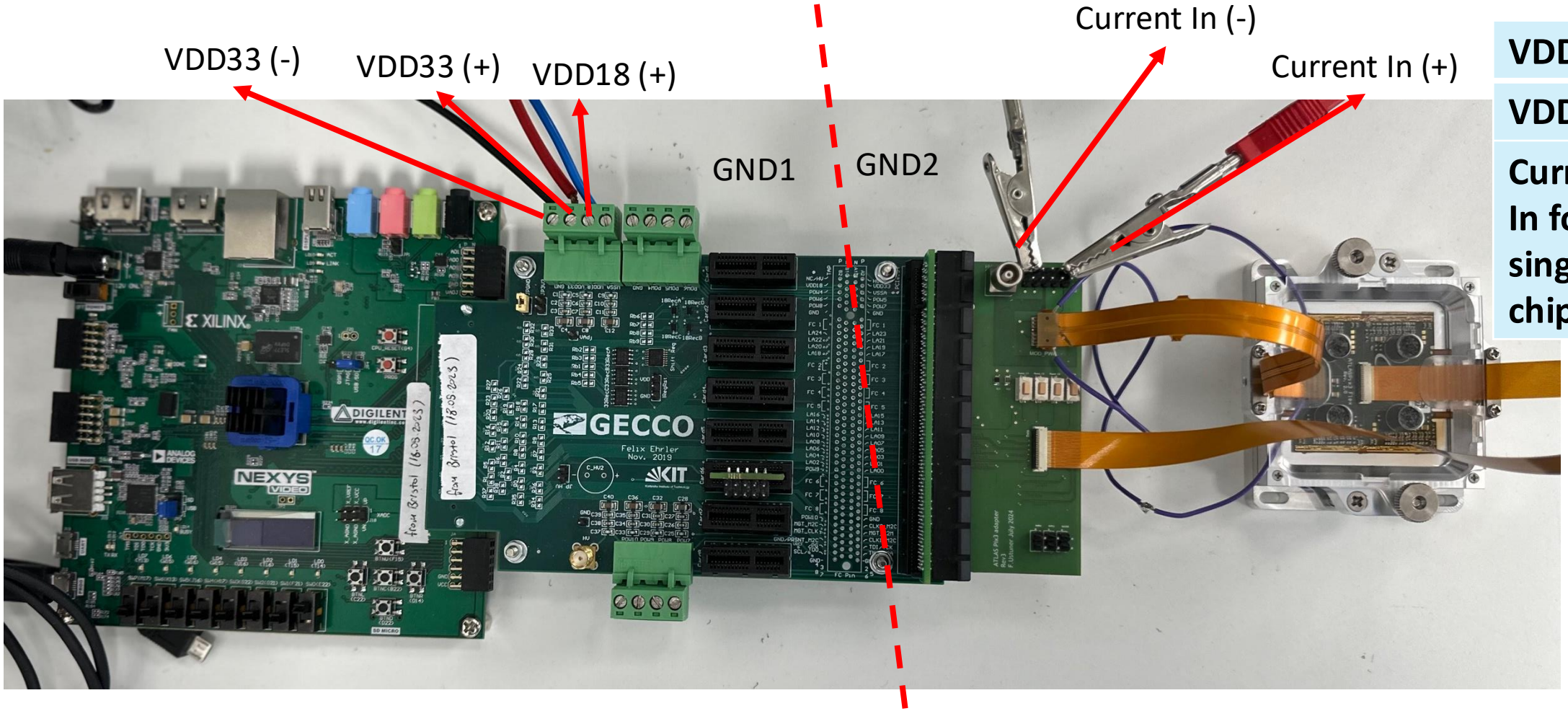
- Two quad modules are powered serial.
- One of them has just **one chip** while the other **two chips**.
- Aim:
  - The voltage regulation quality of the SLDOs in a quad module serial powering.
  - Mimic the failure of the one chip in the module.

Serial Chain with two Quad Modules



- The serial powering chain for two quad modules.
- Each quad module has an individual regulation process that begins for the **two Vin values** separately.
- **W6-40:**
  - VDDD = 1.99 V
  - VDDA = 1.965 V
  - @ 350 mA
- **W6-28:**
  - VDDD = 2.033 V
  - VDDA = 1.977 V
  - @ 703 mA
- **W6-29:**
  - VDDD = 2.045 V
  - VDDA = 2.01 V
  - @ 699 mA

ATLASPix3.1 Quad Module GECCO Readout DAQ



VDD33	**3.3V**
VDD18	**2.1V**
Current In for single chip	**~400mA**

- **CMD configuration** mode is used as slow mode.
- APix3.1 quad readout does not work out of the box with the same **software/firmware.**
- After debugging on **hardware/software/firmware**, the **we could configure the chip and readout.**

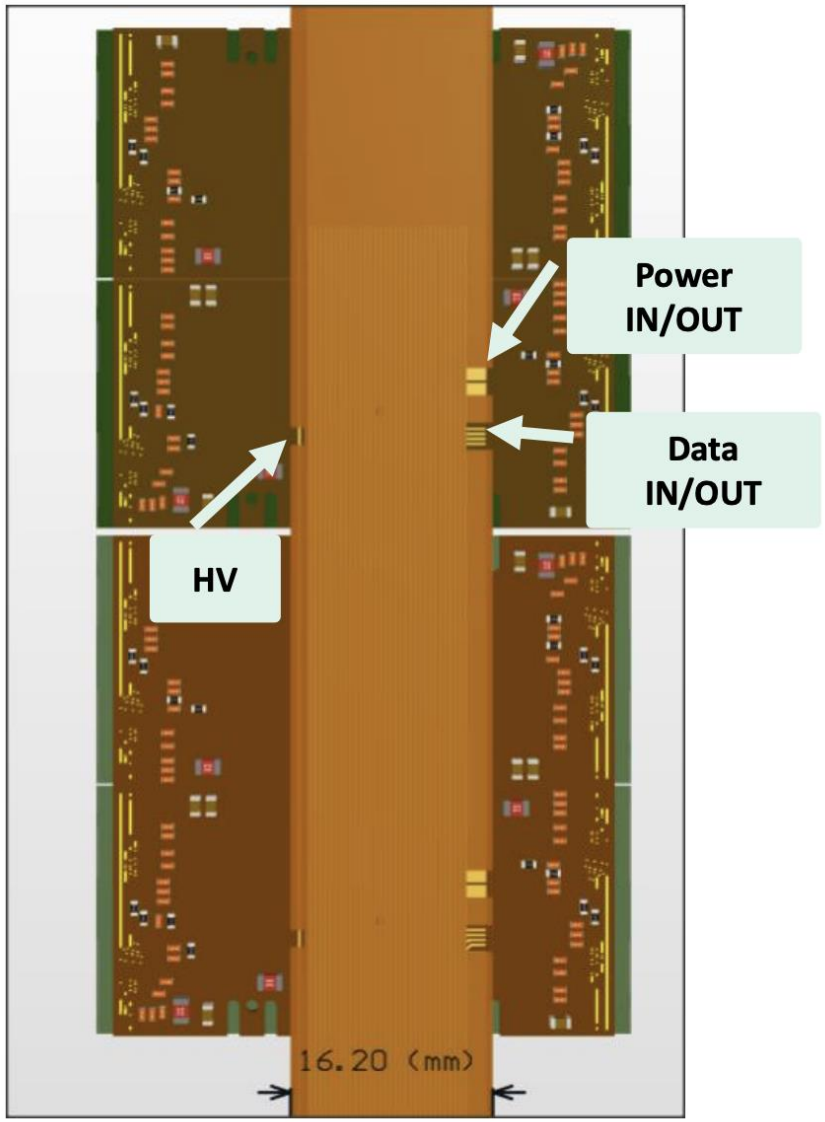
Summary & Further Plans (1)

- We tested the **electrical characterisation** to understand the responses of the ATLASPix3.1.
- The **source and beam tests** have been completed to see the irradiated environment responses of the chip.
- **ATLASPix3.1 Shunt-LDO regulators using KIT GECCO DAQ are tested**
  - The **regulators** are **working** as expected from **single-chip tests.**
- The shunt-LDO regulator performances are tested in different configurations:
  - **Quad module level.**
  - **In the serial powering chain.**
- The VDDD/A are regulated at chip operation level **(1.9V-2V)** for all configurations.
- The variation of the regulator outputs (VDDD/A) for each test setup is **=< 5 %.**
- The chips in the quad module can be **configured and readout via GECCO DAQ.**

Summary & Further Plans (2)

Next Steps:

- Assemble the full quad modules.
- Characterisation tests, including **S-curve analysis**, **threshold and noise distribution measurements**, and **full chip tuning**.
- Perform source tests using a serial chain, scaling up to at least three quad modules with current GECCO DAQ setup.
- **Prototype an SP chain with 2-3 quad modules integrated in a stave, including power and data distribution flexes and structural support.**



A. Andreazza, The IDEA Silicon Tracker. ICHEP 2024

Thank you!
Questions?

Backup

ATLASPix3.1 Quad Module Assembly Process

1) Flex verifications before assembly: Electrical characterisations and signal integrity tests on 5 differential lines

2) Bare Chip Probing using probe stations (no probe card)

3) Quad Base Production for Assembly Process

4) Dummy Flex Assembly

5) Gluing the Chip to the Quad Flex

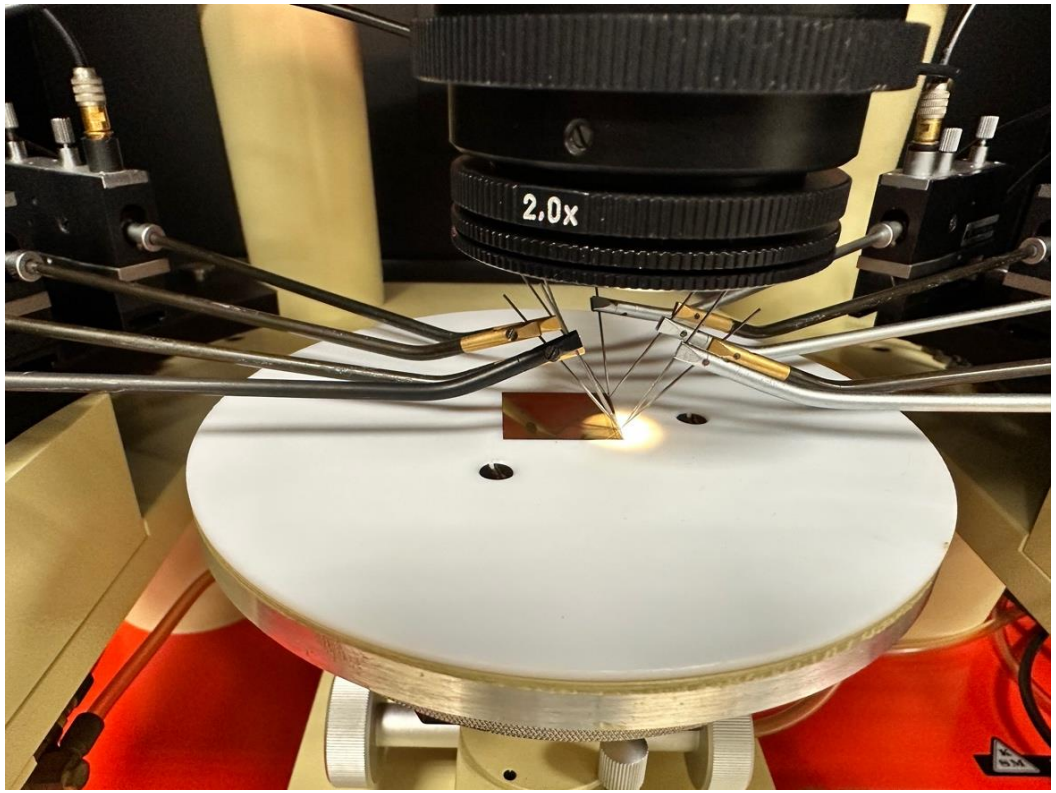
6) Basic Visual Inspection and Metrology Tests

7) Wirebonding the Chip

8) Powering Tests with Full Module

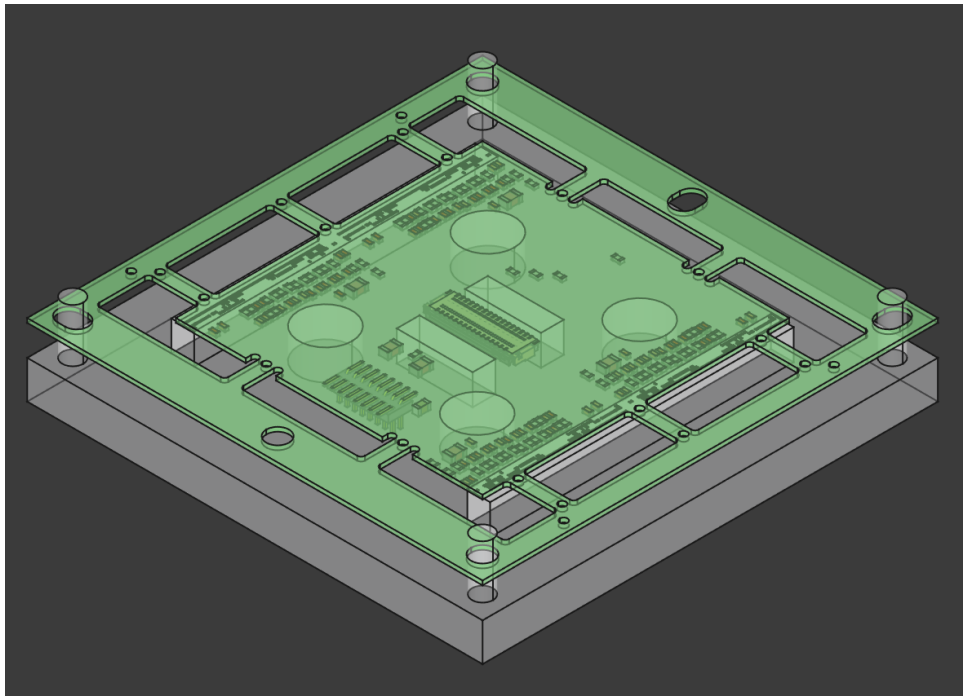
Chip Probe Testing

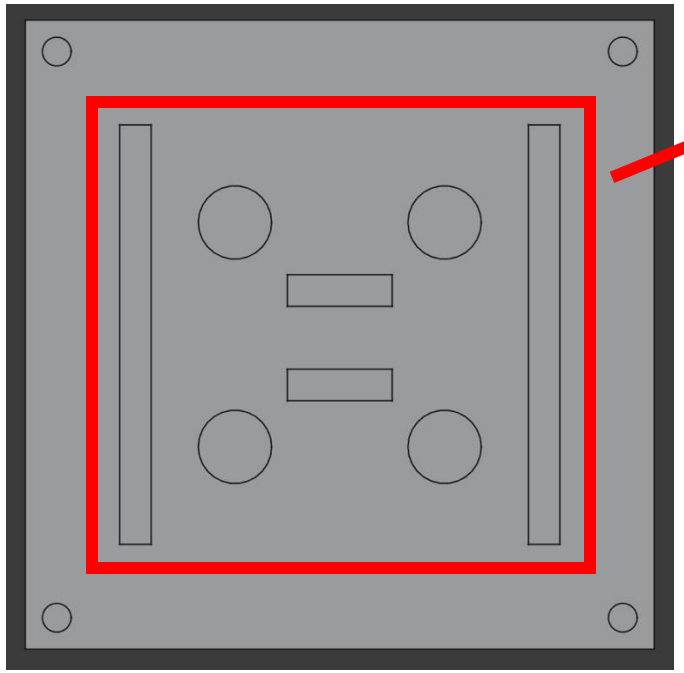
- Probe testing, at the individual chip level, is a key step in semiconductor manufacturing.
- Evaluates functionality and quality of individual ICs while still on the wafer.
- **Temporary electrical contact is made with test pads or contact points on each chip.**
- Electrical signals are sent through the probes.
- Aims:
  - Test electrical behaviour of **regulators**
  - Identify **potential defects and contaminations**



Quad Flex Base Production

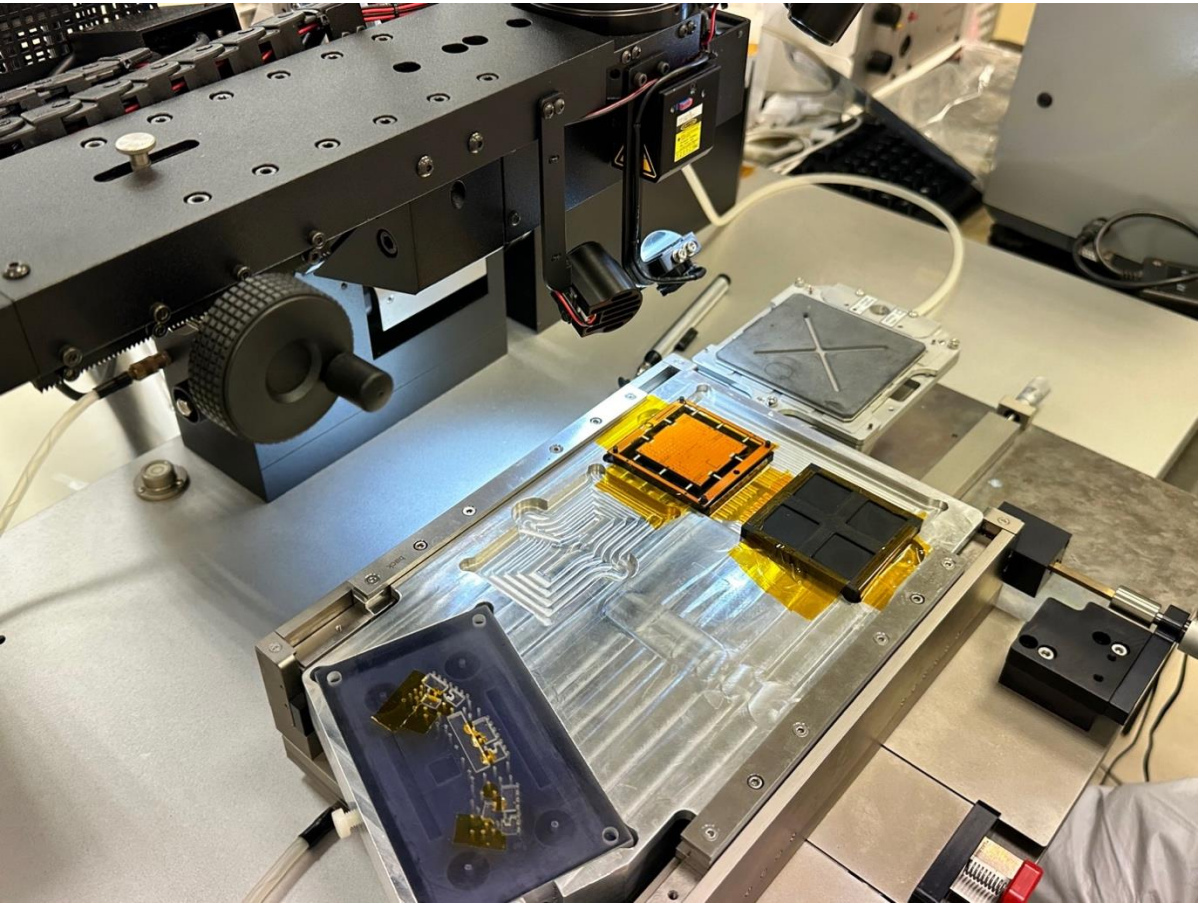
- For the further assembly process the base unit for the quad flexes should be produced.

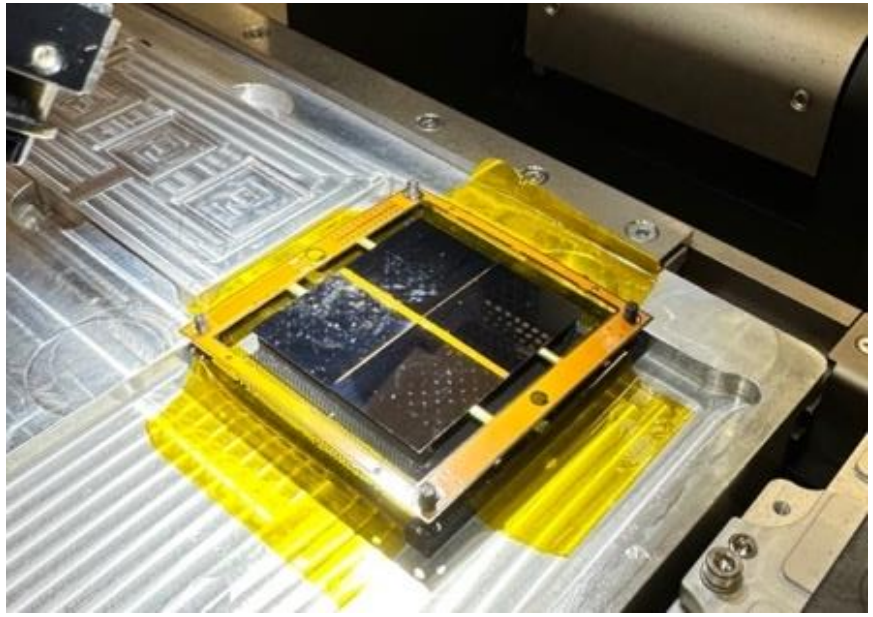




- This area secures the bare flex for stability during the assembly.
- 7 mm diameter columns for the four chip area and two 40x3 mm columns for wirebonding pads.

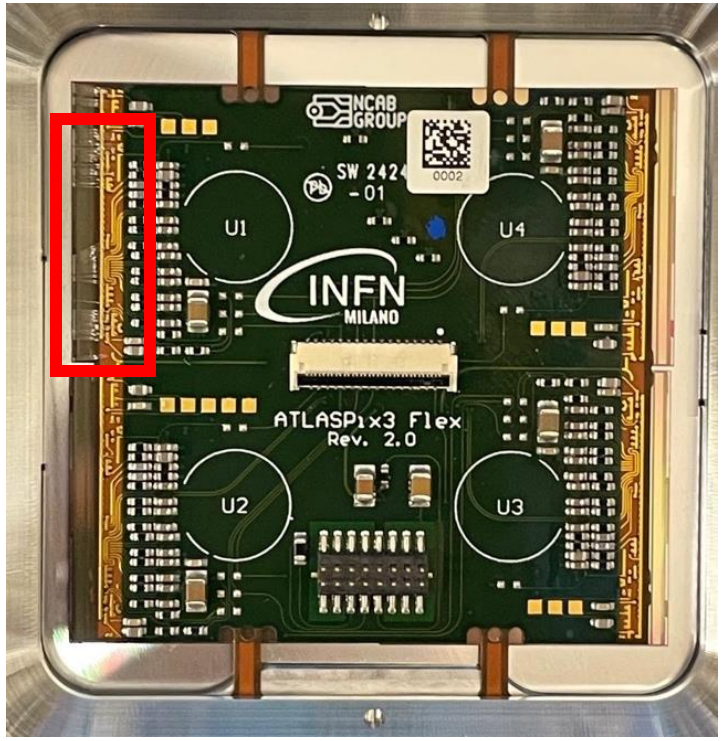
Gluing the Chip to Quad Flex



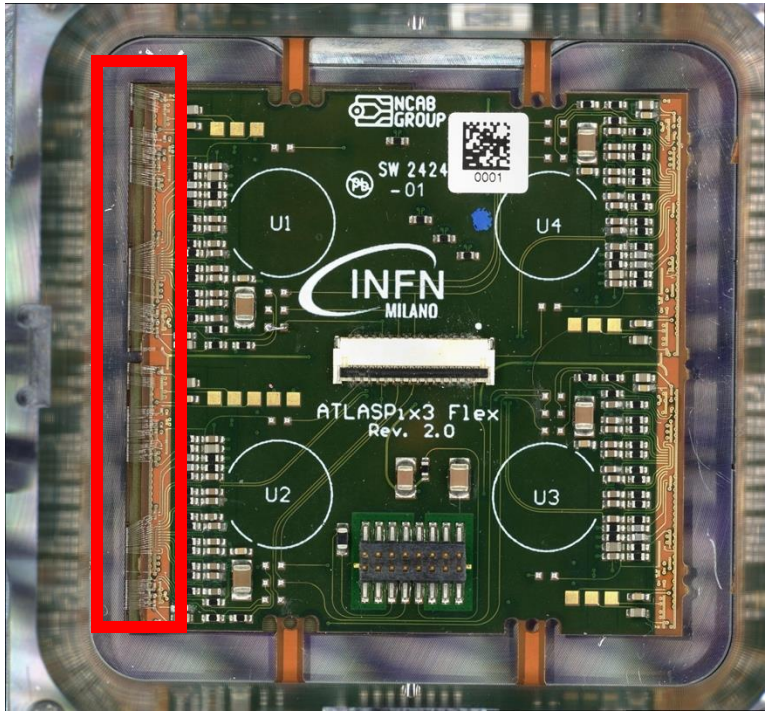


- The gluing process for four chip to the quad flex is presented in these figures.
- The pick and place machine is operated for this step.

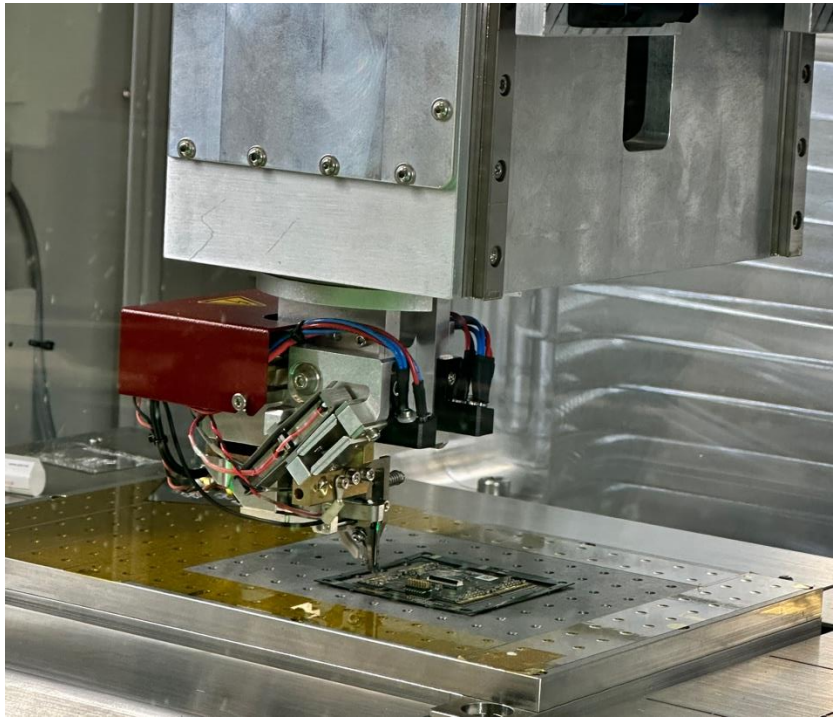
Chip Wirebonding to Quad Flex Assembly



Quad module-1



Quad module-2



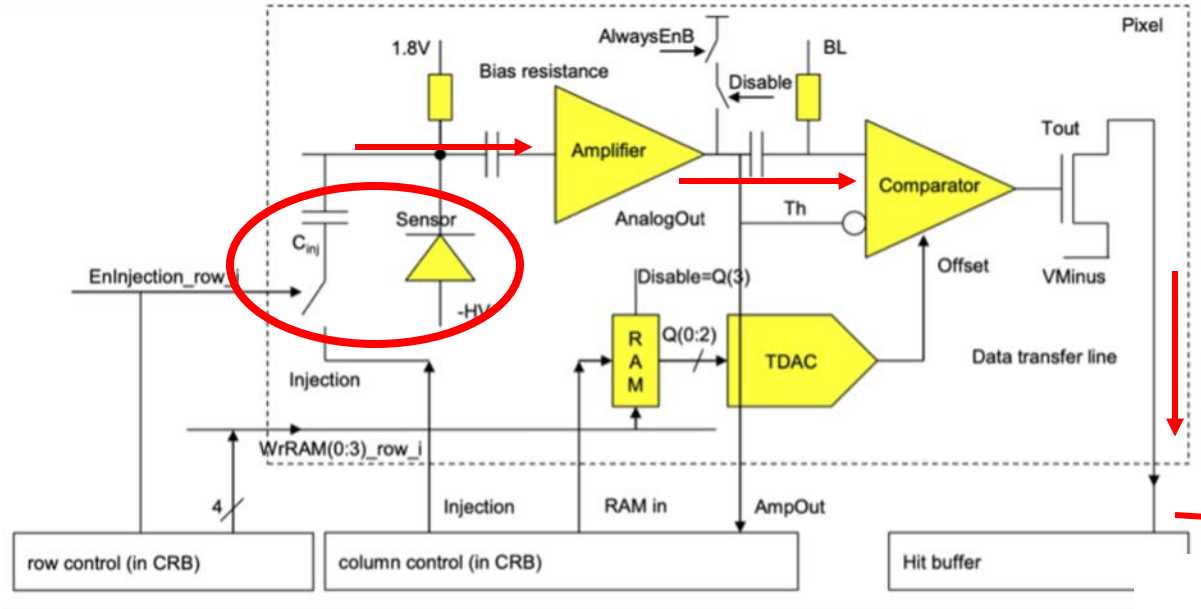
- Two quad modules are wirebonded:
  - Quad Module-1: **Chip1 - W6-40**
  - Quad Module-2: **Chip1 - W6-28** and **Chip2 - W6-29**

Comparison of the each test setup

Chip	Voltage	Probing Tests	In a Quad Module	Serial Chain	Variation (%)
W6-40	VDDA	N/A	1.93 V	1.965 V	**1.81 %**
	VDDD	N/A	1.97 V	1.99 V	**1.02 %**
W6-28	VDDA	2.06 V	1.97 V	1.977 V	**4.49 %**
	VDDD	2.14 V	2.05 V	2.033 V	**5.01 %**
W6-29	VDDA	2.07 V	2.05 V	2.01 V	**2.91 %**
	VDDD	2.04 V	2.09 V	2.045 V	**2.45 %**

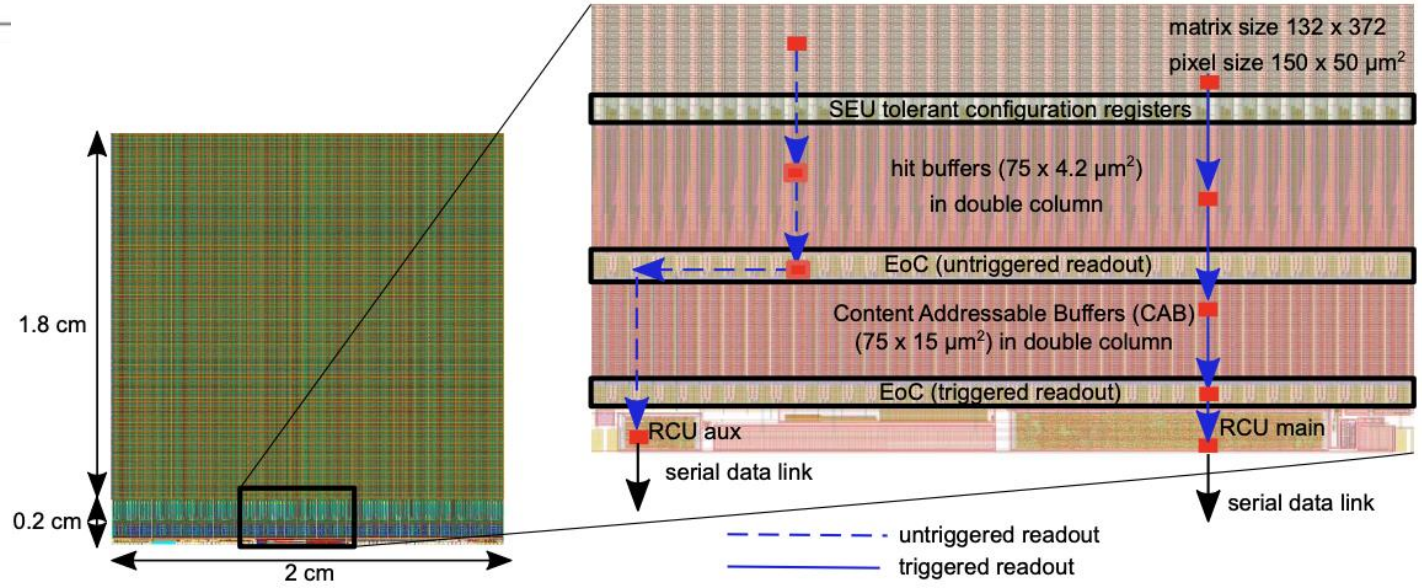
- The variation of the regulator outputs (VDDD/A) for each test setup is **=< 5 %.**
- The regulators can supply the voltage value for analog and digital circuits of the chip in the quad module and the serial powering chain.
- A test was done to mimic a failed chip in the serial powering chain.

ATLASPix3.1



- Sensor (sensitive area)
- Charge Sensitive Amplifier (CSA)
- Comparator
- 3-Bit Threshold tune DAC
- Pixel-out

- Hit buffers (one per pixel)
- End of Columns (EoCs)
- Content Addressable Buffer (2x40)
- **Triggered and triggerless** readout



ATLASPix3.1 Quad Module Readout