THE UNIVERSITY *of* EDINBURGH

HV-CMOS pixel tracking detector R&D for future collider experiments

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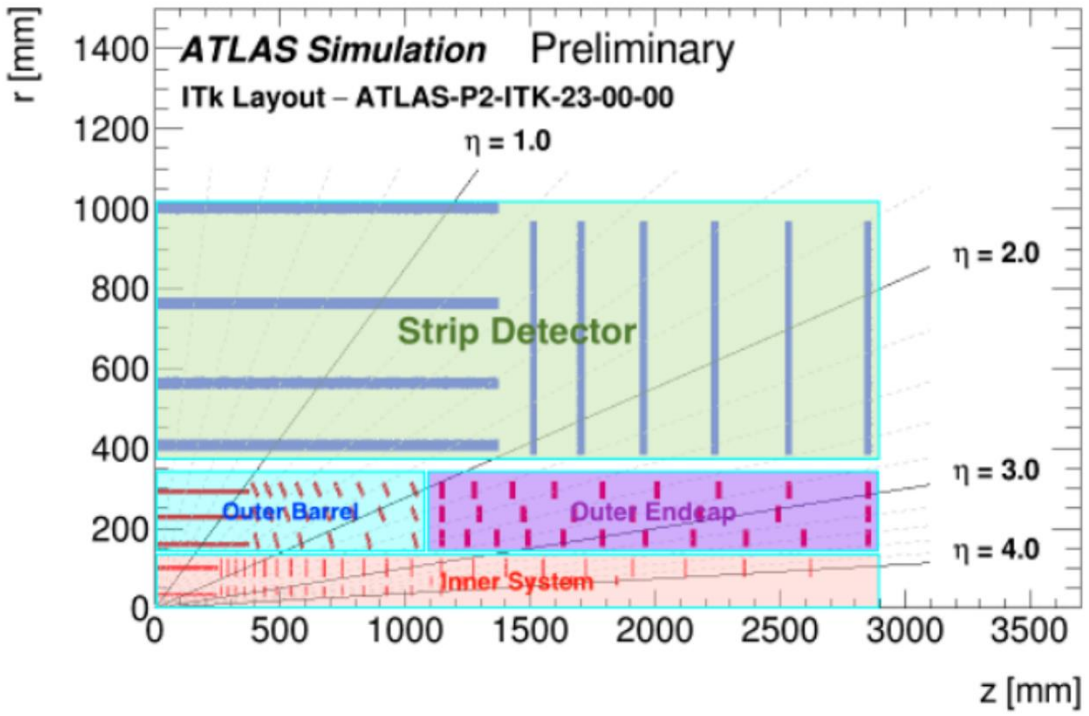
08.07.2025

All IPNP meeting, 08/07/2025

Silicon as a Tracking Device

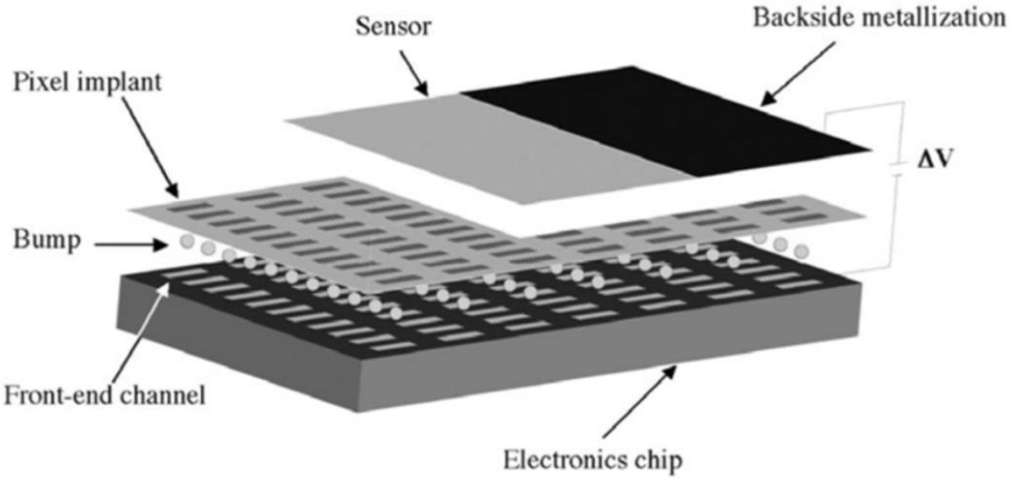


- Silicon is the most common material for collider-based experiments as a tracking detector.
- The combination of well-suitable properties for charged particle detection.
- Examples of silicon-based tracking detectors from,
  - **ATLAS ITk upgrade (pixel area ~14m^2)**
  - **Mighty Tracker Upgrade (~15m^2)**
  - **Future experiments:**
    - **IDEA (~100m^2) for FCC-ee and CEPC**

Pixel Detectors in Particle Physics

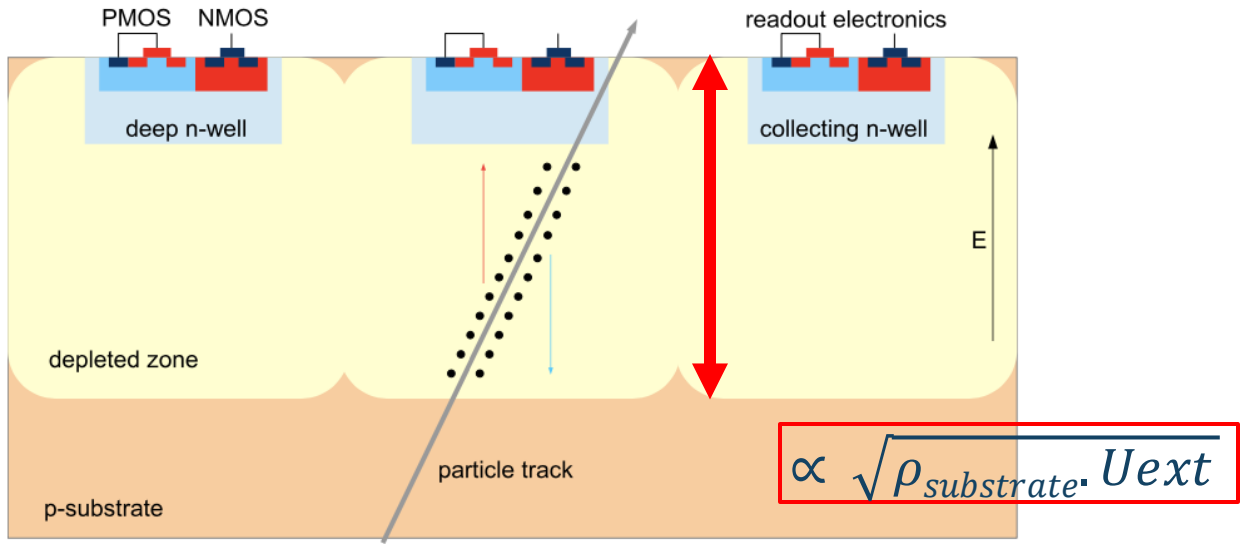
Hybrid-pixel detectors:

- ITk upgrade
- Some limitations:
  - **Cost (High):**
  - **Construction process is complex**
  - **Large amount of material**



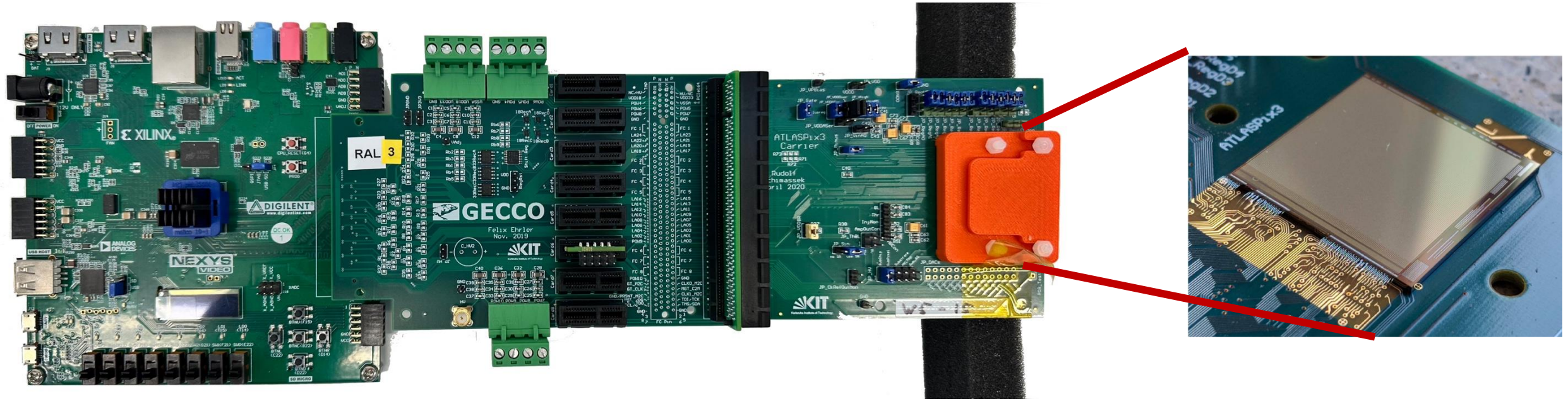
HV-CMOS:

- offers promising **solutions** to address **some of the limitations.**
- The electronic readout and active area are in **the same silicon die**. (monolithic).
  - Production cost (low) → No hybridisation
  - A much simpler assembly procedure



H. Spieler, Semiconductor Detector Systems. Oxford, U.K.: Oxford Univ. Press, 2005
Peric et al., High-Voltage CMOS Active Pixel Sensor, 2021

ATLASPix3.1 and GECCO DAQ

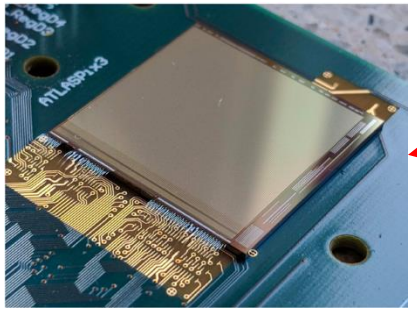


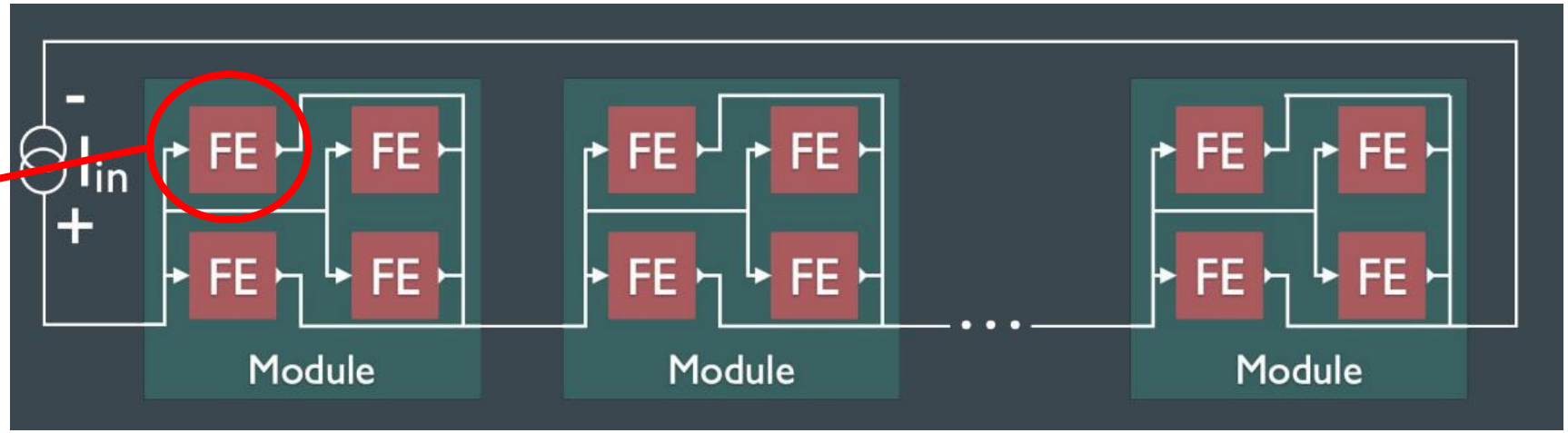
HV-CMOS Technology	TSI 180nm
Substrate [Ωcm]	200
Matrix [pixel]	132x372
Pixel Pitch [µm²]	50x150
Sensor size [mm²]	20.2x21

- The first full size monolithic HV-CMOS sensor including two fully functional **shunt low-dropout regulators**. → Serial Powering
- The breakdown voltage is ~-65 V (unirradiated)
- Each pixel has a custom design readout circuitry.
- Each column has a digital FE.

System Scale and Serial Powering (SP)

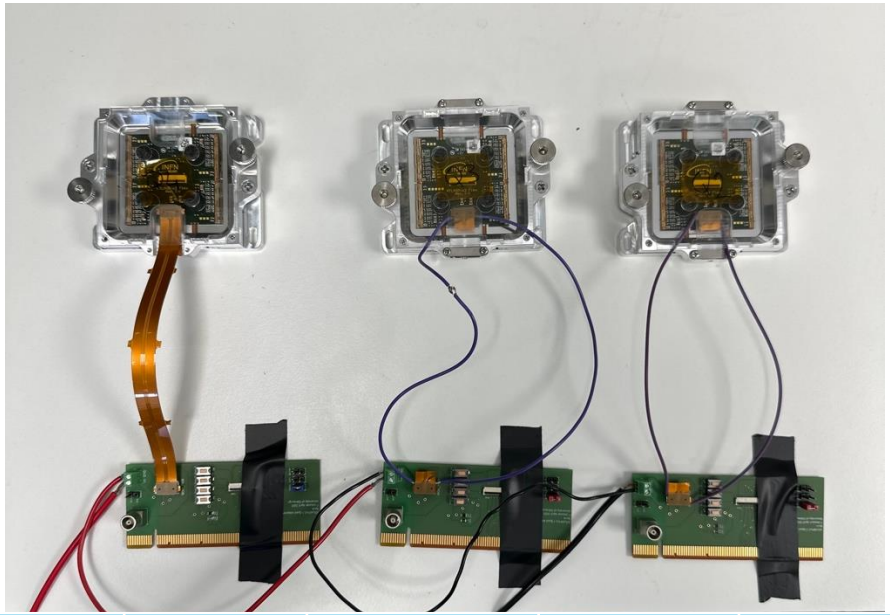
- System readout challenge: scale 1 -> $2x10^5$ sensors
  - Data aggregation is usually implemented to minimize services (power/data lines)
    - Leads to multi-chip modules (e.g. quad module in ITk) usually powered in parallel
  - Serial Powering, where all modules in a local structure are powered via **constant current**
- SP is developed and verified for **ATLAS and CMS** pixel upgrade LS3 using **hybrid pixel detectors**.
- **However, this has not been studied for HV-CMOS-based pixel detectors.**



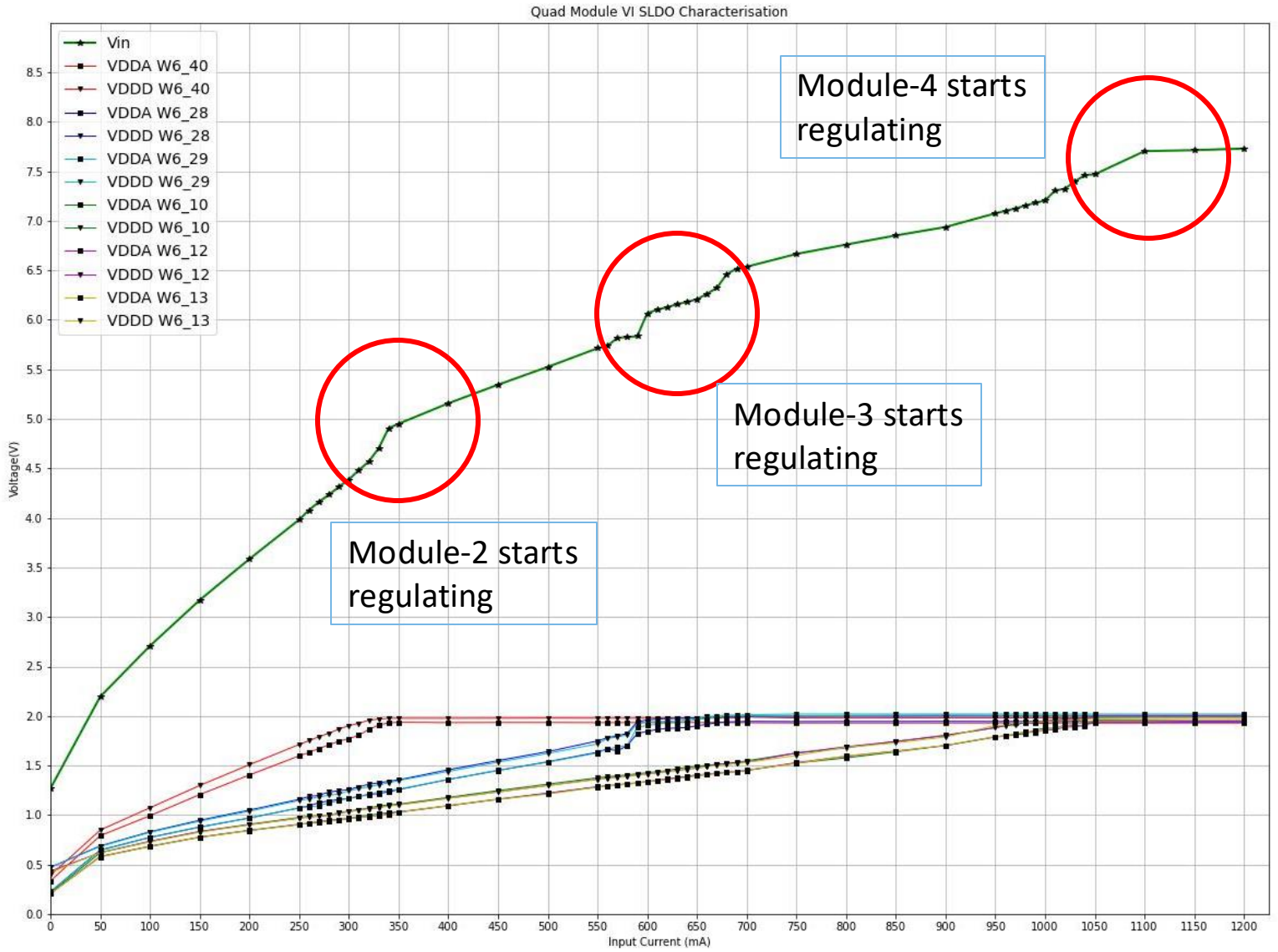


J. Chan, Serial Powering of ATLAS ITk Pixel Modules

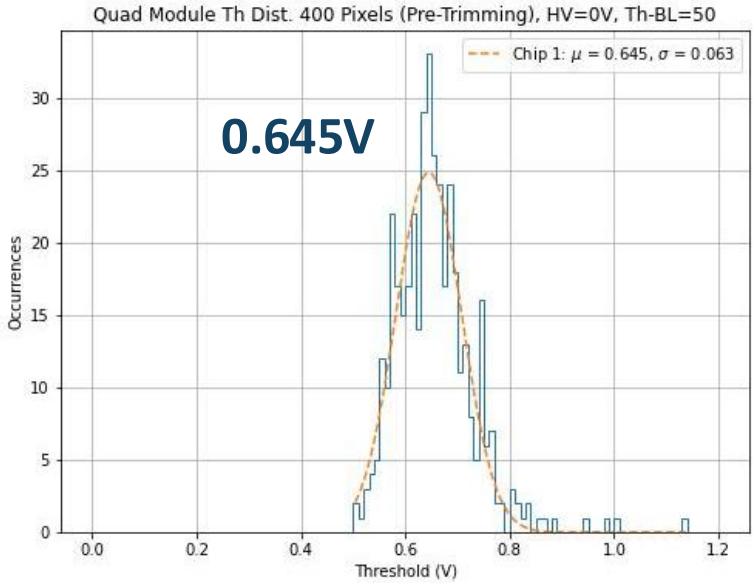
Serial Powering Chain with 3 Quad Modules



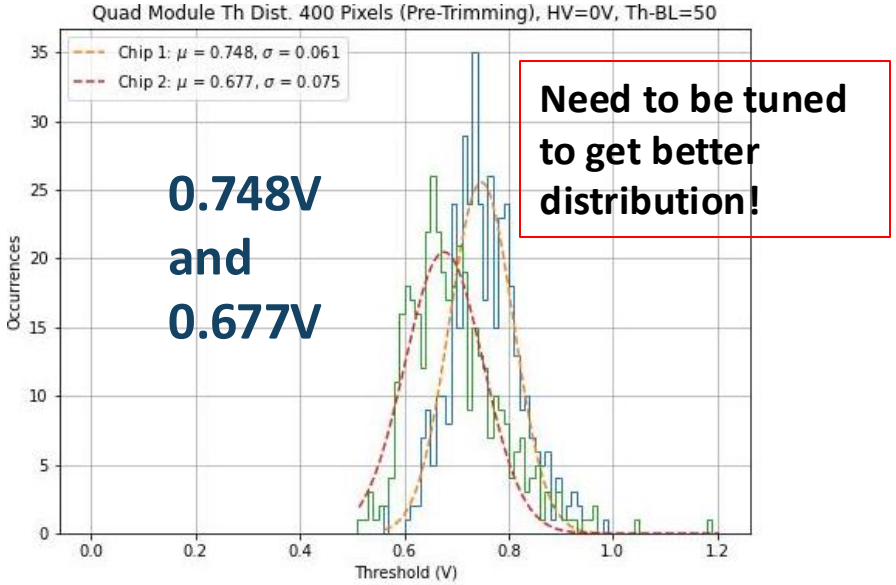
	Chip	Current	VDDD	VDDA
Q-2	W6-40	350 mA	1.98 V	1.93 V
Q-3	W6-28	703 mA	2 V	1.946 V
	W6-29	699 mA	2.01 V	1.99V
Q-4	W6-10	1040 mA	2.02 V	1.97 V
	W6-12	1048 mA	2 V	1.937 V
	W6-13	1052 mA	1.981 V	1.96 V



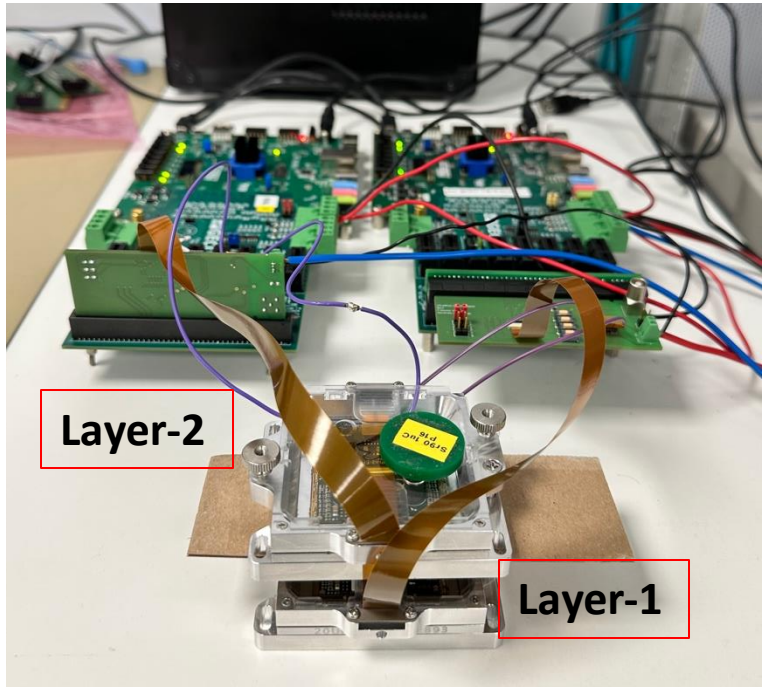
Threshold Scan (Untuned) & Sr90 Measurement

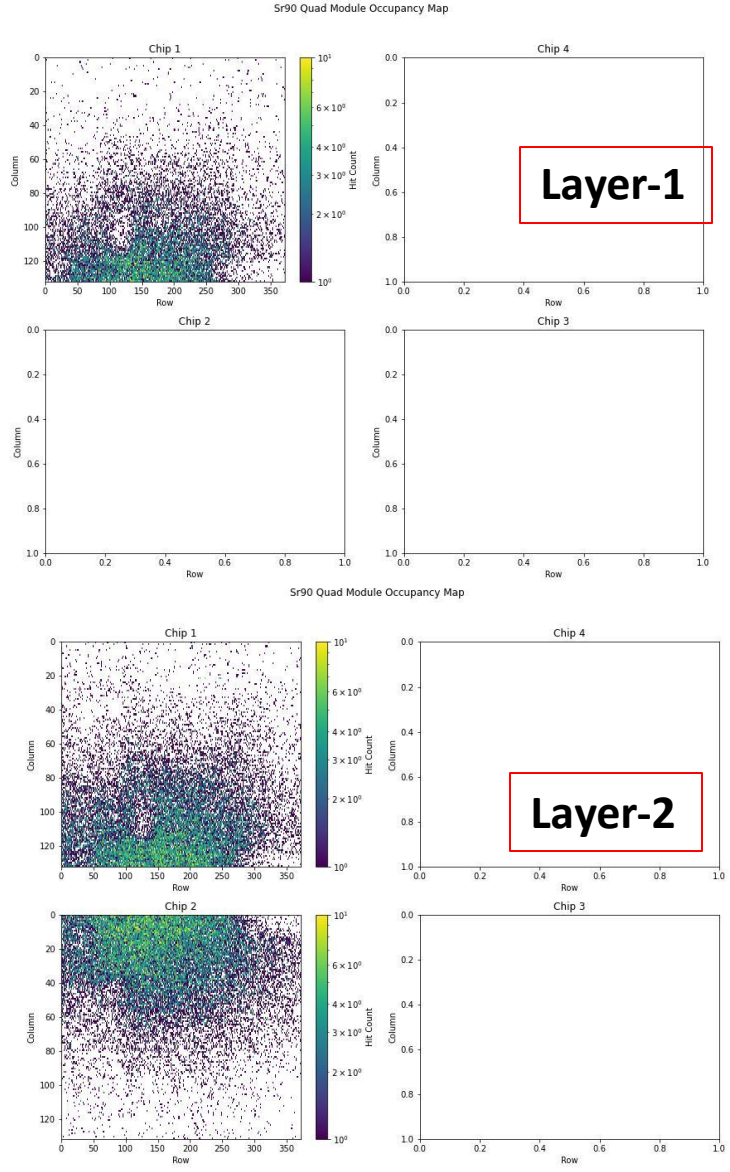


- **400** pixels are used. (10-29 / 150-169).
- **TDAC=4**, and global threshold DAC is **50**.



Need to be tuned to get better distribution!

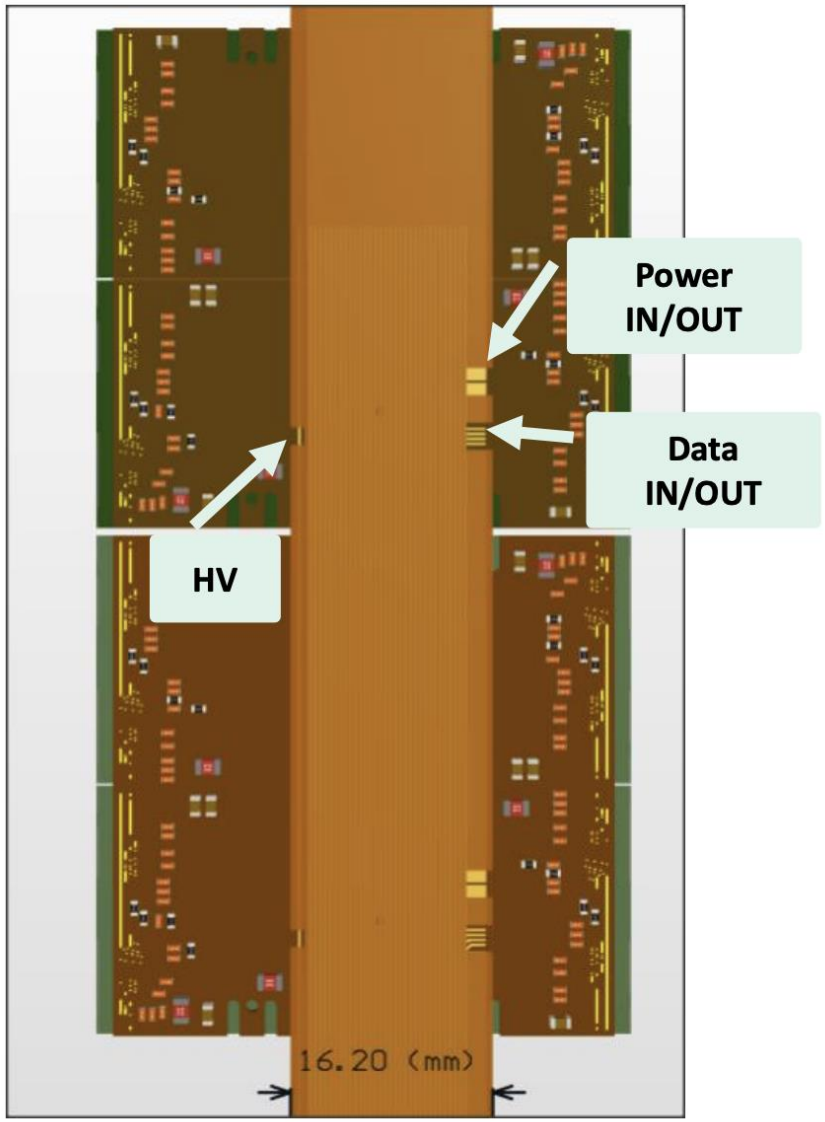




Next Steps

Next Steps:

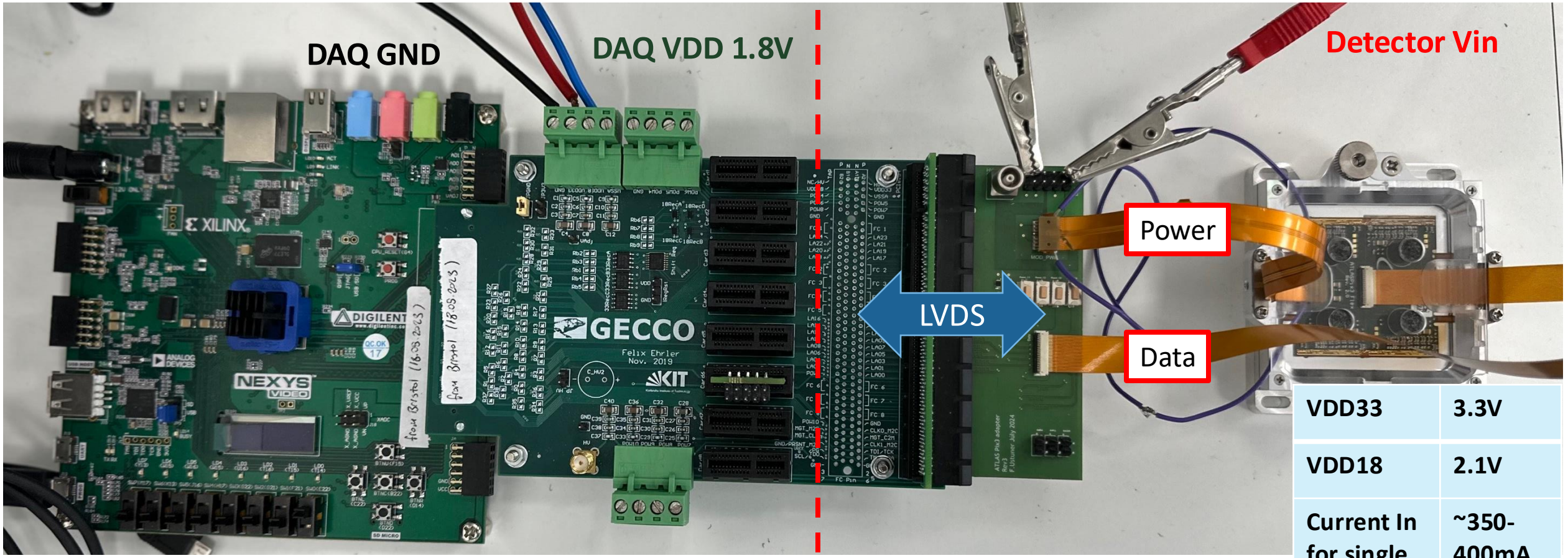
- Supplying the HV for measurements.(near term)
- Expand SP setup to include more chips/modules. (near term)
- **Prototype an SP chain with 2-3 quad modules integrated in a stave, including power and data distribution flexes and structural support.**



A. Andreazza, The IDEA Silicon Tracker, ICHEP 2024

Backup

ATLASPix3.1 Quad Module GECCO Readout DAQ



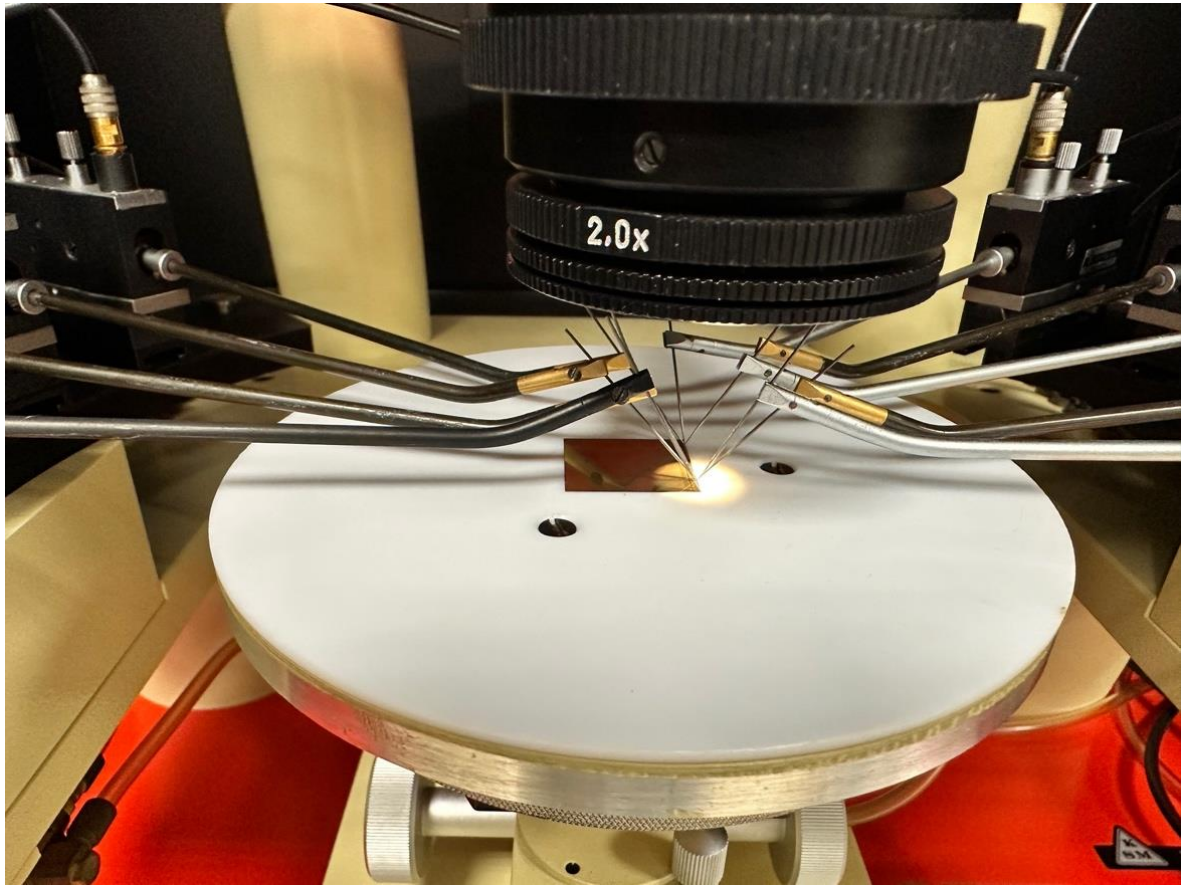
VDD33	3.3V
VDD18	2.1V
Current In for single chip	~350-400mA

- **GECCO**, flexible readout system developed by **KIT**
- **Power adapter** is splitting the power domains.
- LVDS signals are **decoupled** on flex.

- **Firmware and software adapted for quad module operation**
- **CMD configuration** mode is used **at 160 MHz**.

Chip Probe Testing

- Probe testing, at the individual chip level, is a key step in semiconductor manufacturing.
- Evaluates functionality and quality of individual ICs while still on the wafer.
- **Temporary electrical contact is made with test pads or contact points on each chip.**
- Electrical signals are sent through the probes.
- Aims:
  - Test electrical behaviour of **regulators**
  - Identify **potential defects and contaminations**



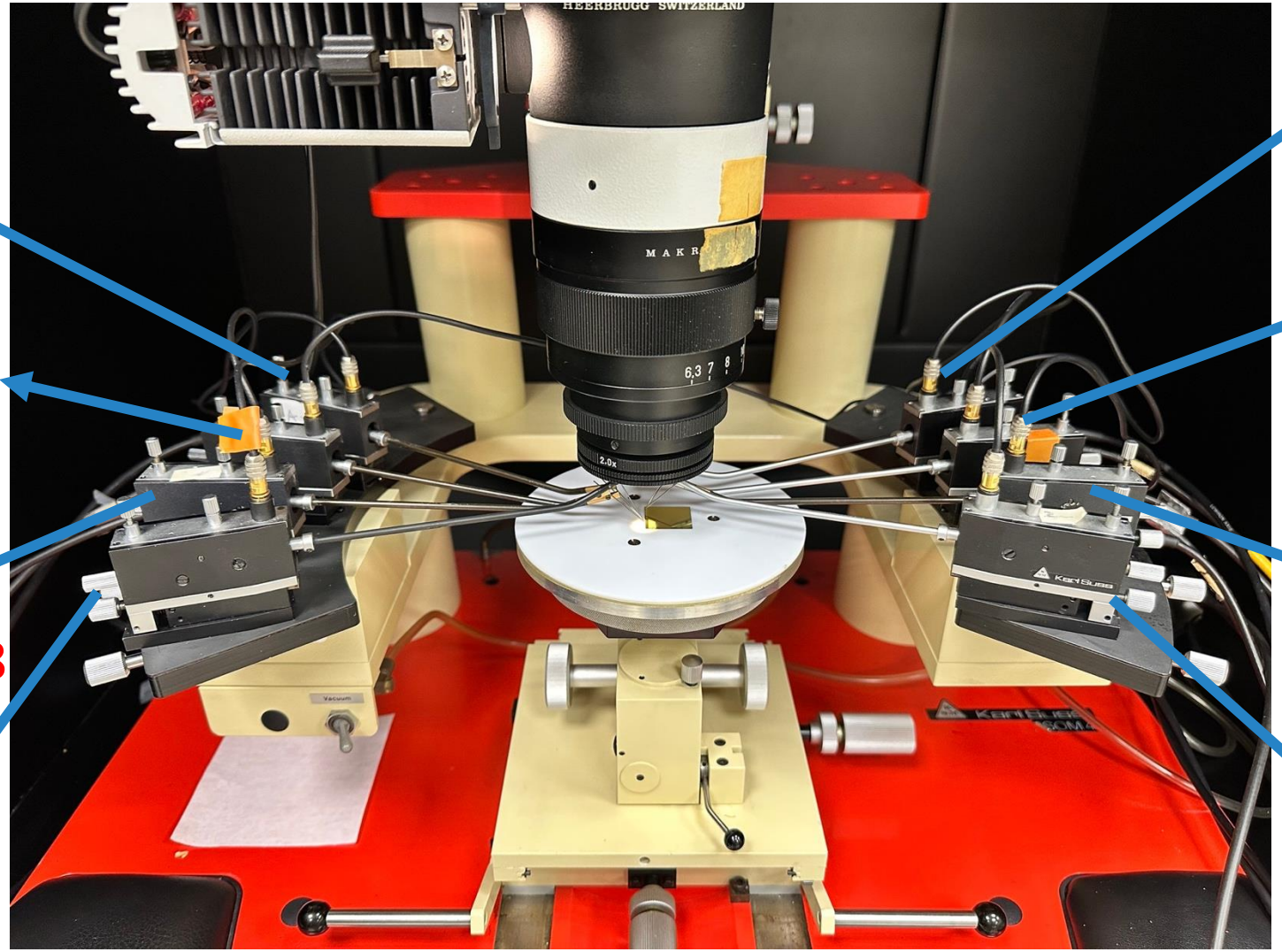
Probe Testing Setup at Milan

VDDA2 in, Pad-104
GNDD, Pad-116

VDDA2 out, Pad-106
VDDD2 in, Pad-117

Vina2, Pad-108
VDDD2 out, Pad-118

GNDA, Pad-110
Vind2, Pad-119



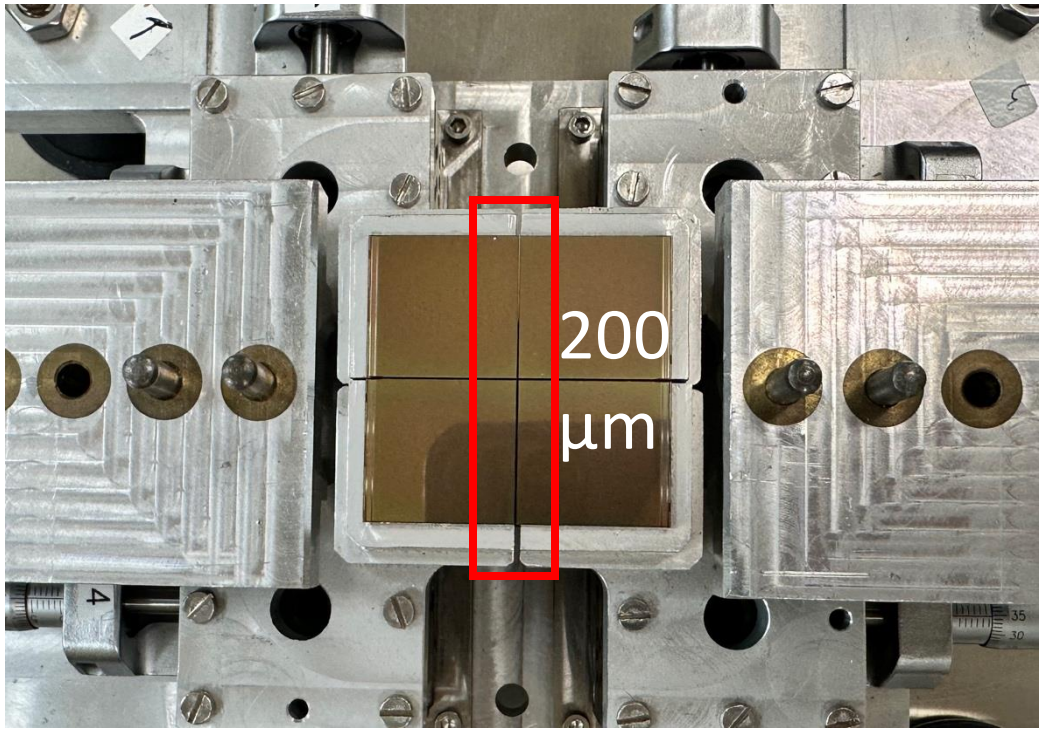
VDDA1 in, Pad-24
GNDD, Pad-39

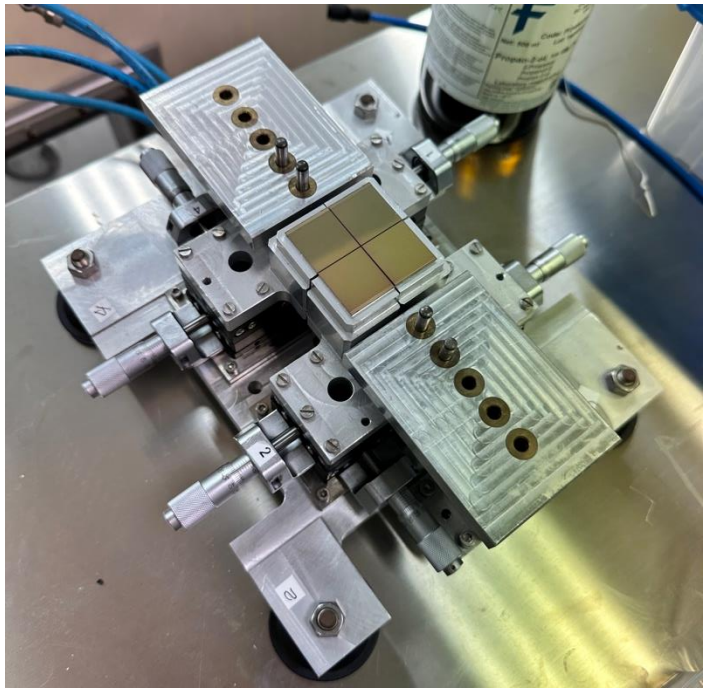
VDDA1 out, Pad-26
VDDD2 in, Pad-40

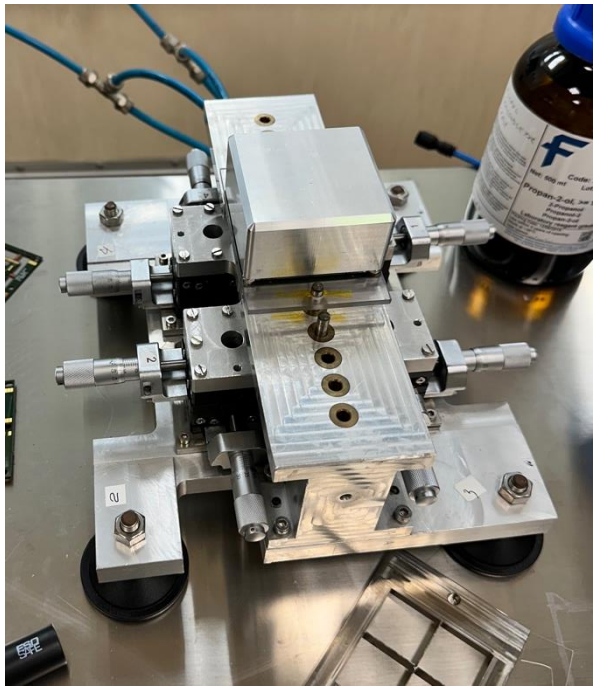
Vina1, Pad-28
VDDD2 out, Pad-41

GNDA, Pad-30
Vind2, Pad-42

Gluing the Chip to Quad Flex

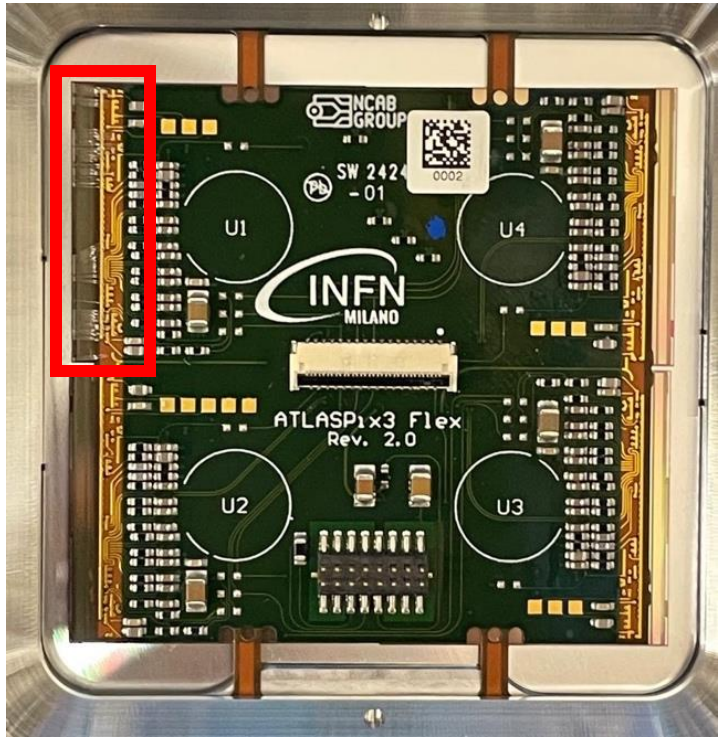




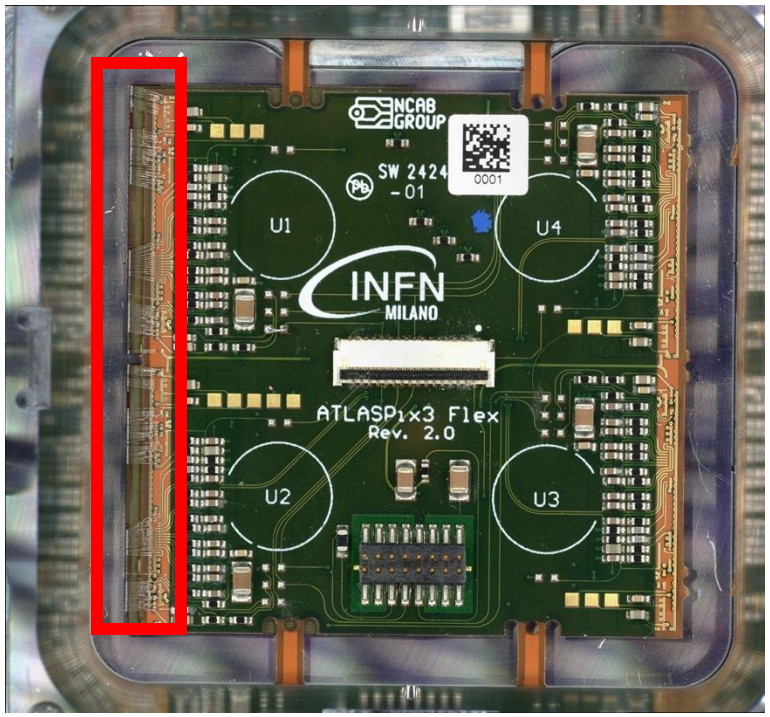


- The **assembly tool** is used to mount the chips onto the quad flex.
- This tool ensures **precise alignment and positioning** of the chips onto the quad flex.
- The inter-chip spacing at the **center** is maintained at **200 µm**.
- After gluing, a weight (300g) is applied to the module for at **least 5 hours.**

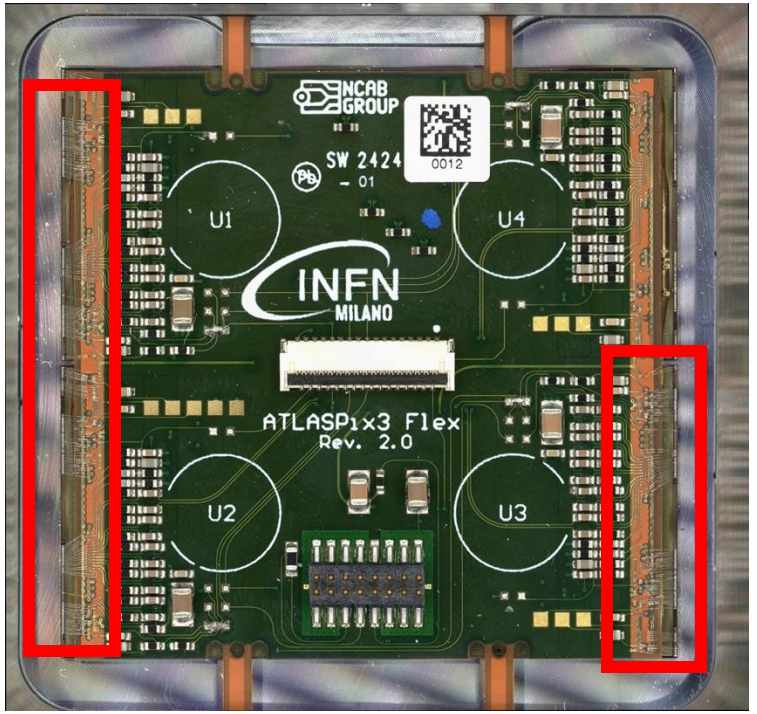
Assembled “Quad” Modules



Quad module-2



Quad module-3

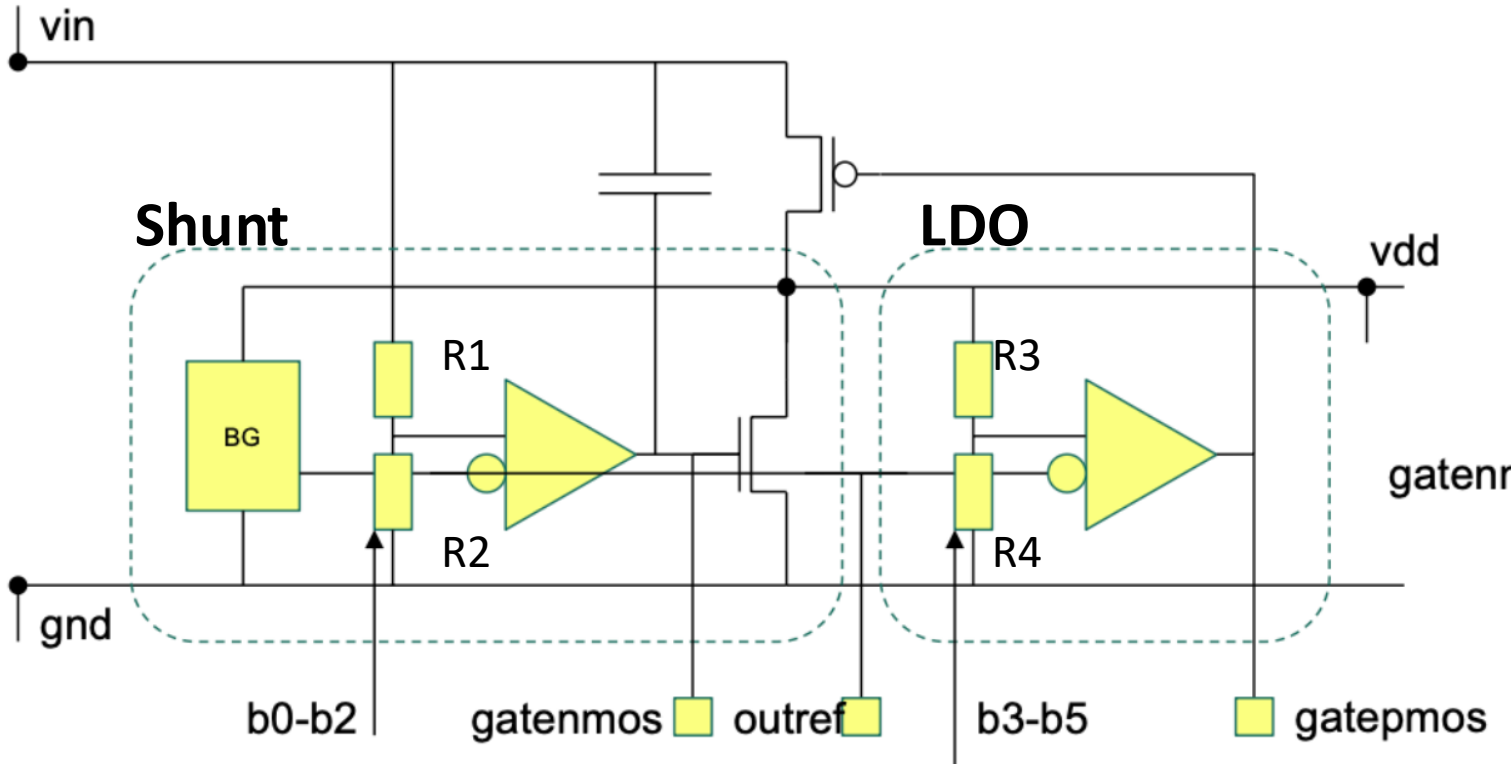


Quad module-4

- In total 5 quad-modules are assembled, 3 are in Edinburgh for SP and multichip studies
  - Quad Module-2: **Chip1 - W6-40,**
  - Quad Module-3: **Chip1 - W6-28** and **Chip2 - W6-29**
  - Quad Module-4: **Chip1 - W6-10, Chip2 - W6-12, Chip3 - W6-13 and chip4 - W6-14 (chip4 couldn’t be bonded)**
- **The wirebonding process time is around an hour per chip, and ~4 hours for one module (in best case scenario).**

Shunt-LDO Regulators on ATLASPix3.1

- ATLASPix3.1 can be powered via a **single constant current** with two shunt-low dropout regulators.
  - **Digital &Analog (VDDD/A)**
  - 3-bits to **tune threshold** of the shunt regulator
  - 3-bits to **tune VDDs**
- **Vin** is created from constant current via regulators.
- **VDDD/A** presents the **regulated voltage** (output of the shunt-LDOs) to use the chip for operation.

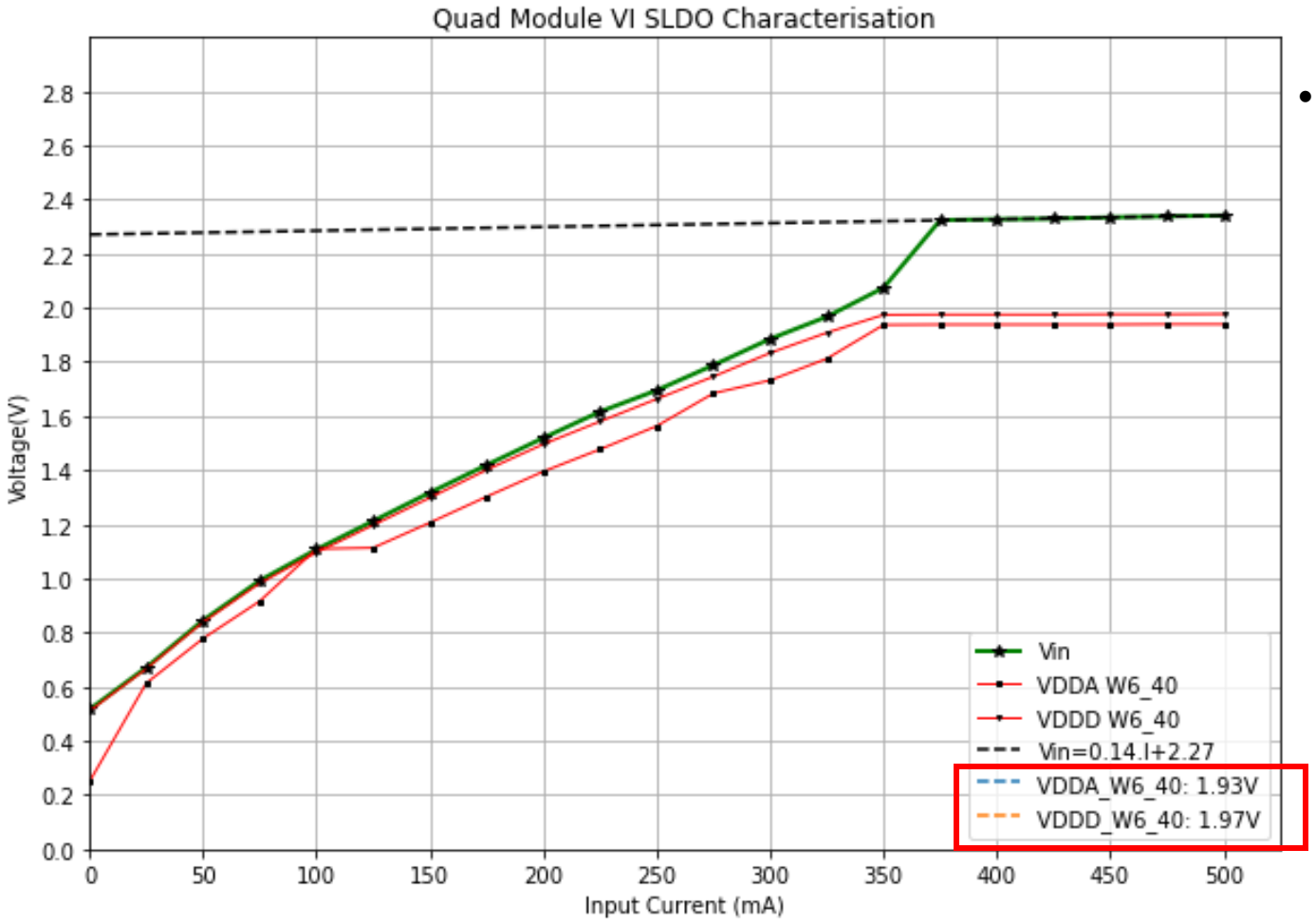


Shunt: allows for the constant current operation, **extra current protection**

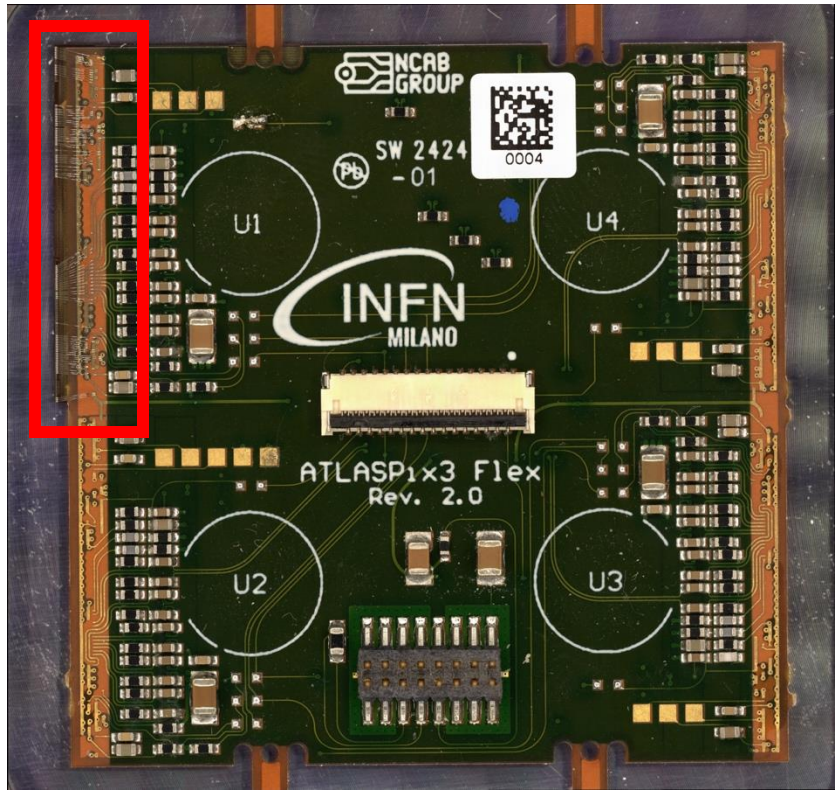
LDO: regulates **VDDD/A**

Quad Module-2

- The quad module-1 includes one wirebonded chip. The chip **is W6-40**, does not have a probing test results.
- The input current is **349 mA** as the regulation starts.

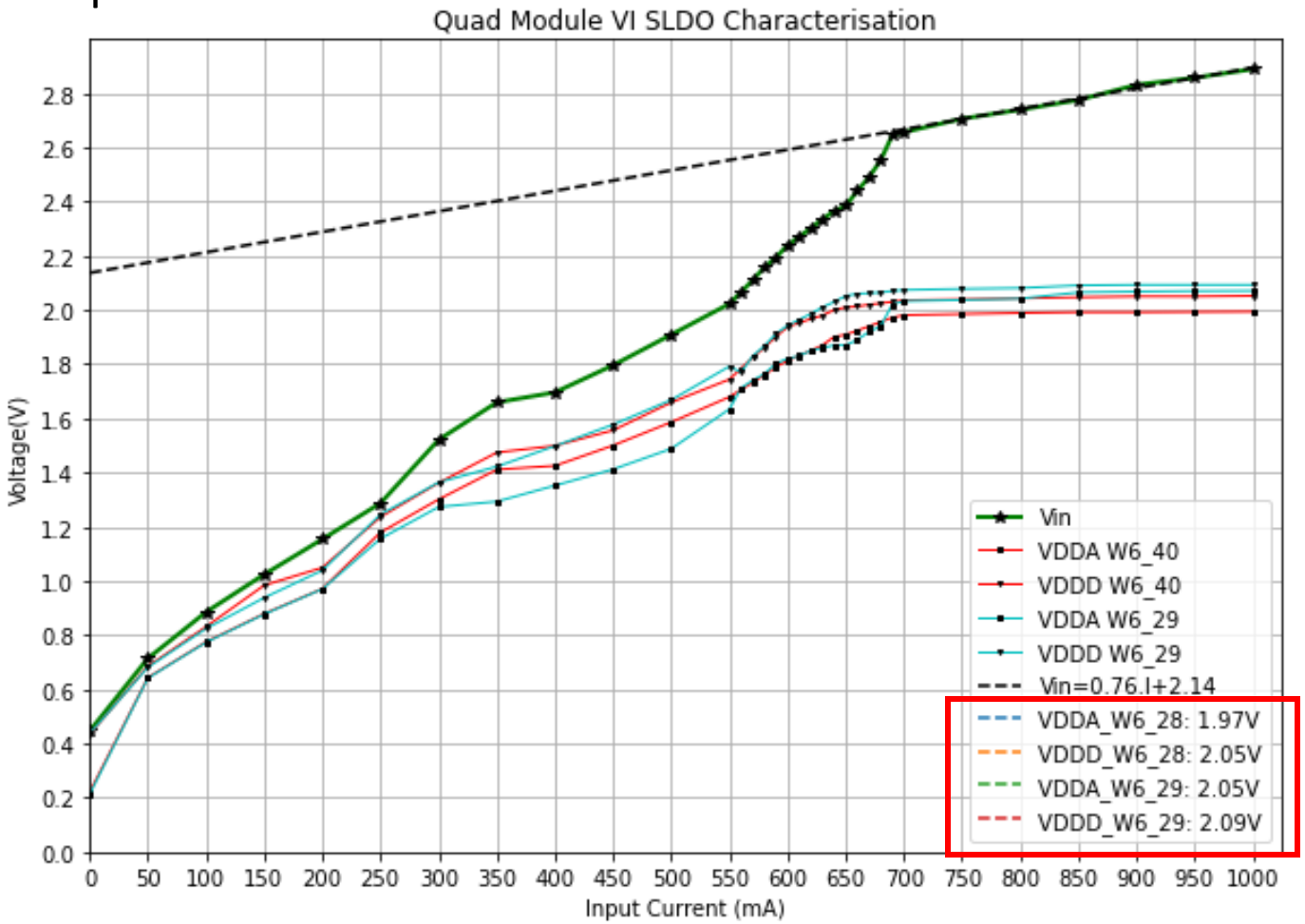


- Ohmic behaviour is seen after regulation starts.
- V_{offset} (the minimum required voltage to run the regulators) **2.27 V.**
- **Parasitic** resistance is **0.14 Ohm**.

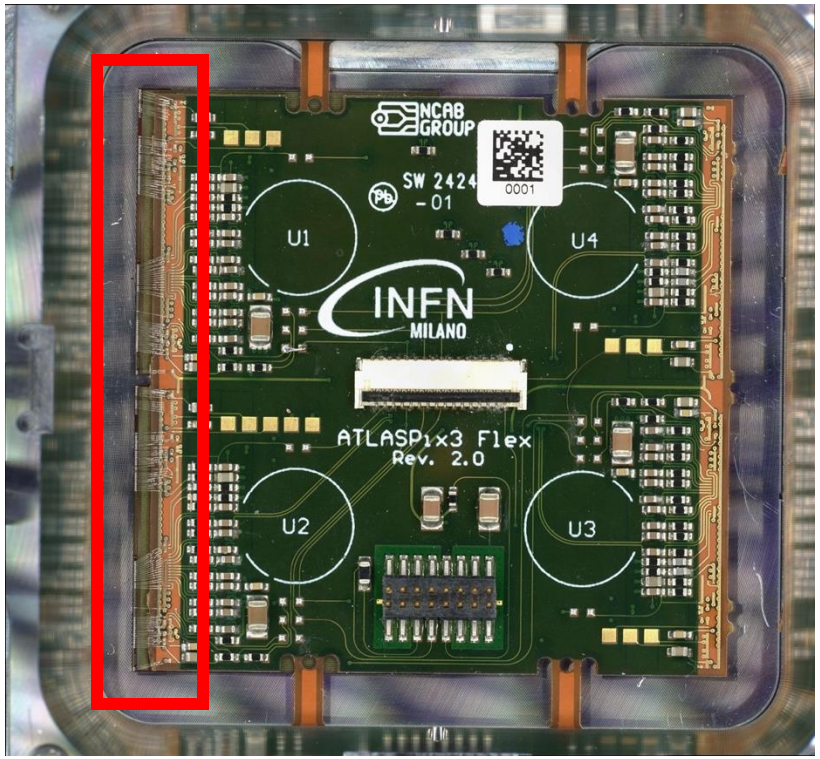


Quad Module-3

- The quad module-2 includes two wirebonded chip. The chips are **W6-28 and W6-29.**
- The input currents change between **640.75 mA and 703.96mA** as the regulation starts for each regulators on the chips.

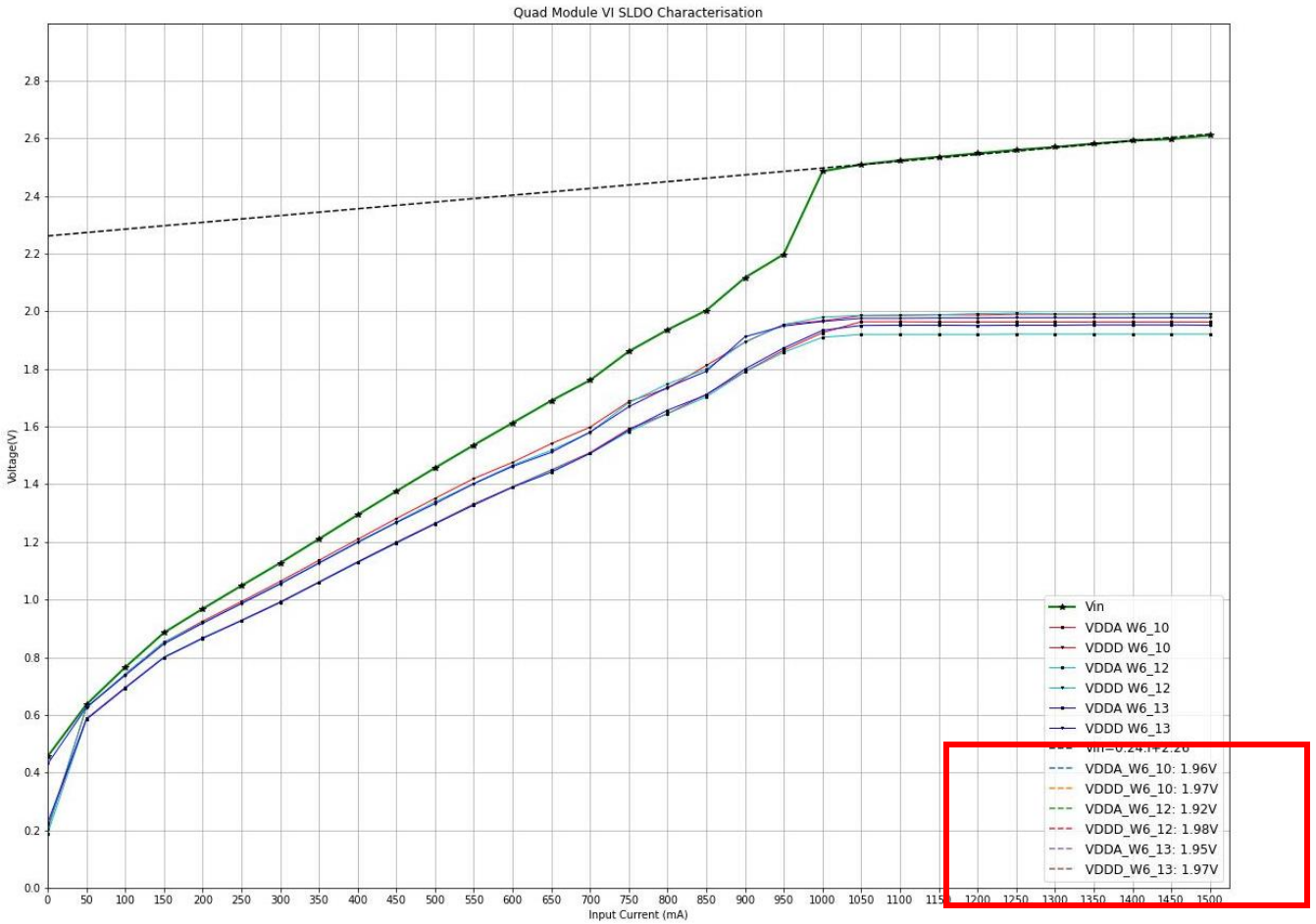


- Ohmic behaviour is seen after regulation starts.
- V_{offset} (the minimum required voltage to run the regulators) is **2.14V.**
- **Parasitic** resistance is **0.76 Ohm**.

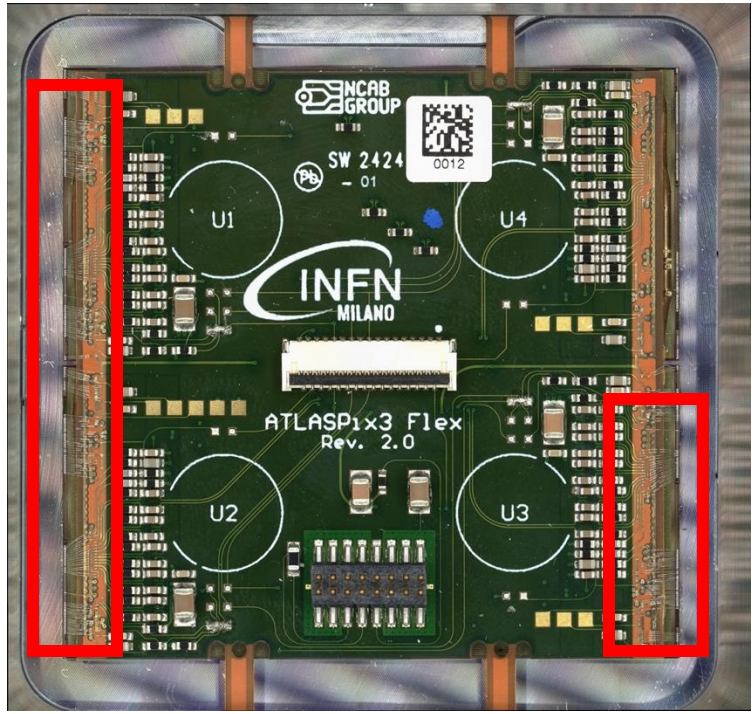


Quad Module-4

- The quad module-4 includes three wirebonded chip. The chips are **W6-10, W6-12 and W6-13.**
- The input currents change between **1 A and 1.2 A** as the regulation starts for each regulators on the chips.



- Ohmic behaviour is seen after regulation starts.
- V_{offset} (the minimum required voltage to run the regulators) is **2.26 V.**
- **Parasitic** resistance is **0.24 Ohm**.



Threshold & Noise scan for 2 configurations

		Single Module		Serial Powering Chain	
		Threshold (V)	Noise (V)	Threshold (V)	Noise (V)
Quad Module-2	Chip-1	**0.683 ± 0.07**	0.018 ± 0.003	**0.685 ± 0.06**	0.016 ± 0.002
Quad Module-3	Chip-1	**0.718 ± 0.06**	0.017 ± 0.002	**0.705 ± 0.06**	0.017 ± 0.002
	Chip-2	**0.677 ± 0.07**	0.018 ± 0.003	**0.675 ± 0.07**	0.017 ± 0.003

- Performed threshold and noise scans with the same 400 pixels in 2 configurations:
  - The variation of threshold values is **<2%.**

ATLASPix3.1 Quad Module Readout