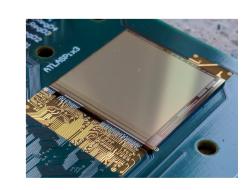


Pixel Detector Modules

a tale of sandwich and pie

- chips, and maybe Christmas lights









Yanyan Gao

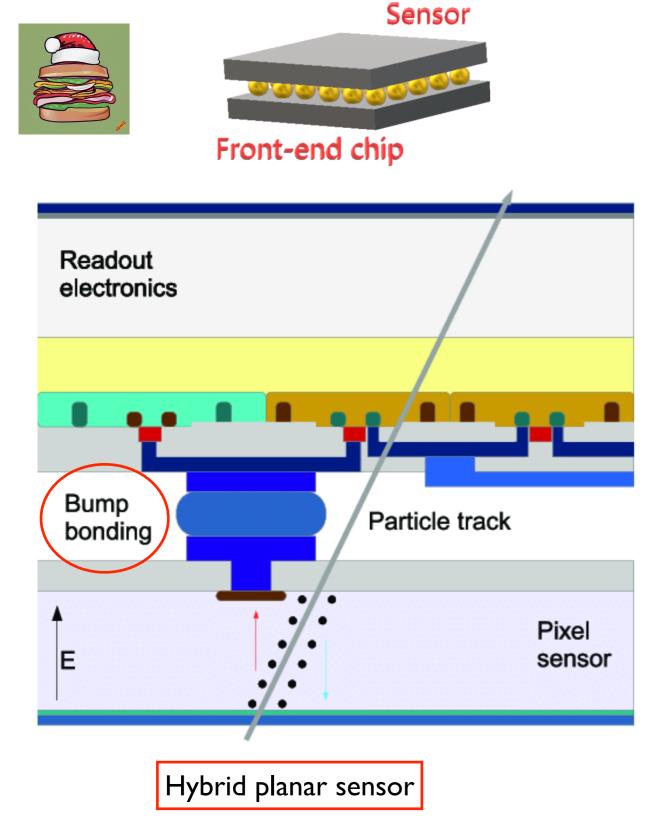


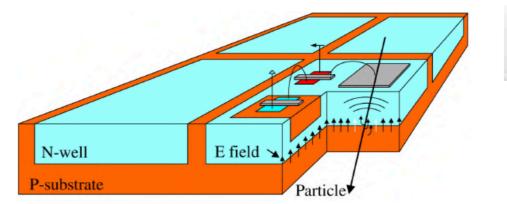


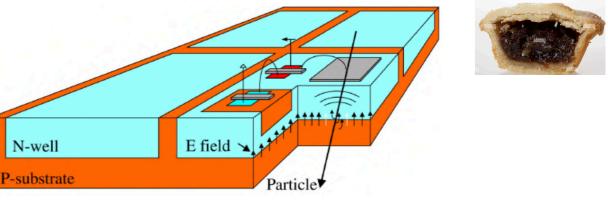


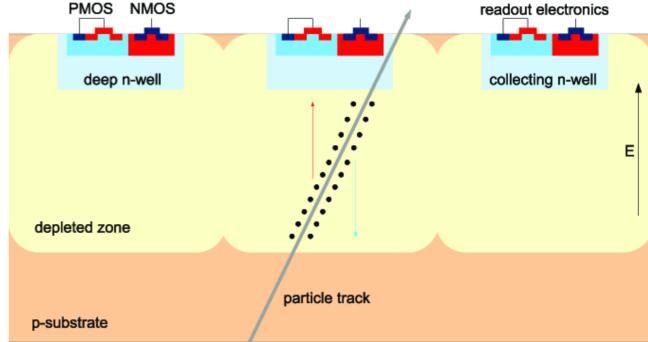
Edinburgh PPE Annual Christmas Gathering 2025

Pixel Detector: Hybrid vs Monolithic concepts



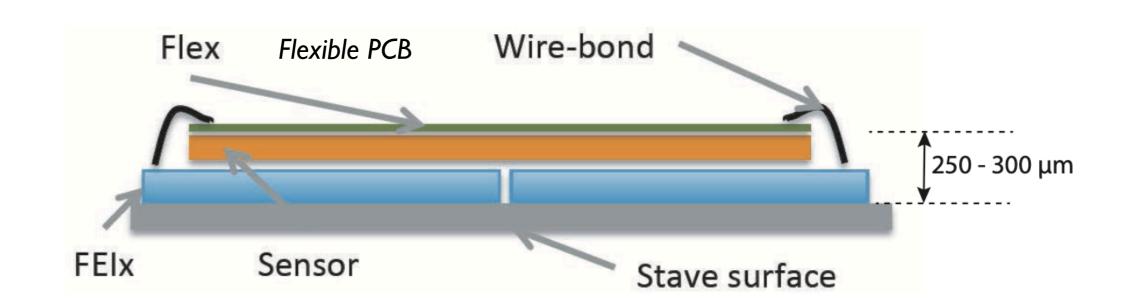




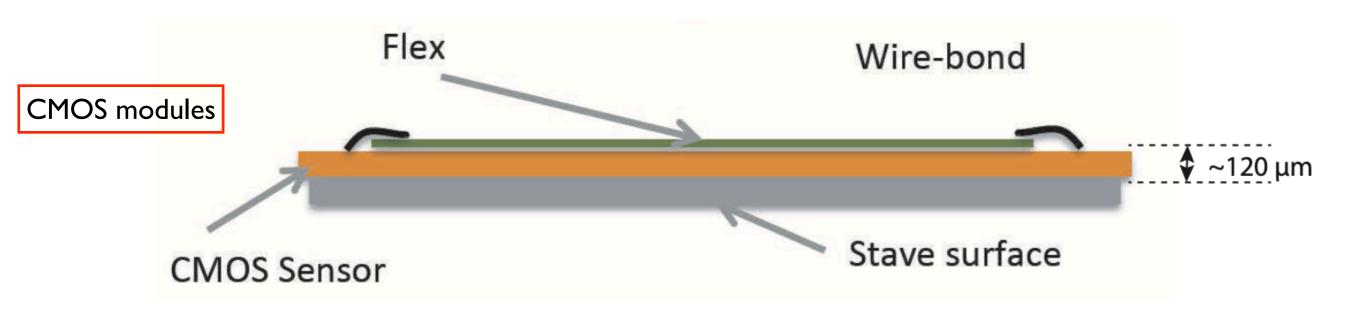


Monolithic Active Pixel Sensor (CMOS process)

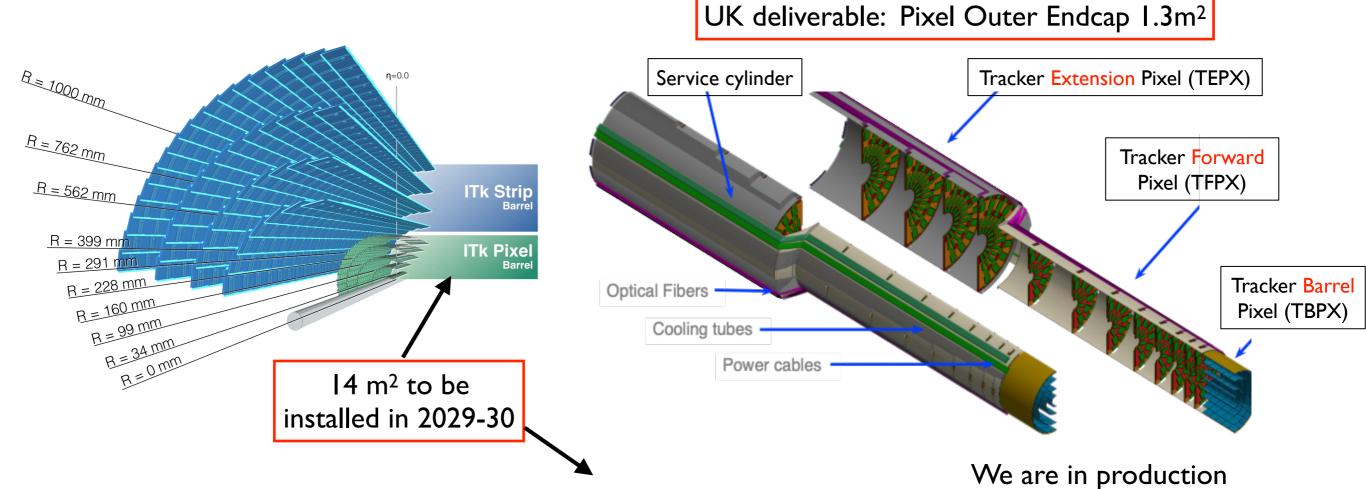
Chip(s) to Modules

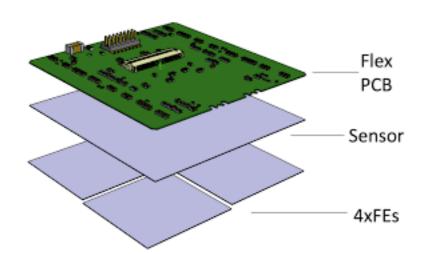


Hybrid modules

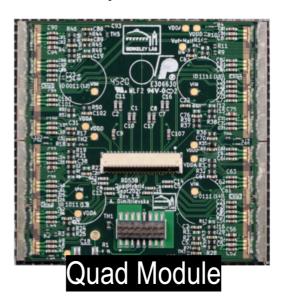


ATLAS Inner Tracker (ITk) Upgrade









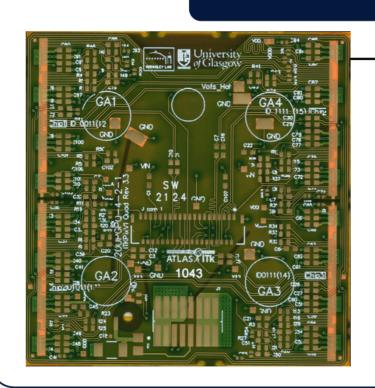


ITk Pixel Quad-Module Flex PCB QC

Afroditi in ITk week



Flex PCBs

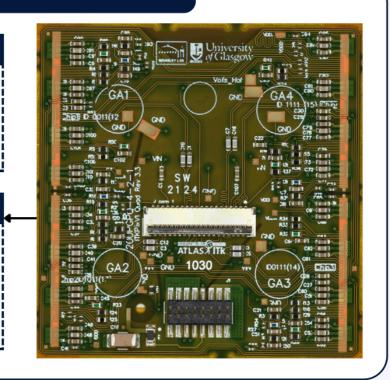


Bare PCB

For bare flexes, the QC workflow includes tests such as Layer thickness measurements and Visual Inspection (VI) to identify fabrication defects.

Populated PCB

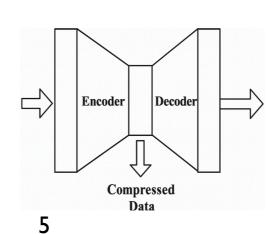
After population, further checks are performed, including VI of the assembled boards and High-Voltage/Low-Voltage (HV/LV) tests to verify electrical integrity.

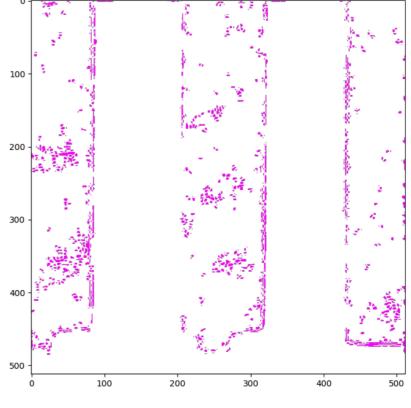






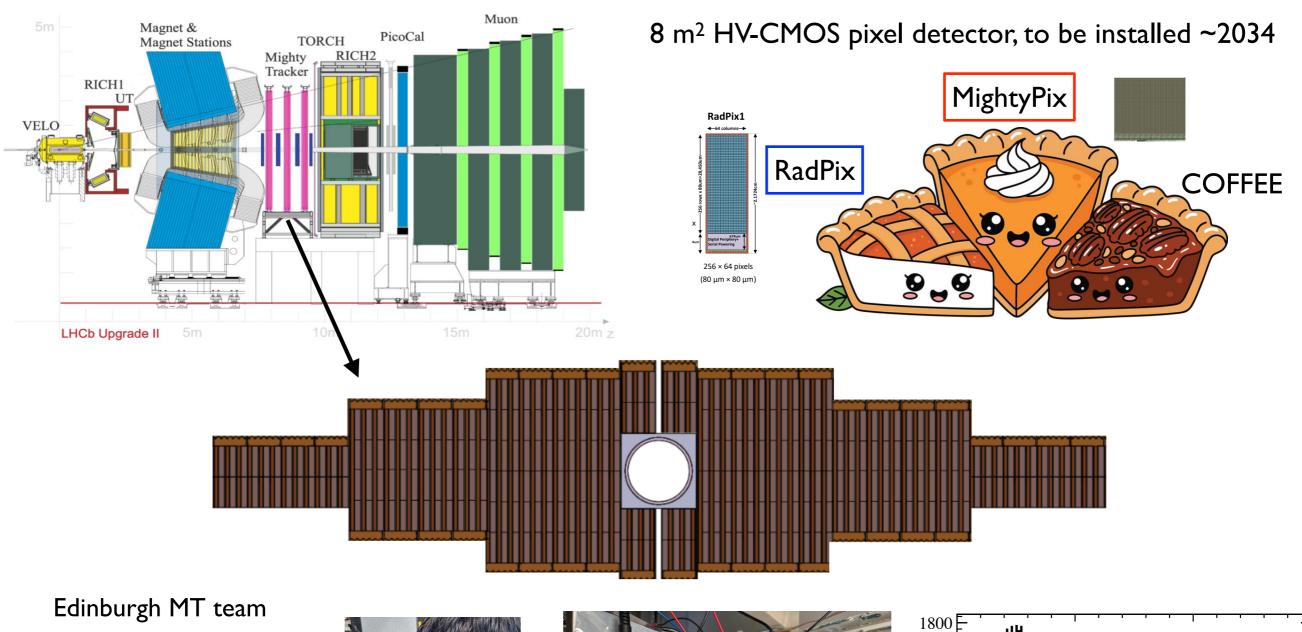




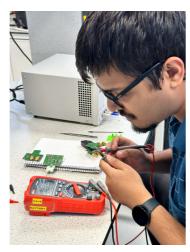


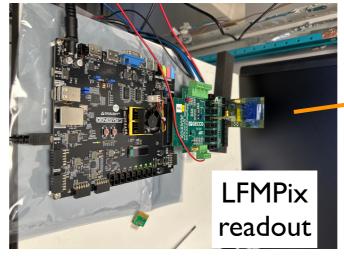
Anomaly Clusters Overlay

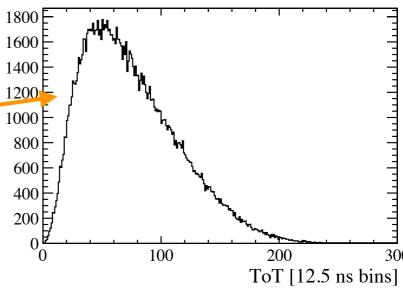
The LHCb Mighty Tracker



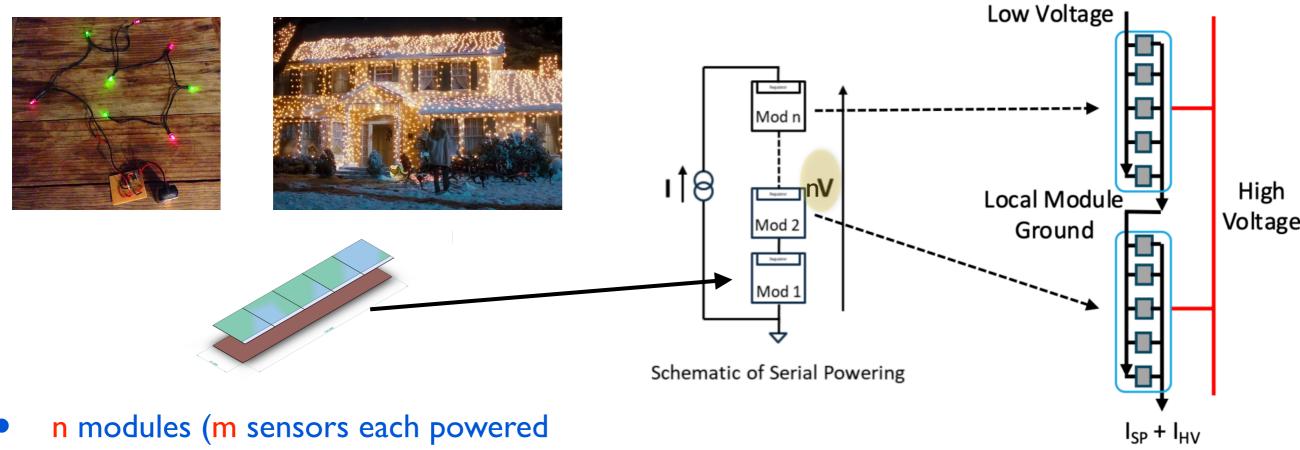






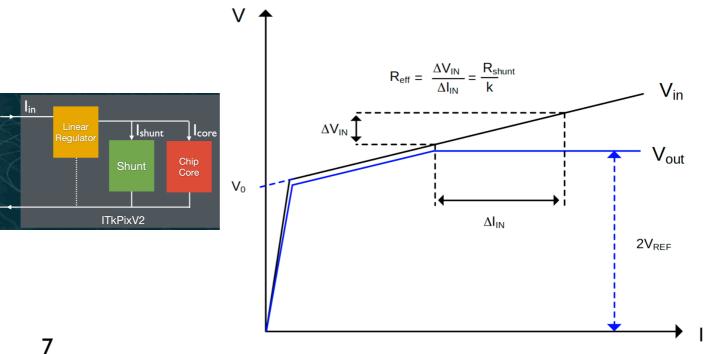


Multi-chip modules and Serial Powering Chain



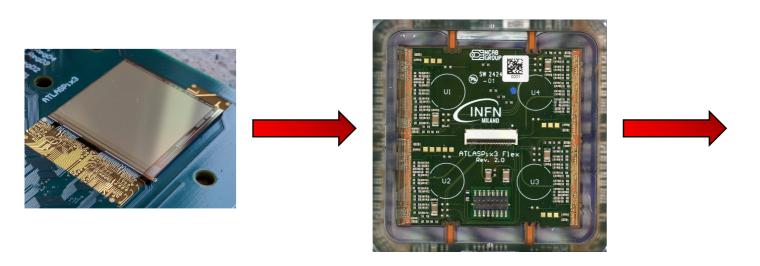
- in parallel) are powered in series
 - This is to power the readout electronics powering (~ a few V)
 - LHCb MT: 9 penta-modules (5 sensor each) in a chain
- Main advantage: service material reduction and power consumption
 - Cable volume/power loss reduce by n

On-chip Shunt Low Drop Out regulators: convert current to constant chip supply voltage VDD



"Large" HV-CMOS Pixel Detector Demonstrator

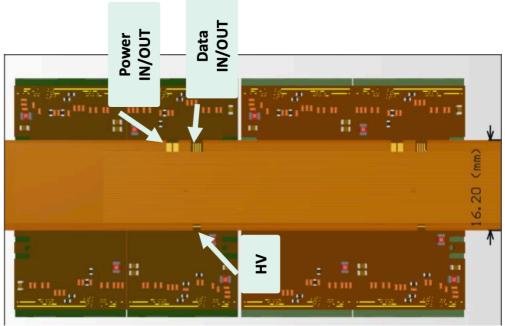
A system prototyping project in LHCb MT/DRD3 (CERN-DRD3-PROJECT-2025-014)



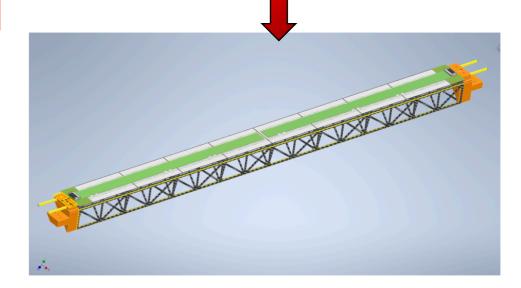


Pixel Detector Development for Future Collider-Based Particle Physics Experiments

Fuat Ustuner



A long (4 cm×60 cm) aluminium flex is in production at CERN Microfabrication Lab



- Optimised power and data signal routing along the stave
- Readout Unit Design
 - Multi-chip modules (e.g., 2×2 quad modules)
 - Serial Powering Architecture:
 - Internal bias generation via shunt-LDO regulators
 - Chip-to-chip data transfer for local aggregation