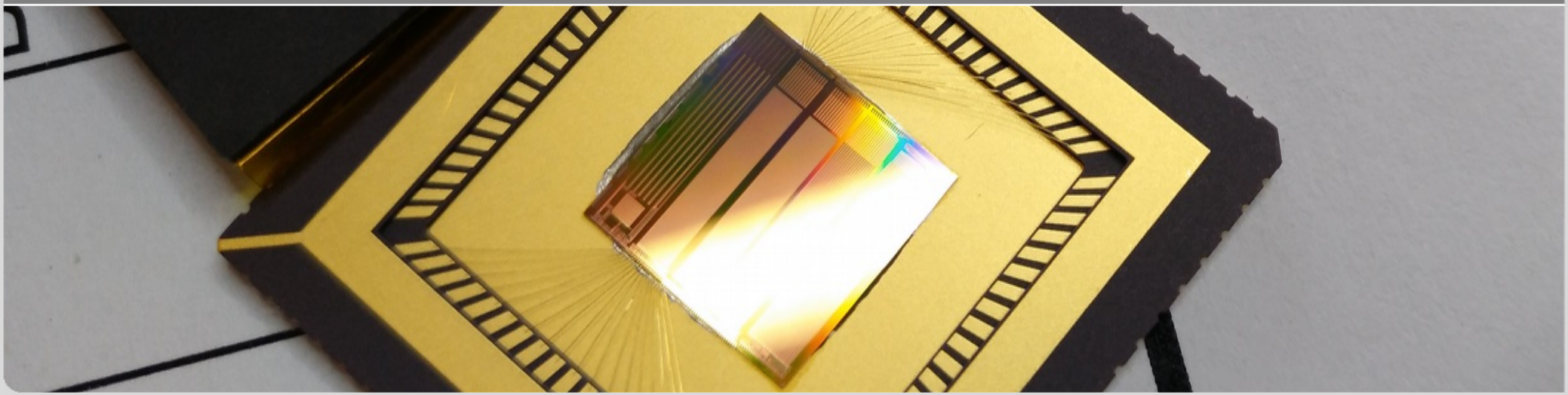
Karlsruhe Institute of Technology

ATLASPix3 – A full Reticle Sized Monolithic Pixel Detector

Rudolf Schimassek, **Ivan Perić**

Institute for Data Processing and Electronics (IPE)

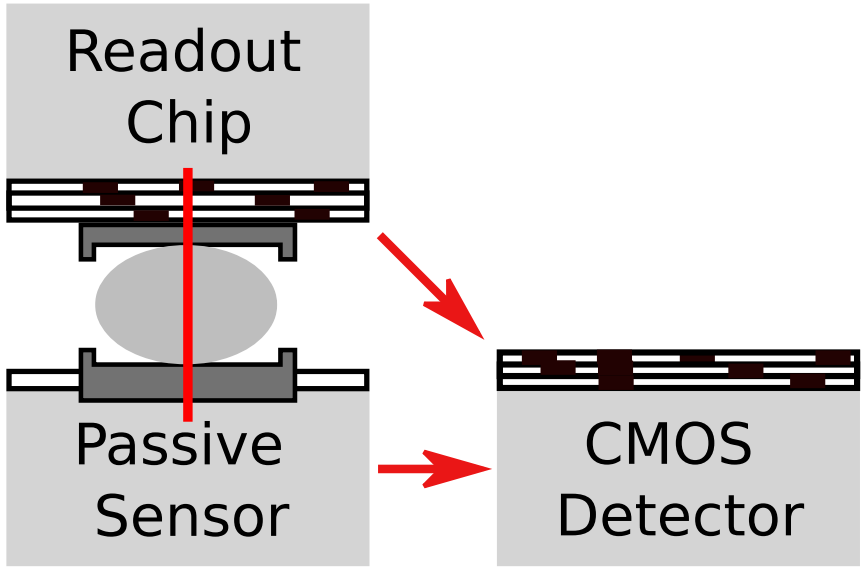


Outline

- Introduction to Monolithic HV-CMOS Detectors
- Development of the ATLASPix Detectors
- Lab Measurements on ATLASPix3
- Beam Test at DESY with ATLASPix3 Telescope

Hybrid ↔ Monolithic Detector

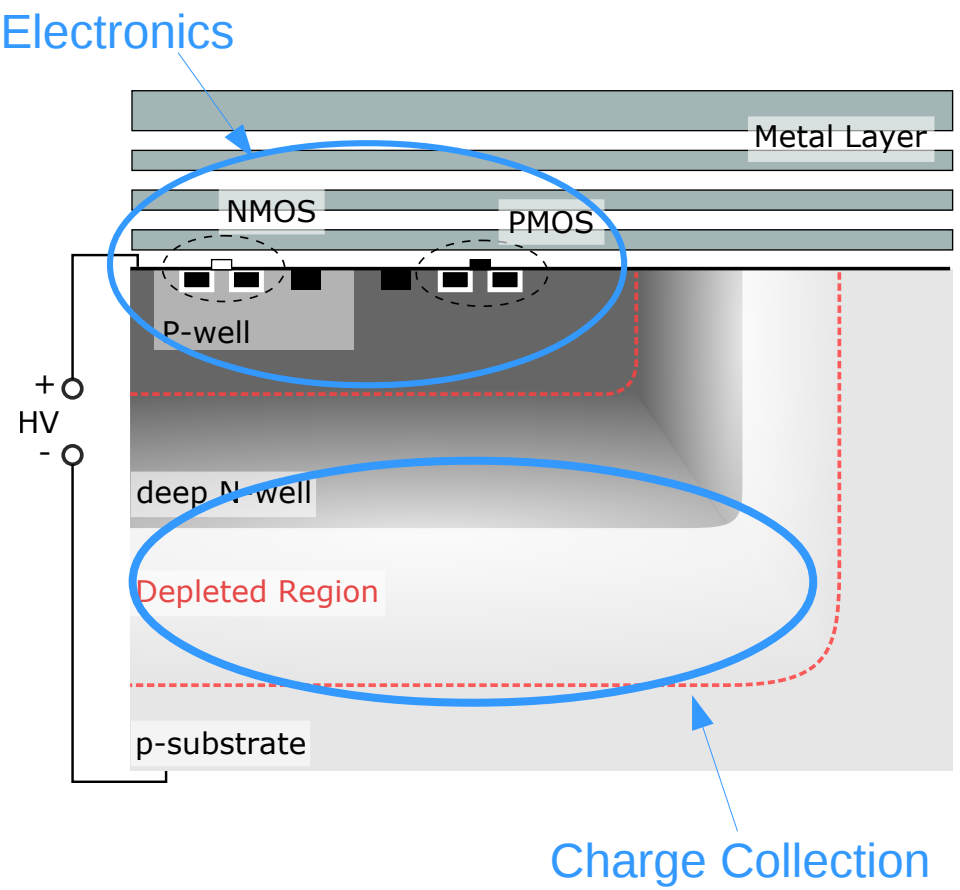
- Standard hybrid pixel detector:
  - Bump bond for signal transmission
  - Passive sensor
- Monolithic HV-CMOS Detector:
  - Integrated sensor with readout electronics on the same die
  - Electronics inside sensing diode
  - Charge collection by drift with high voltage



Hybrid ↔ Monolithic Detector

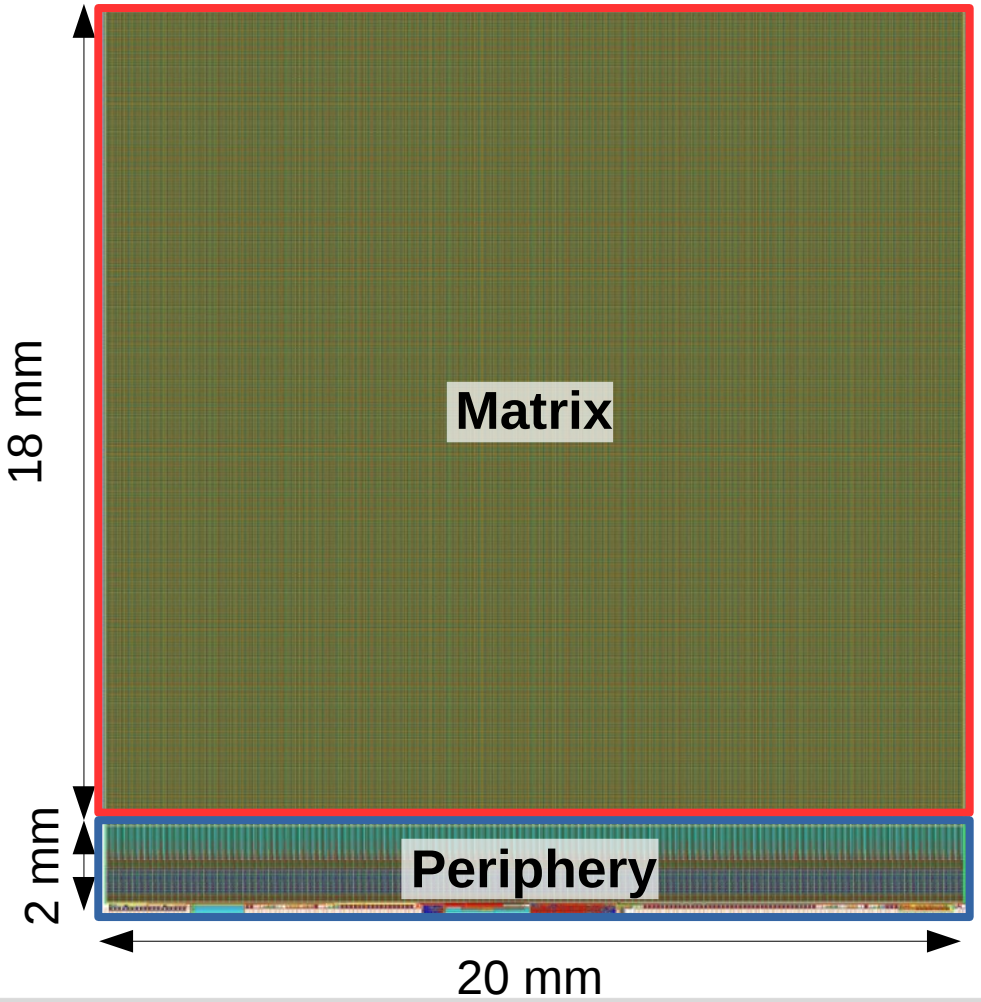
- HV-CMOS Sensor:
  - Charge Collection between p-substrate and deep n-well
  - HV p-sub contact on top side is the common implementation
  - Electronics isolated against HV inside deep n-well as “floating logic“
  - Implemented in commercial processes
    - large factory output available
  - Chip size limited by reticle size:

    ~ (2 x 2) cm²



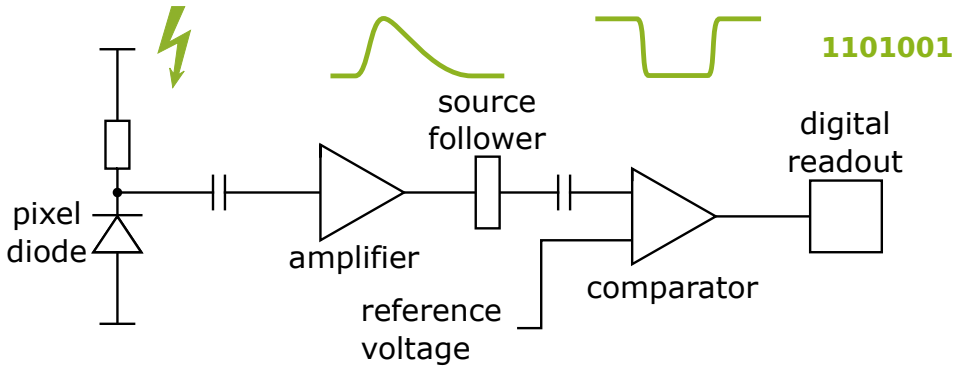
Monolithic HV-CMOS Detectors

- Small material budget
- Pixel size not limited by bump bonds
- Part of the electronics directly inside the pixels (amplifier, comparator)
- Two regions:
  - Pixel matrix (sensitive)
    - Amplifier, comparator, tuning structures
  - Periphery (not sensitive):
    - readout logic, buffers, configuration registers



Components of a Monolithic Detector

- Pixel electronics
  - Amplifier
  - Comparator
- Readout
  - Signal buffers
  - State machine
- Configuration registers
- Biasing structures
- Tuning structures

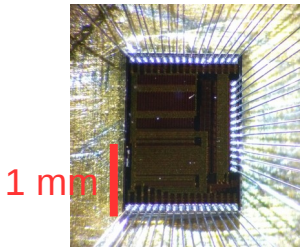


- Closed system
  - Testing structures need to be foreseen in the design to be measurable

THE ATLASPIX DETECTORS

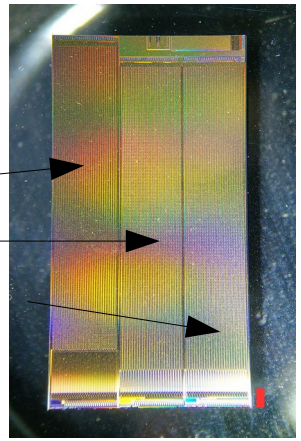
The ATLASPix Detectors

- Development of monolithic Detectors started in 2014 with the HVStripV1
- ATLASPix Development line:
  - large scale prototypes
  - started in 2017
  - design target: ATLAS ITk Upgrade Layer 4



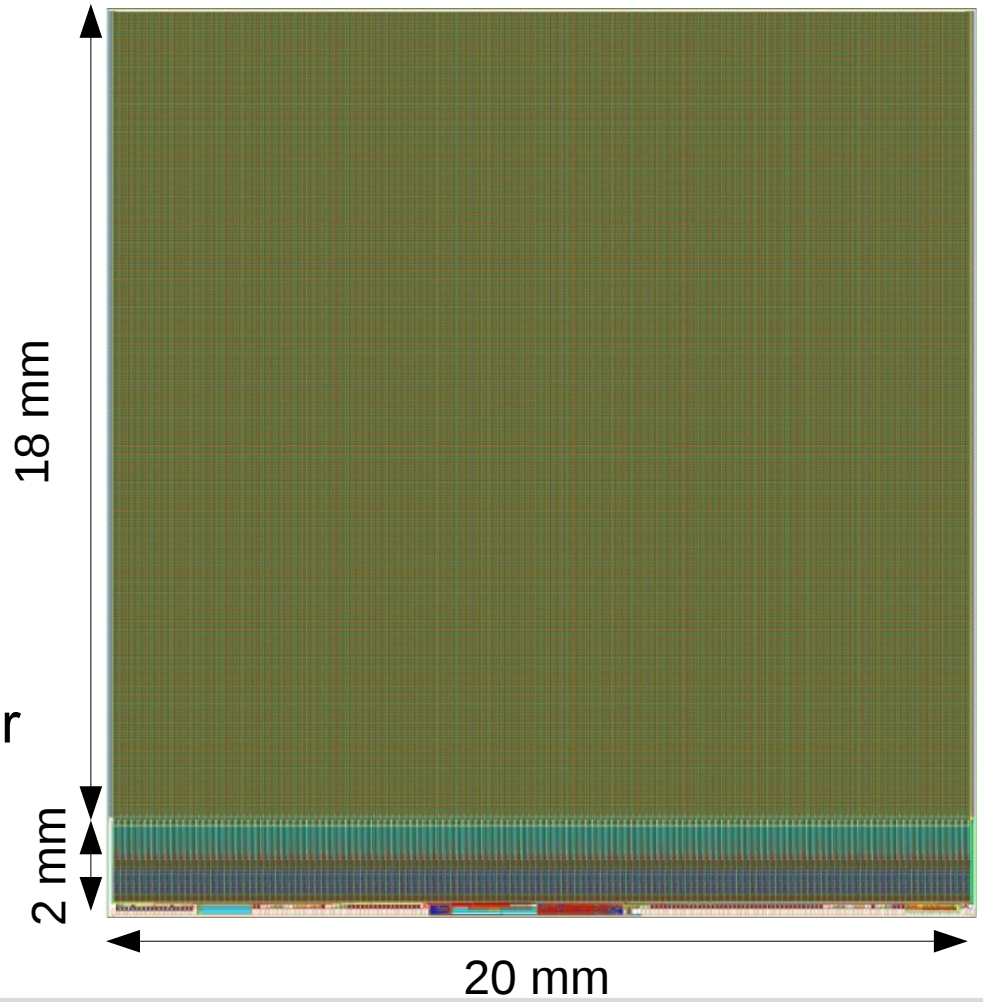
HVStripV1

ATLASPix1



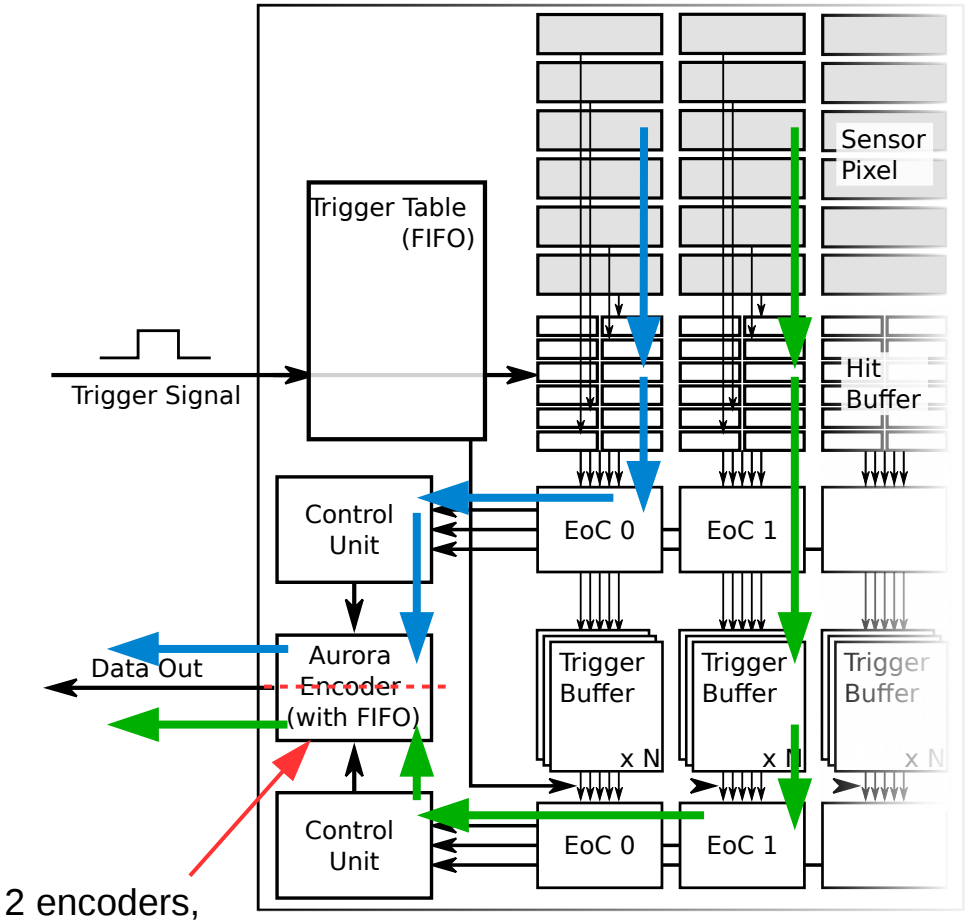
ATLASPix3

- Single matrix: 132 x 372 pixel
  - Pixel size 150 x 50 µm²
- Column-drain readout with and without trigger
- Radiation hard design with SEU tolerant global memory
- 3 bit tuning DAC per pixel plus enable bit
- Several configuration methods for different wire count constraints (serial, SPI, single line)



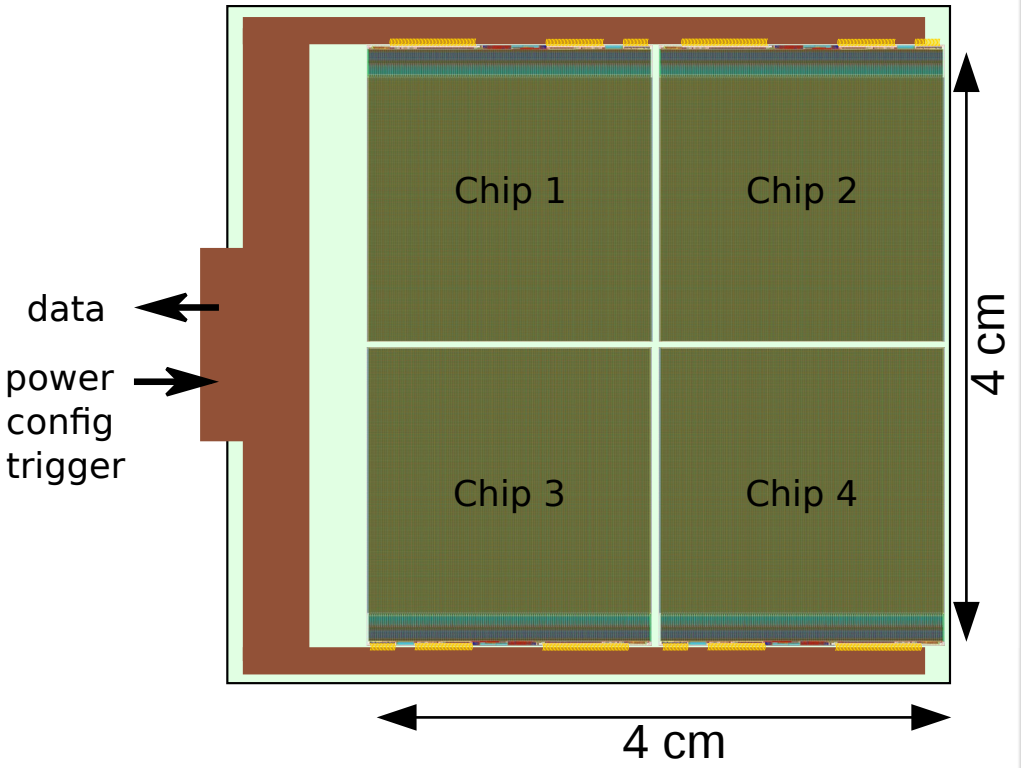
ATLASPix3 – Readout Structure

- Triggered and triggerless readout possible via two concurrent readout structures
  - separate control units
  - Configuration via SEU tolerant registers
- Data transmitted:
  - triggerless: 8/10b Aurora encoded
  - triggered: 64/66b Aurora encoded
- Readout was optimised using verilog and ROME simulations



The ATLASPix Detectors

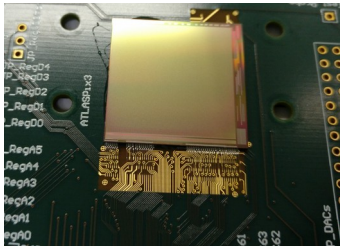
- Required features for ATLAS (with first implementation):
  - Sorted readout (ATLASPix2)
  - Triggered readout (ATLASPix1_M2 / ATLASPix3)
  - RD53 compatibility (ATLASPix3)
    - Data encoding (64/66 bit Aurora encoding)
    - Command decoder
  - Quad module compatibility (ATLASPix3)

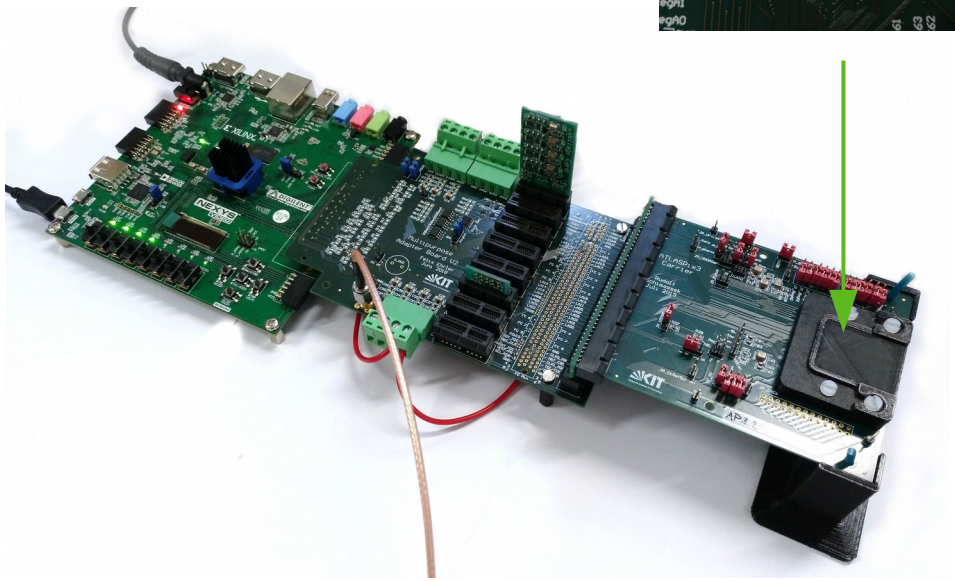


ATLASPIX3

Lab Measurement Setup

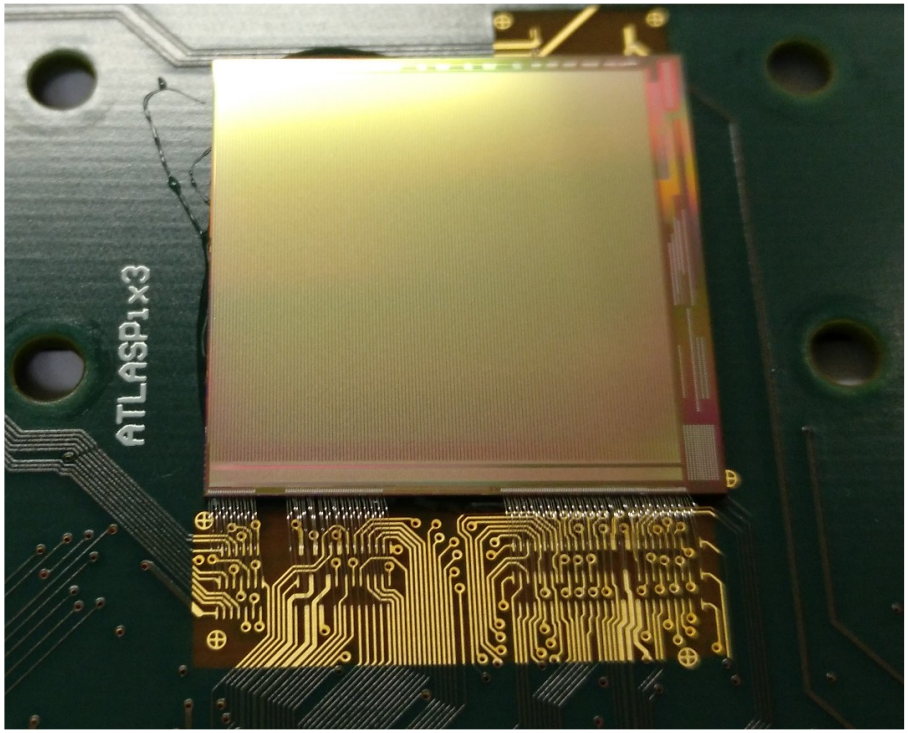
- Artrix-7 FPGA board
- GECCO adapter board
  (GEneric sensor Configuration and COntrol System)
  - PCIe connector
  - Highly modular with function cards
  - No cable connections to carrier PCB
- ATLASPix3 carrier PCB
- Firmware
  - Chip configuration
  - Data decoding and reduction
- Software (Qt based)





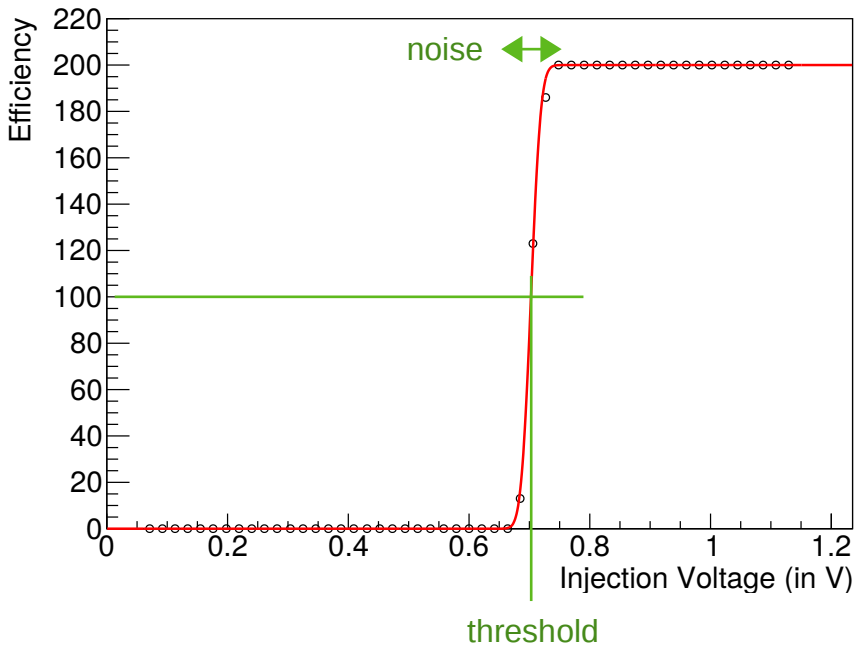
ATLASPix3 Measurements

- Serial and SPI configuration tested to work
- RAM writing is working
- Untriggered readout tested to work at 400 Mbps (DDR, results in 25 ns time stamp)



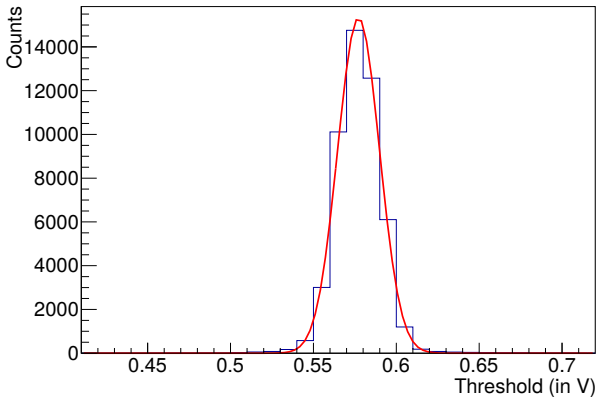
Threshold and Noise Definitions

- Charge injections of increasing strength are sent into a pixel
- Count number of detected signals → detection efficiency
- Shifted and scaled gaussian error function is fitted to the data points

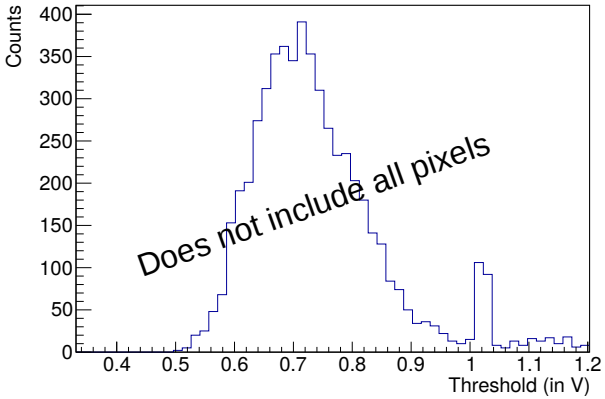


Threshold Distribution

- Using untriggered digital readout and charge injections, a threshold scan has been performed for the whole matrix
- Duration for whole matrix (49104 pixels): 7 hours
  - Limited by USB connection in the measurement setup



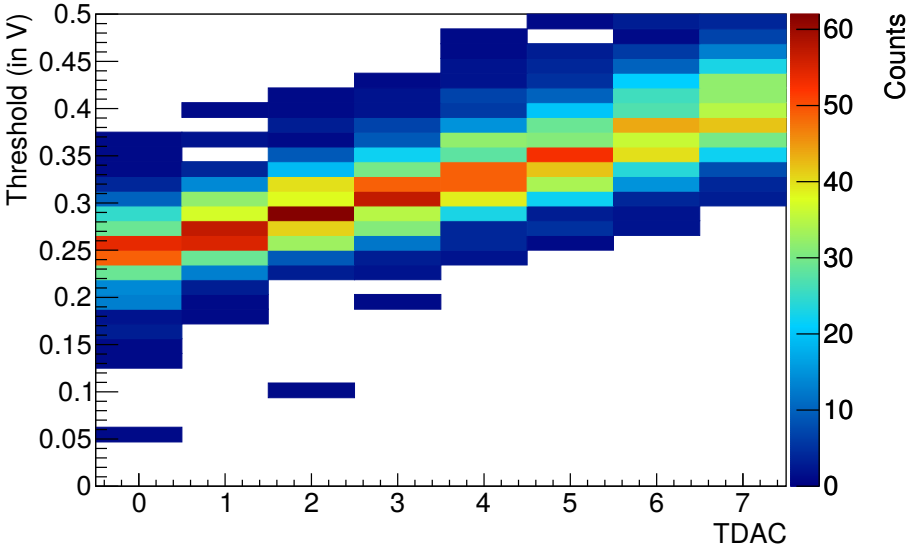
tuned



untuned

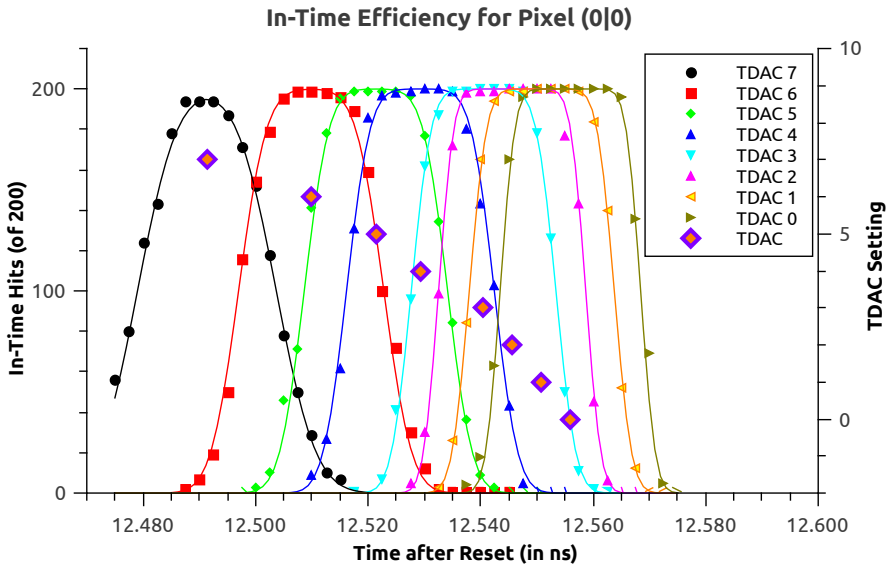
Matrix Tuning

- Detection threshold changes linearly with the tuning DACs settings
- The colour axis is the number of pixels in a bin



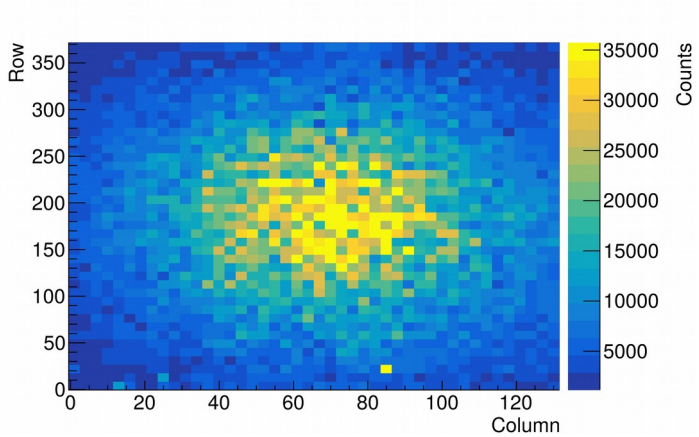
Matrix Tuning

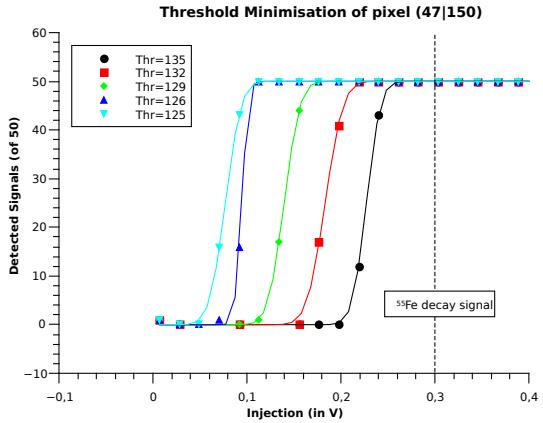
- In case the signal to measure are large, the tuning DACs can be used to correct for timing differences:
  - Limited amplifier current
    → finite rise time
  - Different threshold
    → also different timing
  - Signals of interest large
    → threshold level not important
    → TDAC useable for timing
- An additional means in addition to delay difference compensation in the design



^{55}Fe Source Test

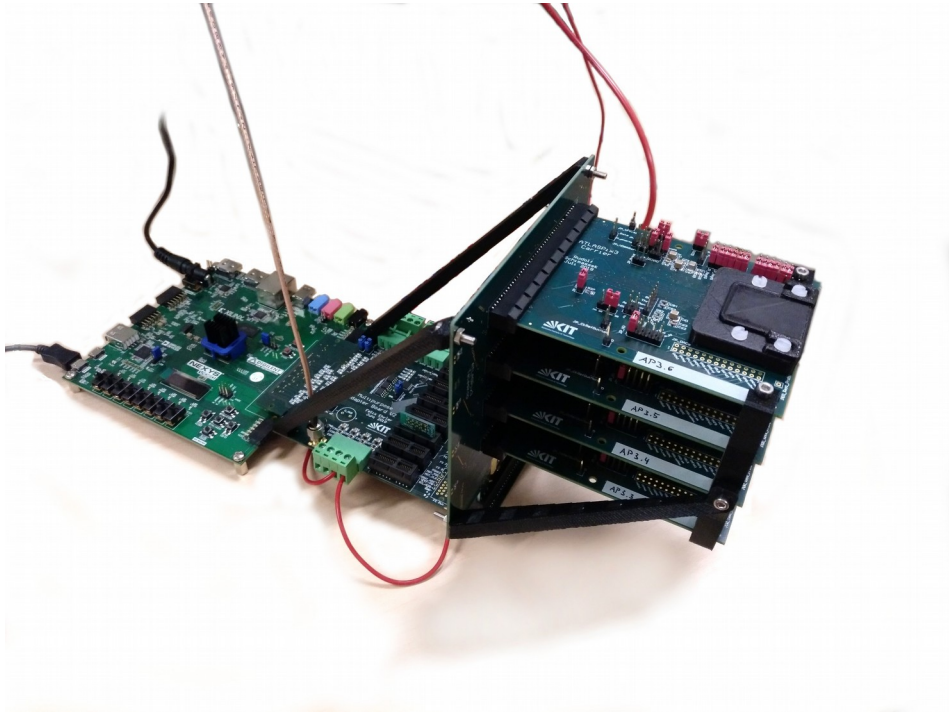
- ^{55}Fe decay signal equals 0.3V of charge injection
- Threshold lowered to get sensitive to these signals
- On single pixel level, thresholds of about a quarter of an ^{55}Fe decay can be achieved without noise





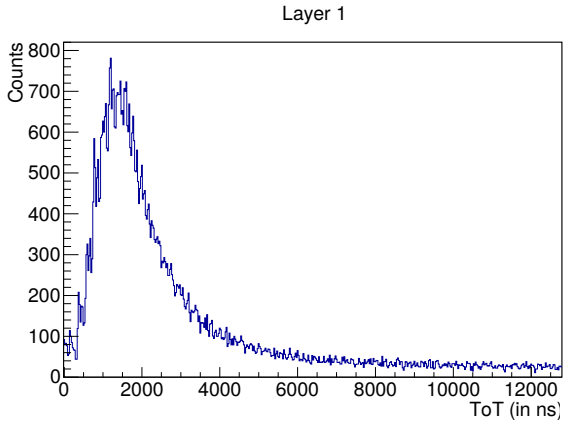
ATLASPix3 Telescope

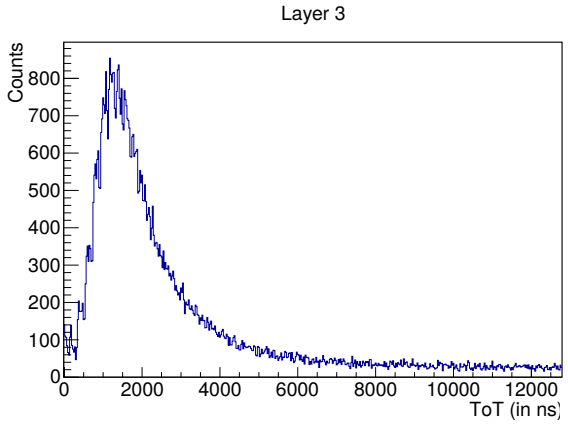
- For a beam test at DESY, a compact four layer telescope was built based on ATLASPix3 sensors
- Uses the same carrier PCB as single chip setup
- Read out by one Artrix-7 via the GECCO board

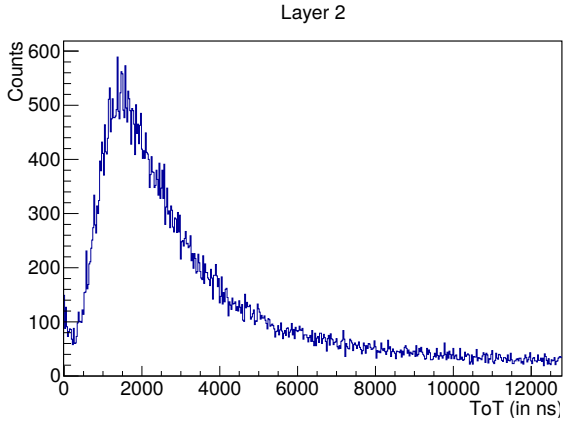


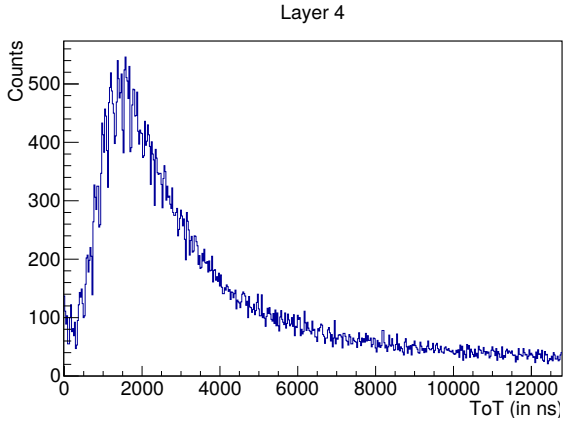
ATLASPix3 Telescope

- 7 GeV electron beam at DESY
- Time over Threshold (ToT) is working on all four layers
- Plots for all pixels on a chip combined
- Jitter due to different time stamp speeds for rising and falling edge



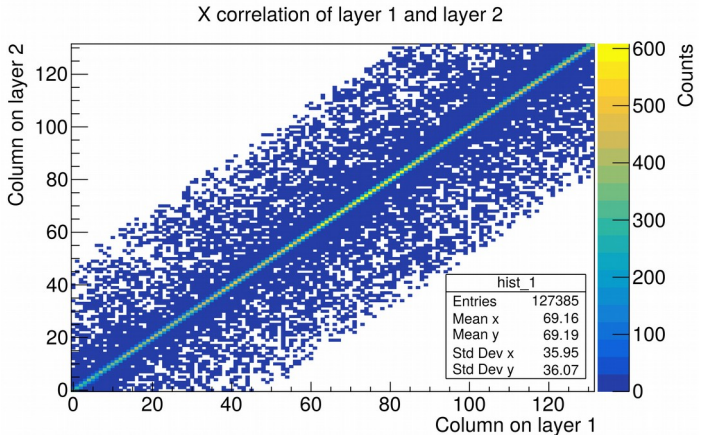


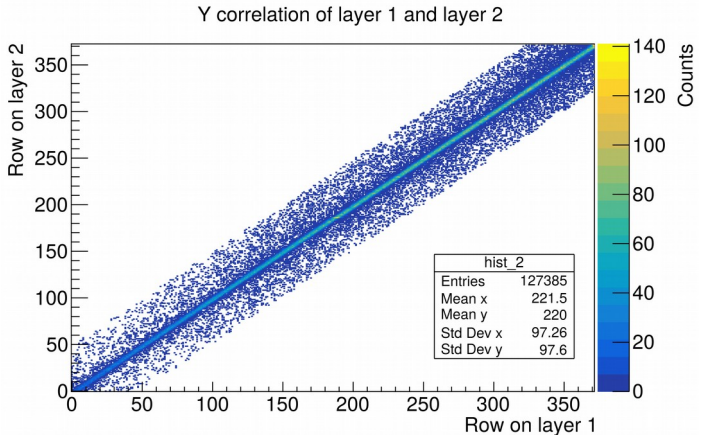




ATLASPix3 Telescope

- Correlation visible between all layers (example plots)
- Cut off due to analysis script
- Major part of the analysis still to be done



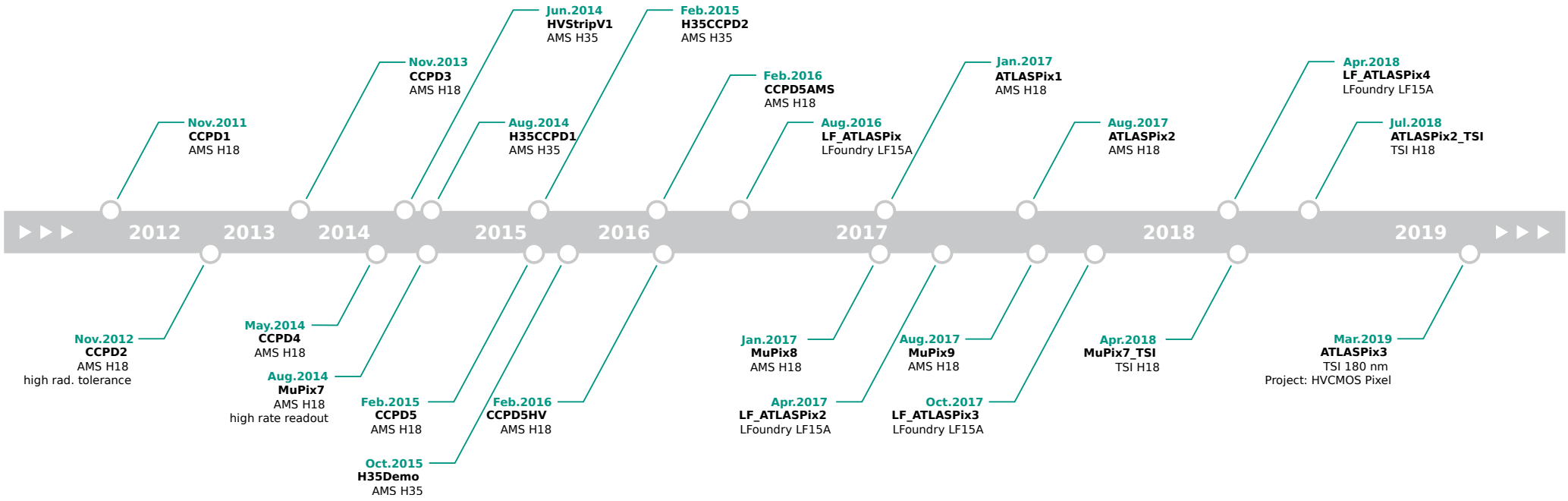


Conclusions

- ATLASPix3 is a full reticle, single matrix detector
- The detector is working and has a high yield
- Trimming is possible to compensate for threshold and timing differences
- A four layer beam telescope was developed and is operational

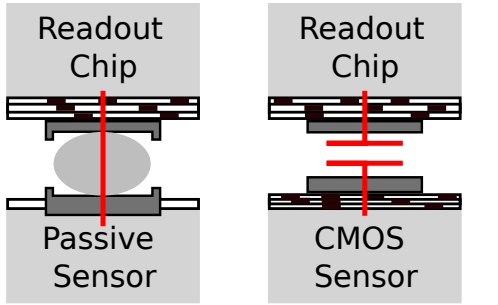
BACKUP

Development of HVCMOS Detectors



Development of HVCMOS Detectors

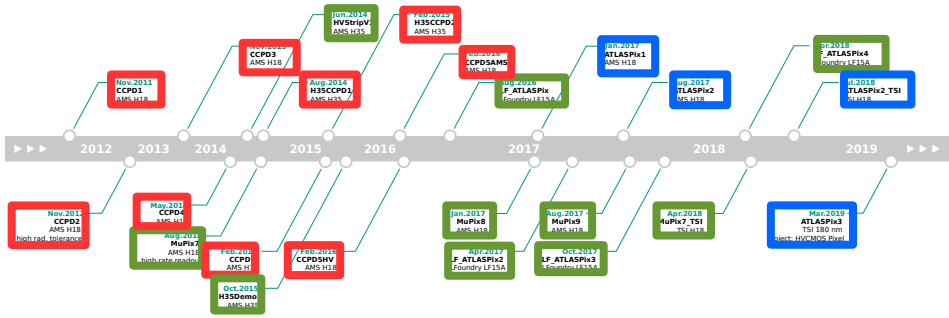
- Development started 2011 with active CMOS sensors:
  - Capacitively Coupled Pixel Detector (CCPD)
- switched to monolithic detectors in 2014 (HVStripV1)



standard hybrid Detector

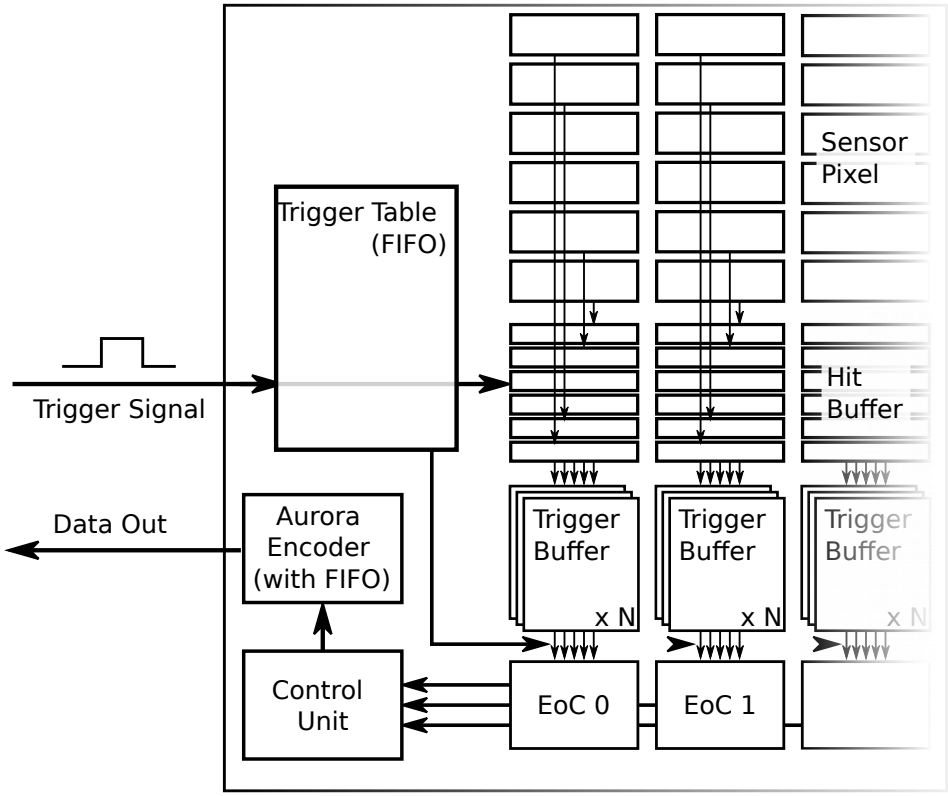
Capacitively Coupled Pixel Detector (CCPD)

- 3 lines of development:
  - CCPD sensors
  - ATLAS ITk prototypes (ATLASPix)
  - Concept evaluation detectors / other projects



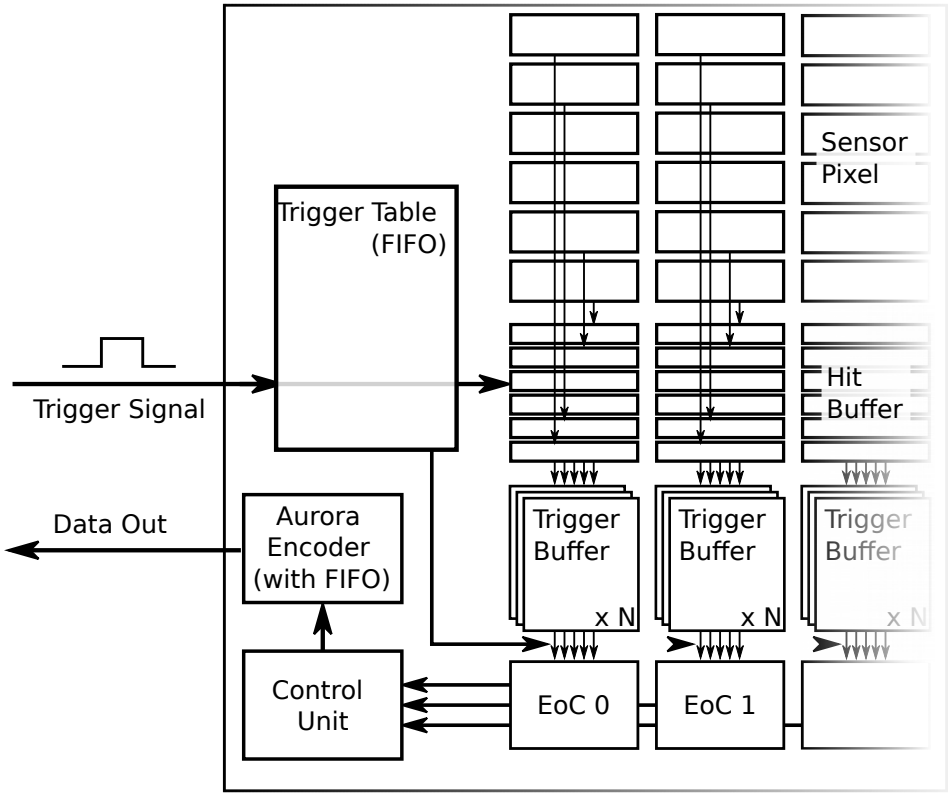
Towards ATLASPix3 – Architecture Changes

- Optimisation of memory sizes and SM using ATHENA / Geant4 data for ATLAS ITk layout using ROME
- Introduction of trigger table and Aurora encoder FIFO
- Triggered column-drain readout with separation of hit buffers and trigger buffers
- Changed readout state machine (SM) for more efficient readout



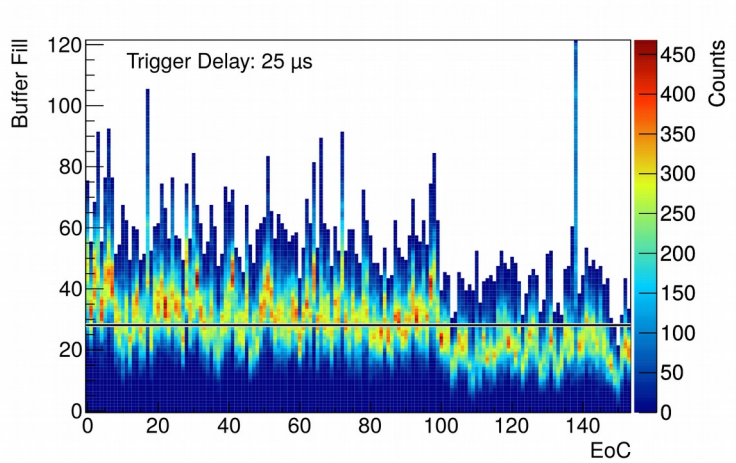
Towards ATLASPix3 – Architecture Changes

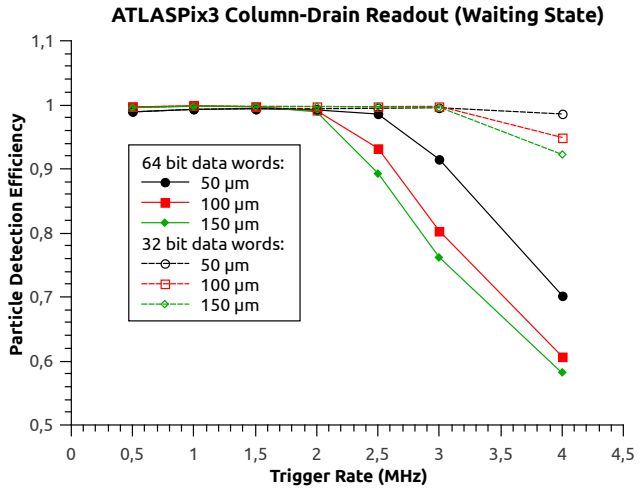
- Decision for Column-Drain Readout:
  - ATLAS layer 4 hit rate too low/clusters too small to gain from PPtB benefits
  - Simpler integration of additional per-pixel information (ToT)



Towards ATLASPix3 – Architecture Changes

- Dimensioning of the trigger buffers depends on trigger delay and cluster size
- Reducing the data word size to 32 bit effectively doubles the bandwidth improving the efficiency of the readout



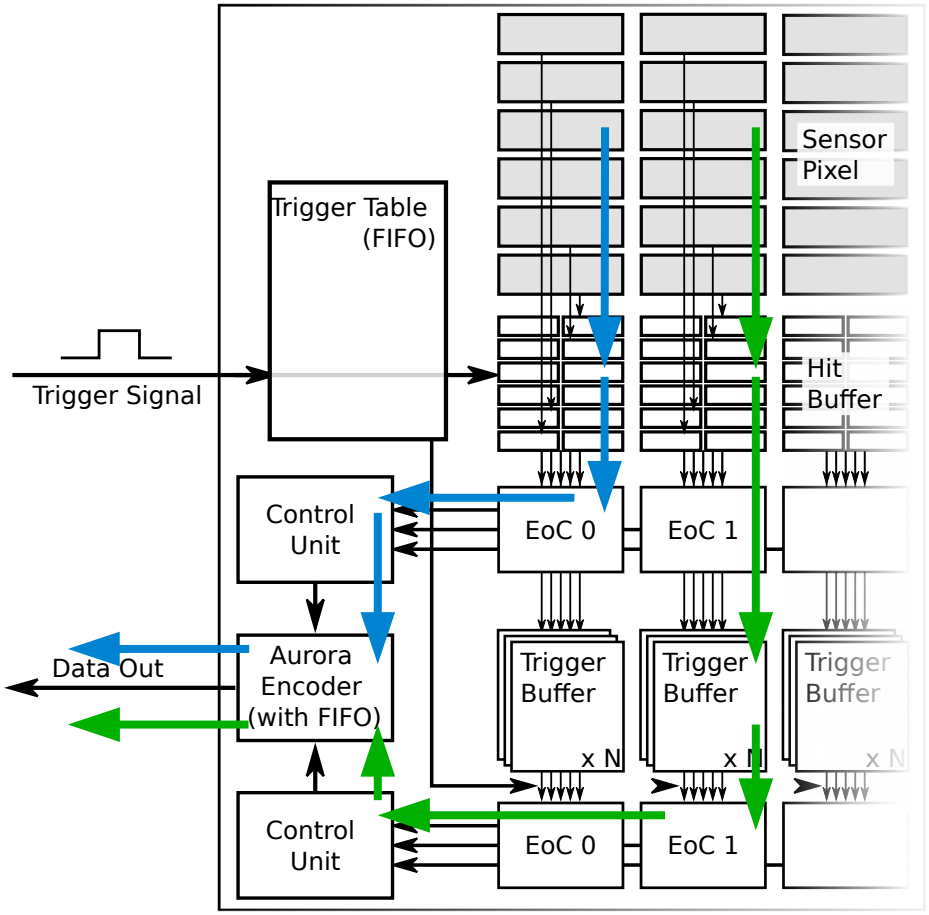


ASIC and Detector Lab at KIT
ROME

ATLASPix3 – The Submitted Design

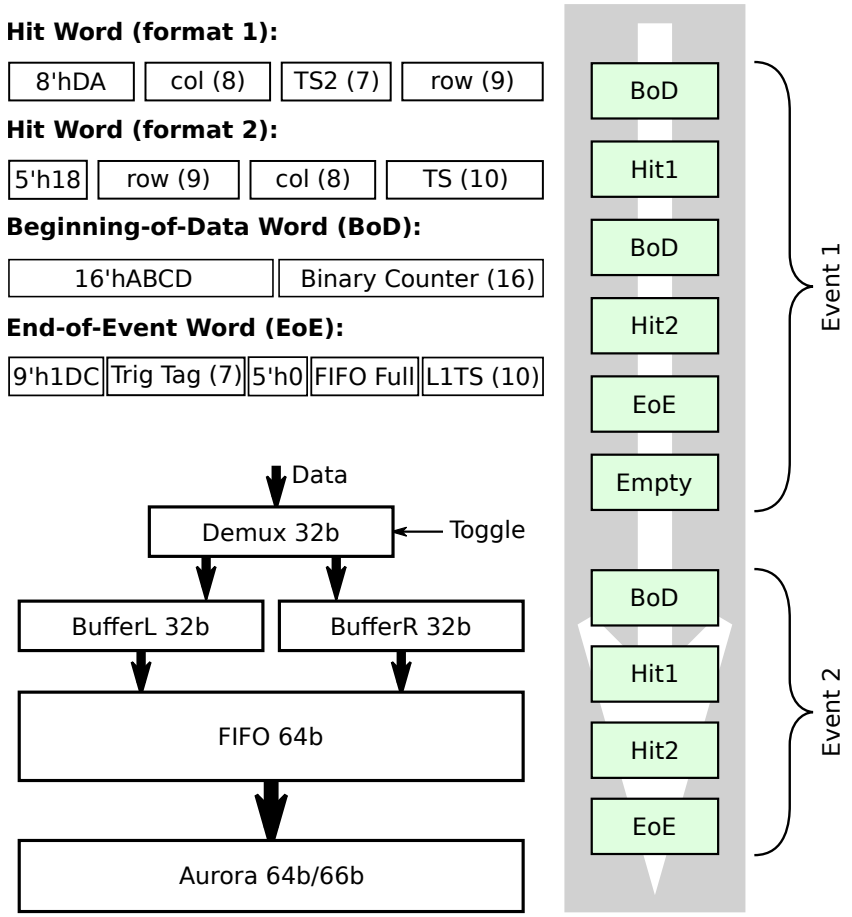
- Triggered and triggerless readout possible via two concurrent readout structures
  - separate control units
  - Configuration via SEU tolerant registers
- Data transmitted:
  - Row address 9 bit
  - Column address 8 bit
  - Time stamp 10 bit
  - Time over Threshold 7 bit

  total per pixel hit: 34 bit



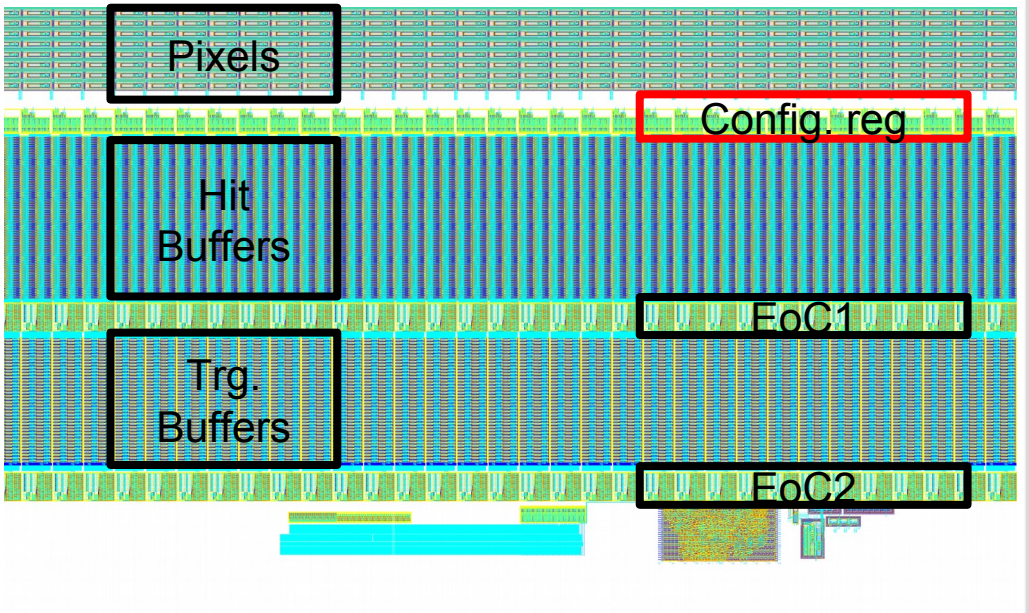
ATLASPix3 – The Submitted Design

- Data transmission in 32 bit words:
  - beginning-of-data word
  - Hit word
  - End-of-event word
  - Spacing word
- Multiplexer structure to use full width of the Aurora code
- Spacer words used to make event word number even
- Configurable data contents



ATLASPix3 – The Submitted Design

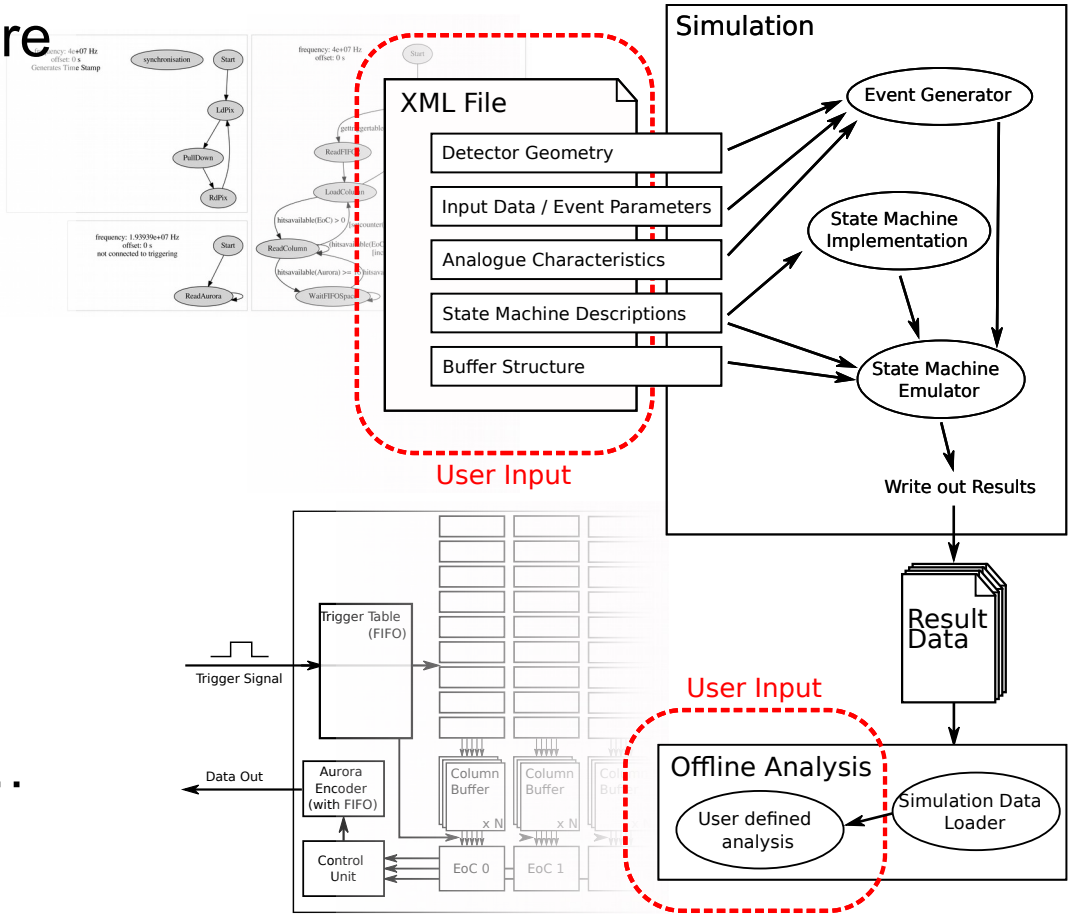
- Slow Control:
  - Shift registers contain chip configuration and enable read/write to pixel RAM
  - Triple redundant shift register elements for SEU tolerance
- Option to bypass the command decoder and access the shift register signals directly
- The 160 Mbps command transmission is used to recover the 160 MHz clock



Pixel	150 x 50 µm²
Hit Buffer (in double column)	75 x 4.2 µm²
Trigger Buffer (in double column)	75 x 15 µm²

The ROME Simulation Framework

- Versatile Readout Architecture Simulation for Synchronous Detectors
  - Dynamic testing instead of static bandwidth calculations
- Optional use of ATLAS ITk physics simulation data
- Complete logging for user defined offline analysis
- Find rate capabilities, bottlenecks, shortcomings, …

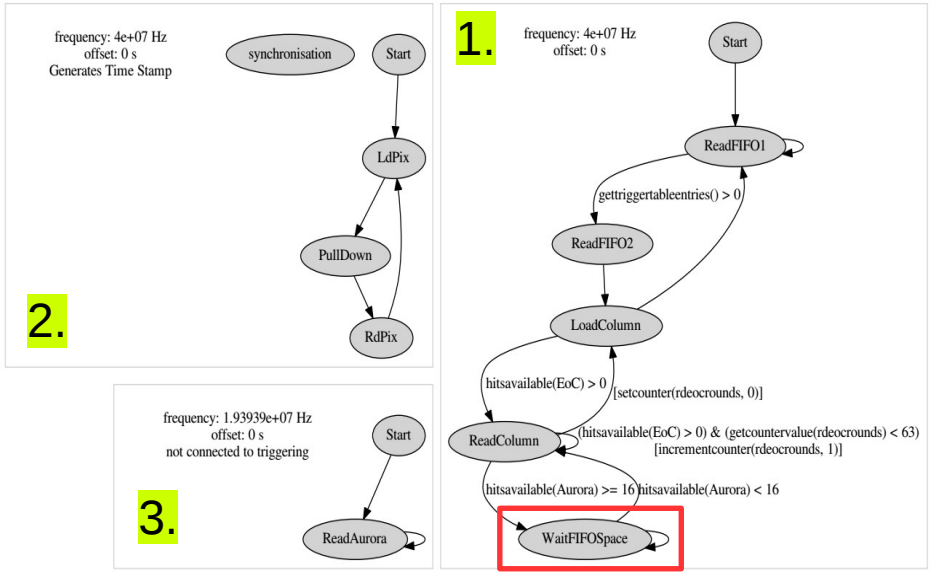


ASIC and Detector Lab at KIT
ROME

Available at: https://git.scc.kit.edu/jl1038/Readout_Simulation

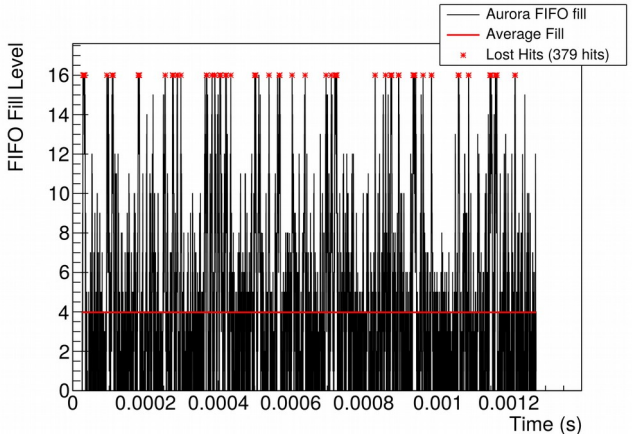
ATLASPix3 – State Machine Variations

- Idea: stop the readout of the Column Buffers to the Aurora FIFO if it is full
  - One additional state in state machine 1
- Effect:
  - State Machine 1 can run faster than state machine 3
  - Compensation for fluctuating number of hits per time

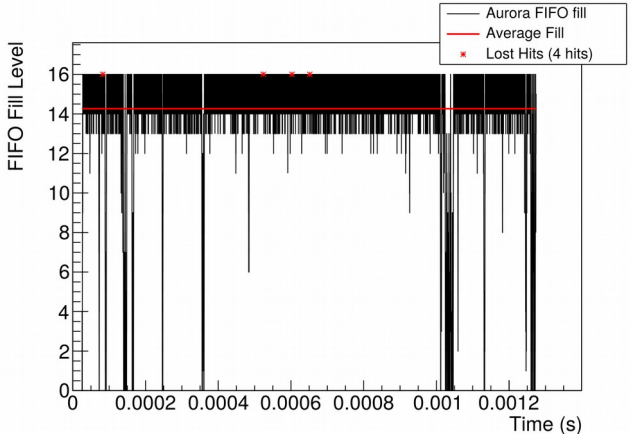


Effects of State Machie Changes – Aurora FIFO

- The Waiting State pauses the writing of hits to the Aurora FIFO
- for 64 bit data sets
- The 4 remaining lost hits originate from the implementation (End-of-Event Word sent in LoadColumn state)
- Better utilisation of output bandwidth



No waiting state



With waiting state

120 buffers/column, 40 MHz readout, 3 MHz trigger rate, 16 buffer trigger table