Towards a working demonstrator

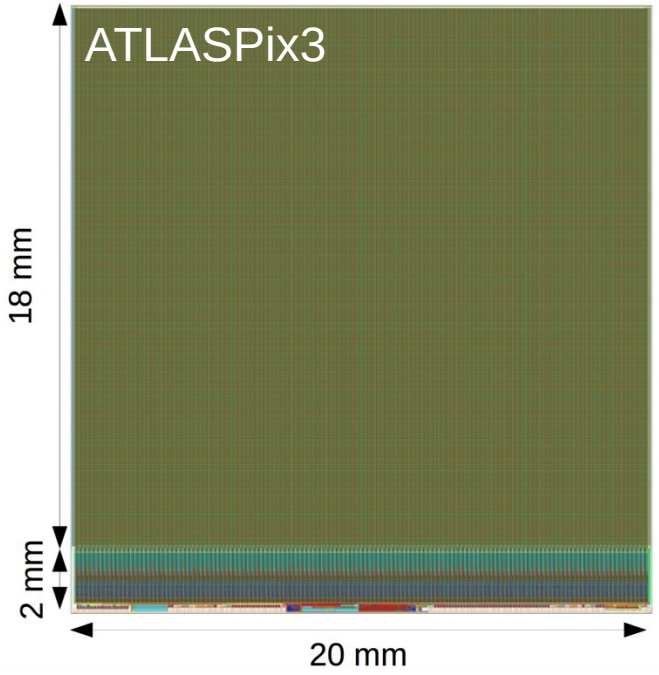
(a CEPC Tracker demonstrator that is)

Jens Dopke, Daniel Muenstermann

2019: “Summary and Prototyping Proposal”

- We seem to already have in hand everything that it takes to build a competitive, light and cost-efficient CEPC tracker
  - why don't we build a prototype “stavelet” to demonstrate its feasibility?

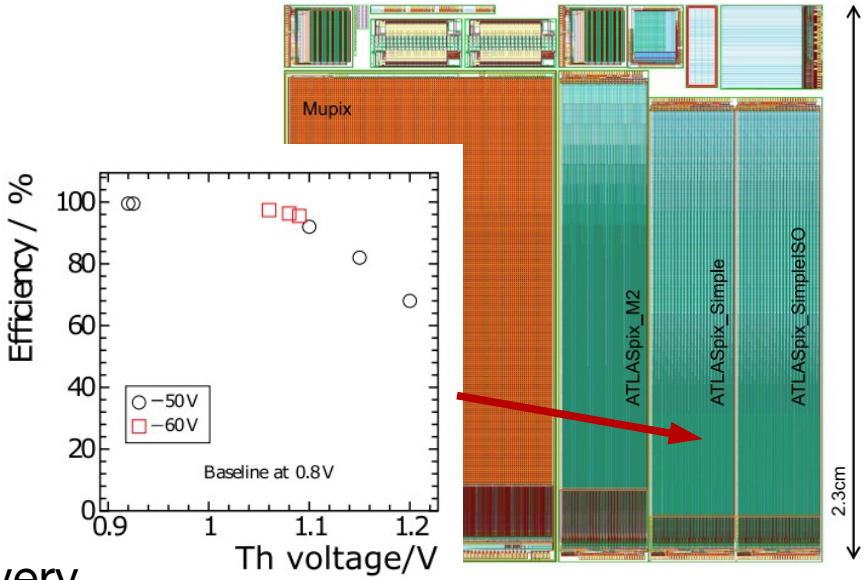
- We propose to
  - use the full-size monolithic CMOS chip ATLASPix3 as a starting point to gain some experience
  - submit a refined/optimised “CEPC-TPix” (“Tracker-Pixel”!) within the coming months to take into account the CEPC specifics
  - **aim to port the HV-CMOS production to a Chinese foundry for the production stage**
  - build prototype modules based on ATLASPix3
  - build a stavelet (short stave) based on the Alice/ATLAS truss approach
  - populate the stavelet with modules to arrive at a fully functional prototype(let)



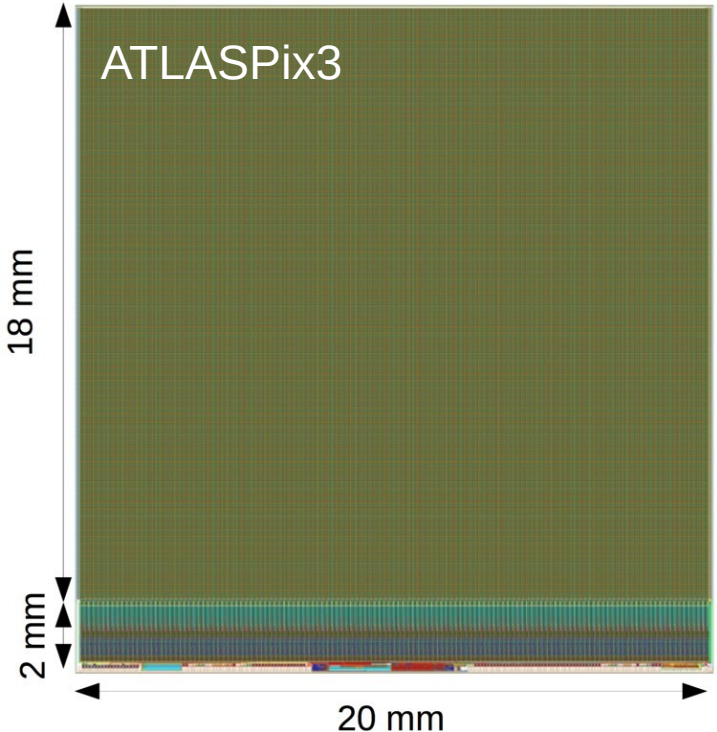
- With our proposal we would like to kick-start R&D and prototyping for the (outer) tracker, not compete with ongoing efforts for the VTX
- Interested parties are very welcome to join in!

What do we have in hand for the tracker?

- Monolithic HV-CMOS detectors
  - From ATLAS Pixel CMOS R&D: ATLASPix
    - ensures 25ns timing compliance
    - hit efficiency 99.5%
    - pixel size 50 µm by 150 µm (or smaller)
    - triggered or triggerless readout possible
    - 1.25 GBit/s downlink
    - Reticule size: about 2 cm by 2 cm
    - Full-size chip (ATLASPix3) just submitted, delivery ~July 2019
  - Monolithic CMOS allows to produce large areas fast and cheap
    - No hybridisation – wirebonds or C4NP bumps possible
    - Production capacity of typical CMOS foundries: some 10.000 wafers/month
    - 100 m^2 ~10.000 wafer (with yield and spares)
    - Typical price: o(1000 EUR/wafer) for large quantities, depending on the process and details

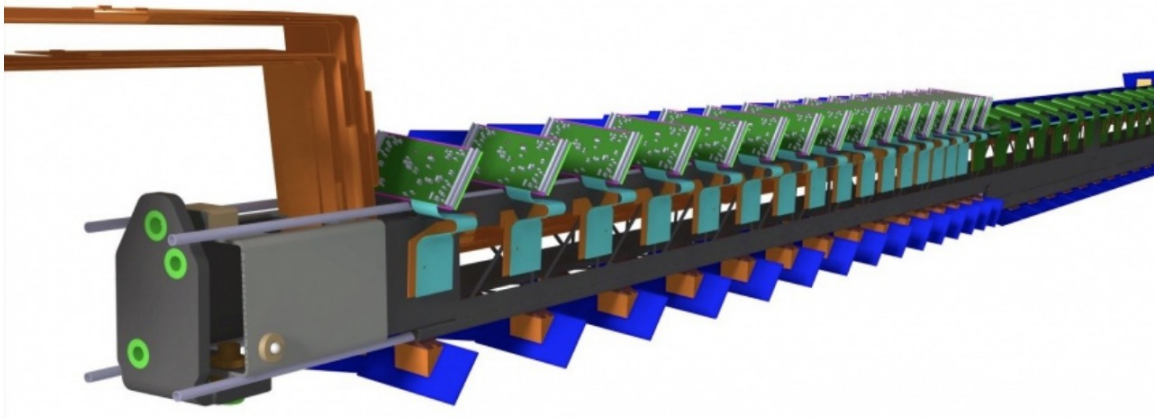


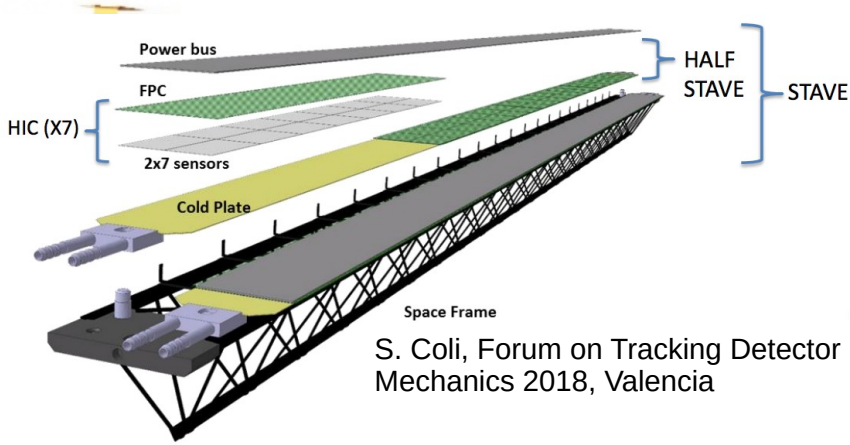
I. Peric et al., NIM A 924 (2019) 99



What do we have in hand for the tracker?

- Module construction
  - Experience from Alice ITS and ATLAS Pixel CMOS R&D
  - Alice ITS uses automatised approach for module assembly (Alicia) → scalable, reproducible, little "handcrafting"
  - No hybridisation, even wirebonds may be avoidable
- Local supports
  - Experience from Alice ITS OB staves (trusses)
  - Inspired ATLAS Pixel outer barrel structures
    - includes CO_2 bi-phase cooling using Titanium pipes
    - includes "inclined" layout to optimise material
    - evolved manufacturing process allowing for larger production speed





S. Coli, Forum on Tracking Detector Mechanics 2018, Valencia

https://www.unige.ch/dpnc/en/groups/giuseppe-iacobucci/research/slim-mechanics/

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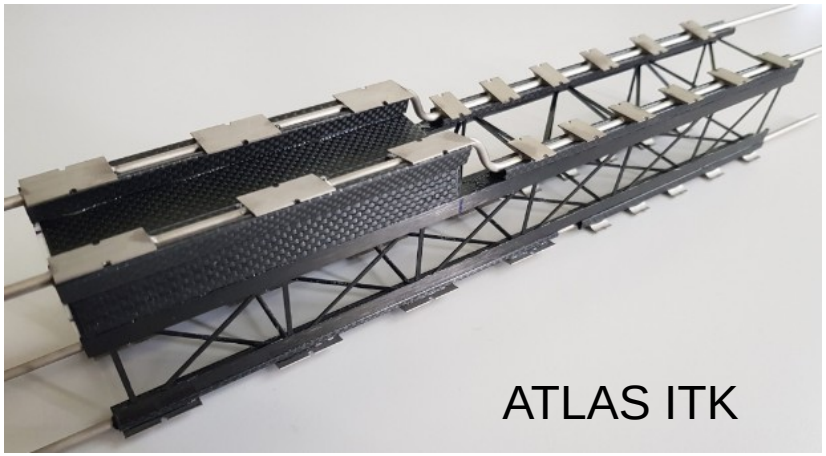

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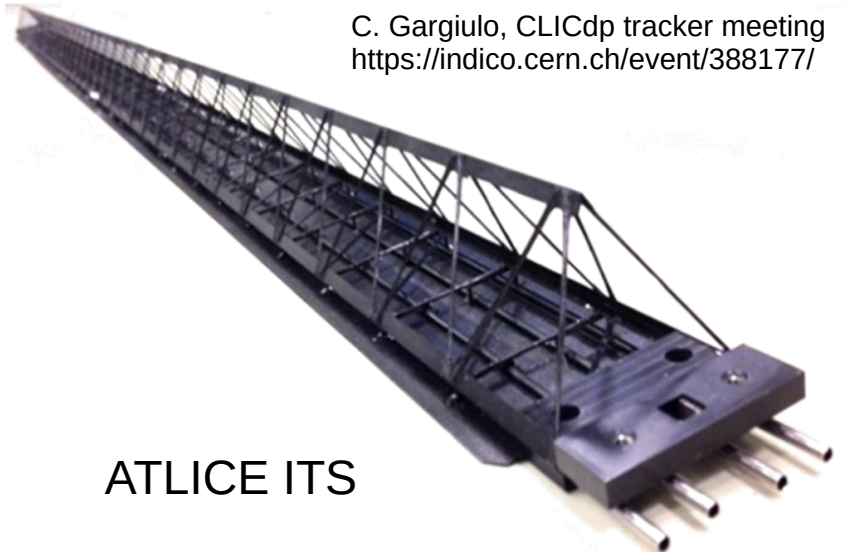
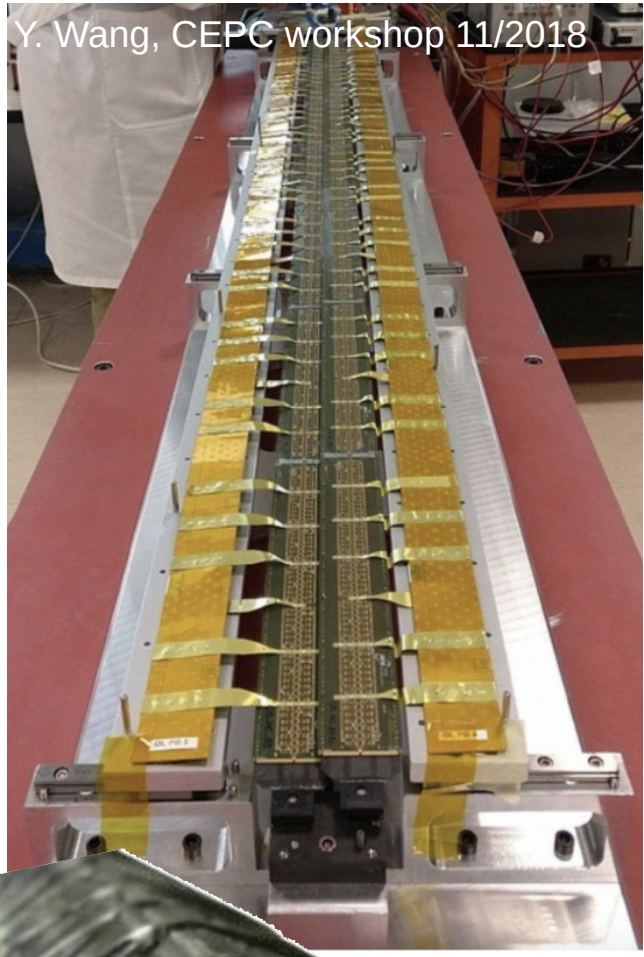
C. Gargiulo, CLICdp tracker meeting
https://indico.cern.ch/event/388177/



What do we have in hand for the tracker?

- Stave loading
  - Experience from Alice ITS: STFC Daresbury Laboratory and CCNU are ALICE ITS loading sides
  - Effort is scalable
- Cooling
  - Experience with bi-phase CO2 cooling in thin-walled Titanium cooling pipes from ATLAS IBL and ITK
    - carbon-foam for heat spreading, carbon foam and faceplates for stiffness
  - Experience with Alice ITS monophase leakless water cooling with polyimide pipes
    - graphite foil and thermal prepreg for heat spreading, truss-based space frame for stiffness
  - Monolithic CMOS allows for a large Delta-T



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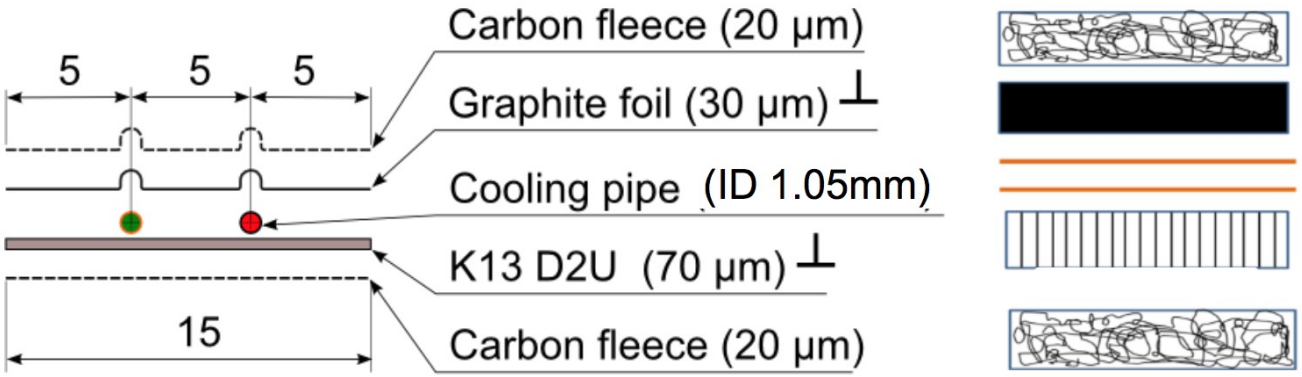

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Requirements in detail

- 25ns bunch spacing
  - default for ATLAS, with much higher occupancy and triggered readout
    → can take a monolithic ATLAS CMOS chip as starting point
- o(100m^2) area
  - o(10.000) 8” wafer (including yield and spares), should result in o(1000 EUR/wafer)
    - could be a bit cheaper, but order of magnitude is correct
    - 12” wafer might help
  - capacity of typcial foundries o(kWafer/month)
- <50µm pitch
  - submitted: 50µm x 150µm, design exists for 25µm x 300µm
- Readout speed: 1.25 Gbit/s demonstrated, triggerless readout available
- Material budget
  - 0.65-1% (?) X/X0 seems not unrealistic compared to what has been achieved
  - Chip runs at room/elevated temperature! Large Delta-T possible
    → no pipes?

Let's get more concrete...

- Up to now: naive (?) proposal from 2019, trying to recycle as much as possible to save cost and effort (as we have no funding)
- Has anything changed?
  - Quite a bit of additional interest in the UK and in China
  - But still no additional funding, i.e. also only limited manpower
  - So we might be able to do a little bit more, but not much
- What is realistic?
  - use ATLASPix3-based modules from the ATLAS efforts
    - not ideal, as we might not want “quad modules”, but rather a fully integrated stave a la ALICE – but we get them “for free”
  - use a stave(let) that we can build – so probably similar to an existing ATLAS or ALICE stave
    - close enough to X/X0 requirements for CEPC?
    - do we need realistic cooling? (CO_2 plant?)
- What do we want to demonstrate?
  - A HV-MAPS-based stave with 25ns time resolution that we actually have in hand?
  - A stave (cooling/readout) concept that fulfils the X/X0 requirement? Is this requirement well justified?

Work sharing

- So if this is the way for us to go – how do we share the work?
  - Bristol:
  - Edinburgh:
  - Daresbury:
  - Lancaster:
  - Liverpool:
  - Sheffield:
  - QMUL:
  - RAL:
  - Warwick: