

2nd UK Workshop on Silicon Tracker for a e^+e^- Collider

Introduction and Overview

1. Welcome
2. CEPC news: Prof. Joao Guimaraes Da Costa (Chinese Academy of Sciences)
 - Snowmass process
3. Silicon Tracker News
 - New Chinese & Italian collaborators
 - ATLASPix3 sensors: delivery and order
 - Readout systems: KIT PCBs, YARR & Caribou
 - Quad flexes
 - Sensor evolution: New “MPW” submission and Chinese fab
4. General discussions for UK collaboration and next steps
 - How do we present ourselves to the outside world?
 - Meanwhile: Snowmass, LHCb, eIC
5. Tracker prototype specifications
 - Next technical steps

CEPC organisation

UK mailing list:

FCEPC-GENERAL@jiscmail.ac.uk

SiTracker meetings & mailing list:

cepc_cmos_tracker@maillist.ihep.ac.cn

<https://doodle.com/poll/7yxeycpavqk75t95>

Should we extend this for a 7am option?

General detector meetings & mailing list

Wednesdays, 8am

cepc-physdet@maillist.ihep.ac.cn

CEPC Days

cepc-general@maillist.ihep.ac.cn

Workshops: Shanghai

October 26-28 2020, Shanghai

<https://indico.ihep.ac.cn/event/11444/>

Looking for session convenors

New Italian collaborators

Italy had put in a proposal for a Silicon Tracker at the same time as us.

Their proposal is well aligned with ours.

Como, Massimo Caccia, CMOS sensor test, strip options

Milano, Attilio Andreazza, CMOS sensor test, CMOS module assembly, strip options, (mechanics and cooling)

Pisa, Franco Bedeschi, mechanics and cooling

Torino, Manuel Da Rocha Solo

CMOS sensor design

- Italian sensor development: ARCADIA
- Quad flex for ATLASPix3
- Carbon fibre support structure (CMS)

ATLASPix3 sensors and orders

1 Wafer (about 40 chips) available. Todo: Cutting, dicing, distribution

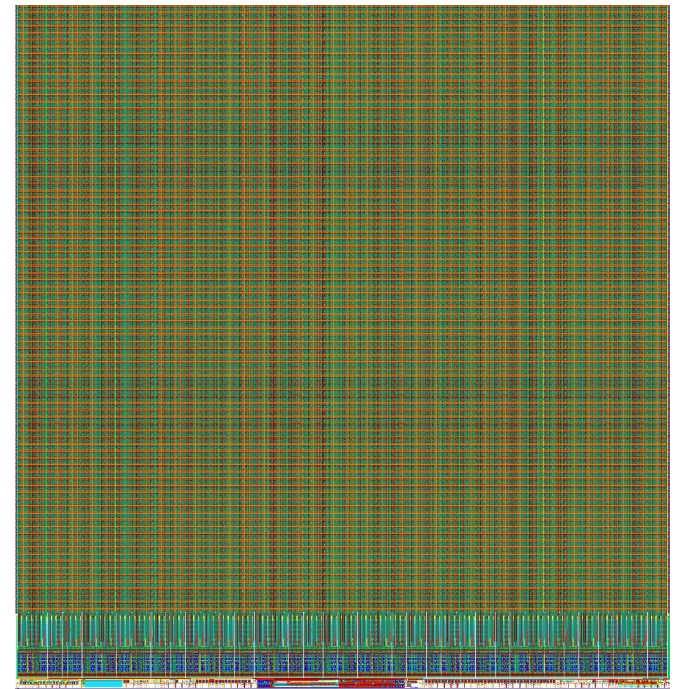
A new order of 25 wafers is planned

Total cost is around £2k / wafer

We could use O(10) for the SiTracker project, shared between UK, China and Italy (and US?).

Any takers or contributors?

ATLASPix3



Readout systems

1. KIT system

The KIT system is a working system, well adapted for ATLASPix3, has been used for a beam telescope. Is relatively cheap.

Contains a single chip board, Gecco readout card, register cards. 40 PCBs on order.

Needs a FPGA card.

10 institutes are interested in the KIT system

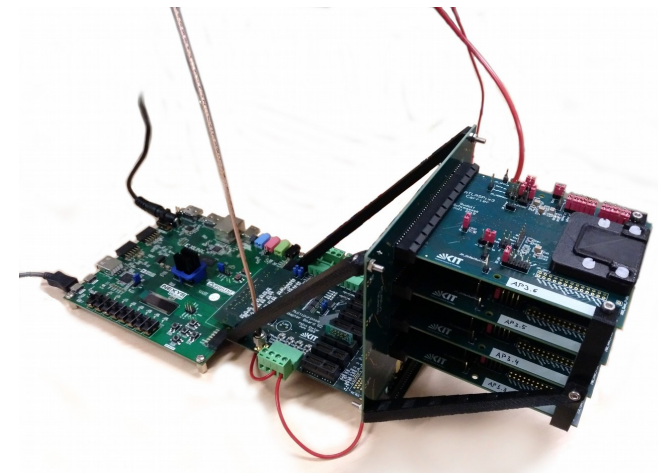
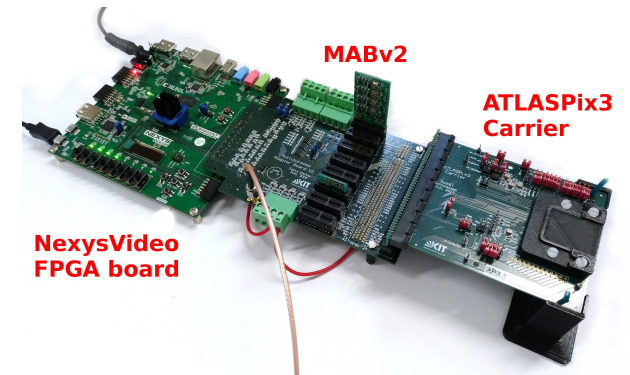
2. YARR

Medium priced system, works for ATLAS, not adapted for ATLASPix3, very powerful.

3. Caribou


Expensive system, very powerful, adapted for ATLASPix3, integrates into FELIX.

New Car boards on order.



Flex: Milano Design for a Quad Module

ATLASPix3 Flex V1.0

Title ATLASPix3 Flex		Istituto Nazionale di Fisica Nucleare Via G. Celoria, 16 20139 Milano ITALY		
Size: A3	Revision: 1.0			
Date: 04/12/2019	Sheet 1 of 6			
Author: F. Sabatini	Email: fabrizio.sabatini@mi.infn.it	Tel: +390250317390		

Page 1 Main

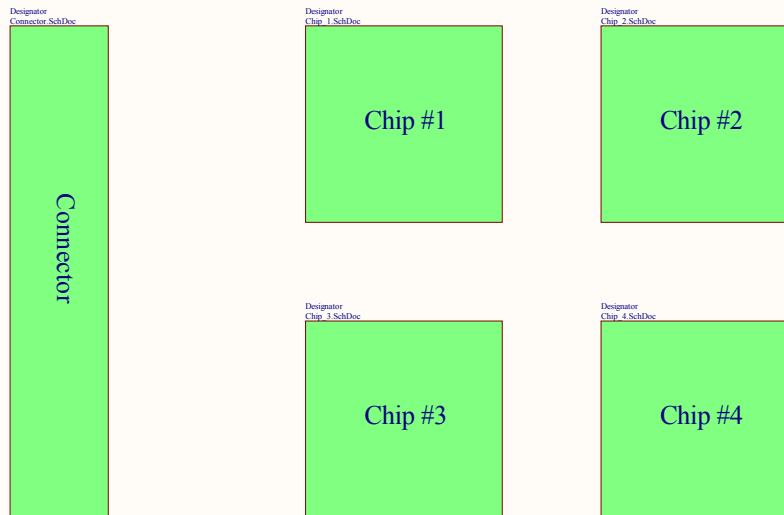
Page 2 Connector

Page 3 Chip #1

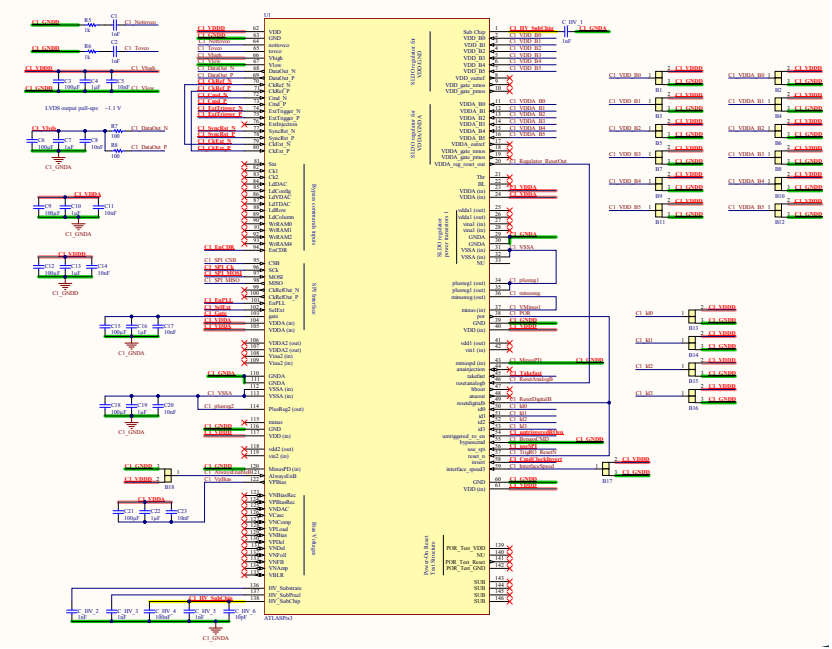
Page 4 Chip #2

Page 5 Chip #3

Page 6 Chip #4



Chip #1



Fully functional design for readout.

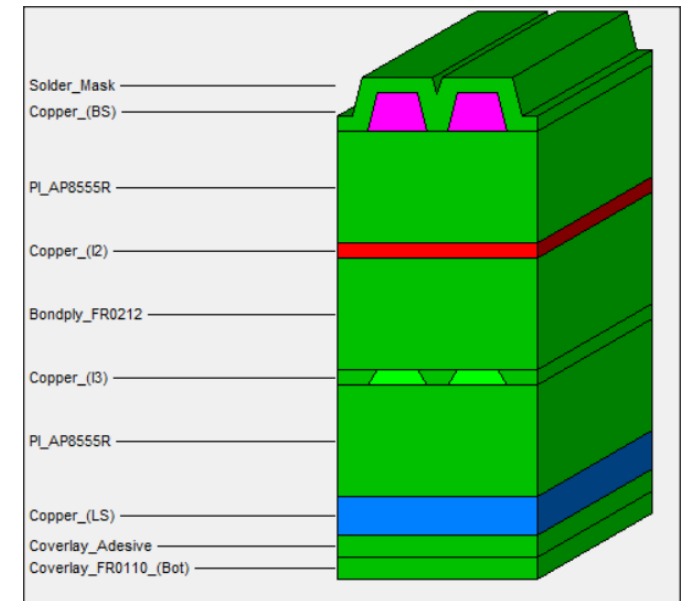
KISS (Keep It Simple and Safe) for first attempt:

Direct powering

Not optimised for low material

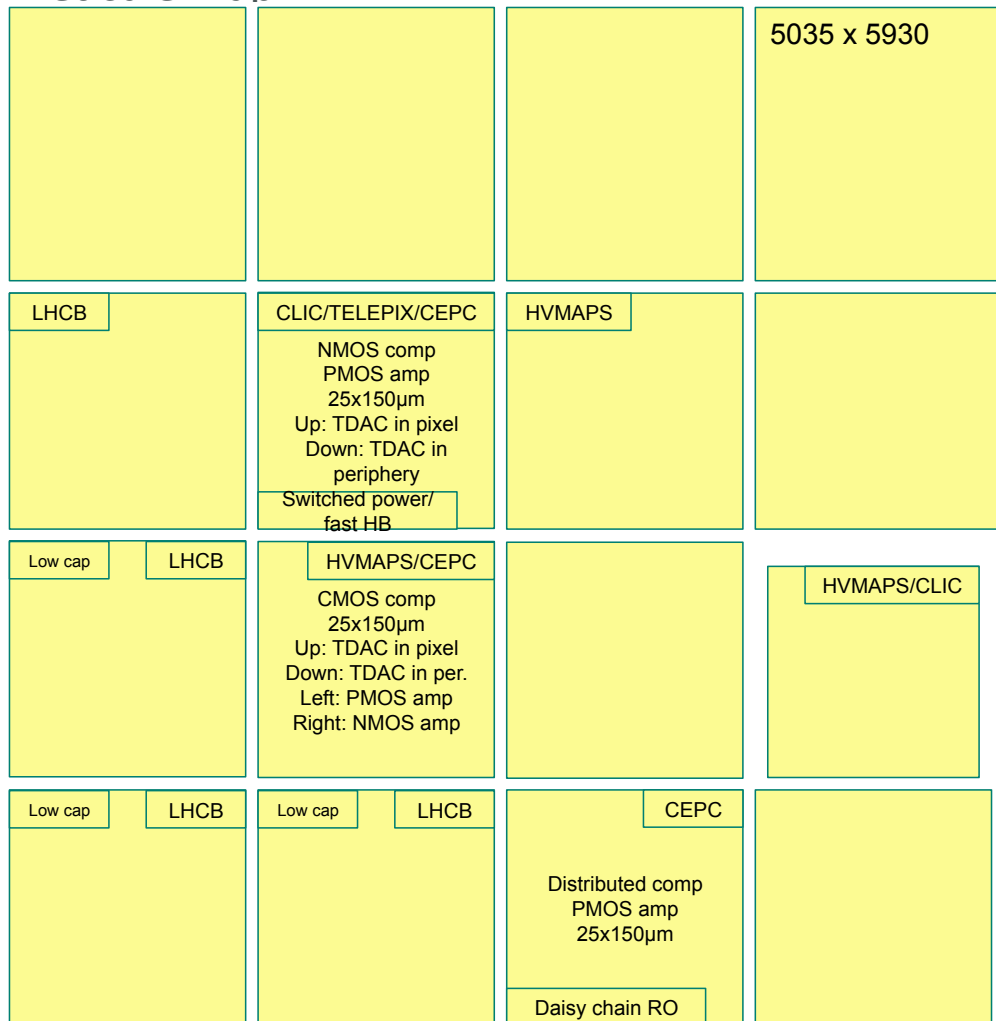
Reduced configuration parameters

Look at **serial powering** in parallel



Engineering run planned for April this year(?)

Reticule map:



Collaboration with **LHCb Mighty Tracker** and other projects.

CEPC institutes make a **significant contribution** to the cost of the submission.

Test evolvment of ATLASPix3:

Smaller pixel size (**25µm**) in ϕ direction

Lower capacitance

Amplifier and comparator design

Electronics in **pixel or periphery**

Daisy chain of readout

Looking at processes with Chinese vendors **HHGrace**, Non disclosure agreement in preparation.

SMIC; talk to agency. 40nm and 55nm processes very interesting.

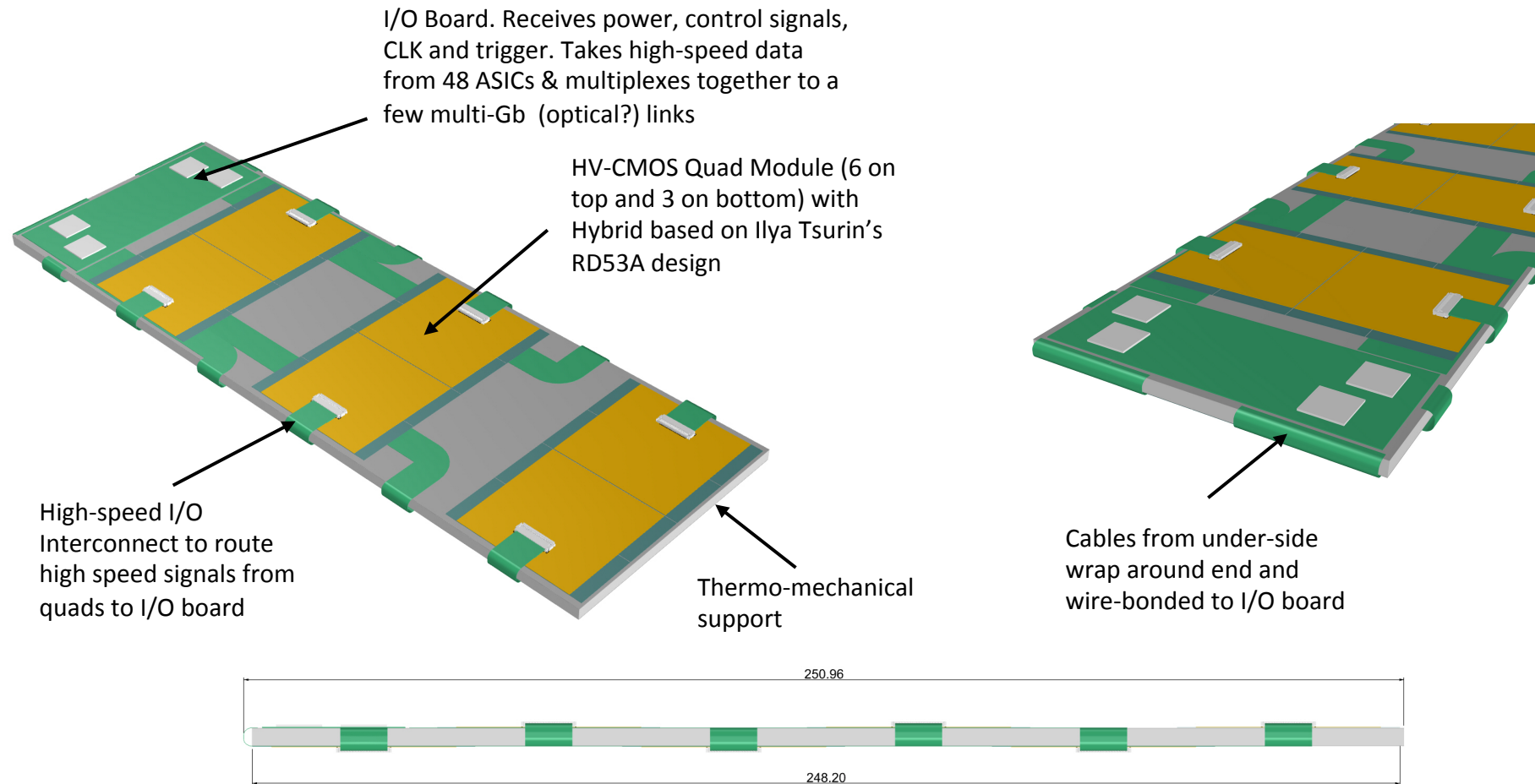
Backup

Module / Mini Stave: FEA Simulation



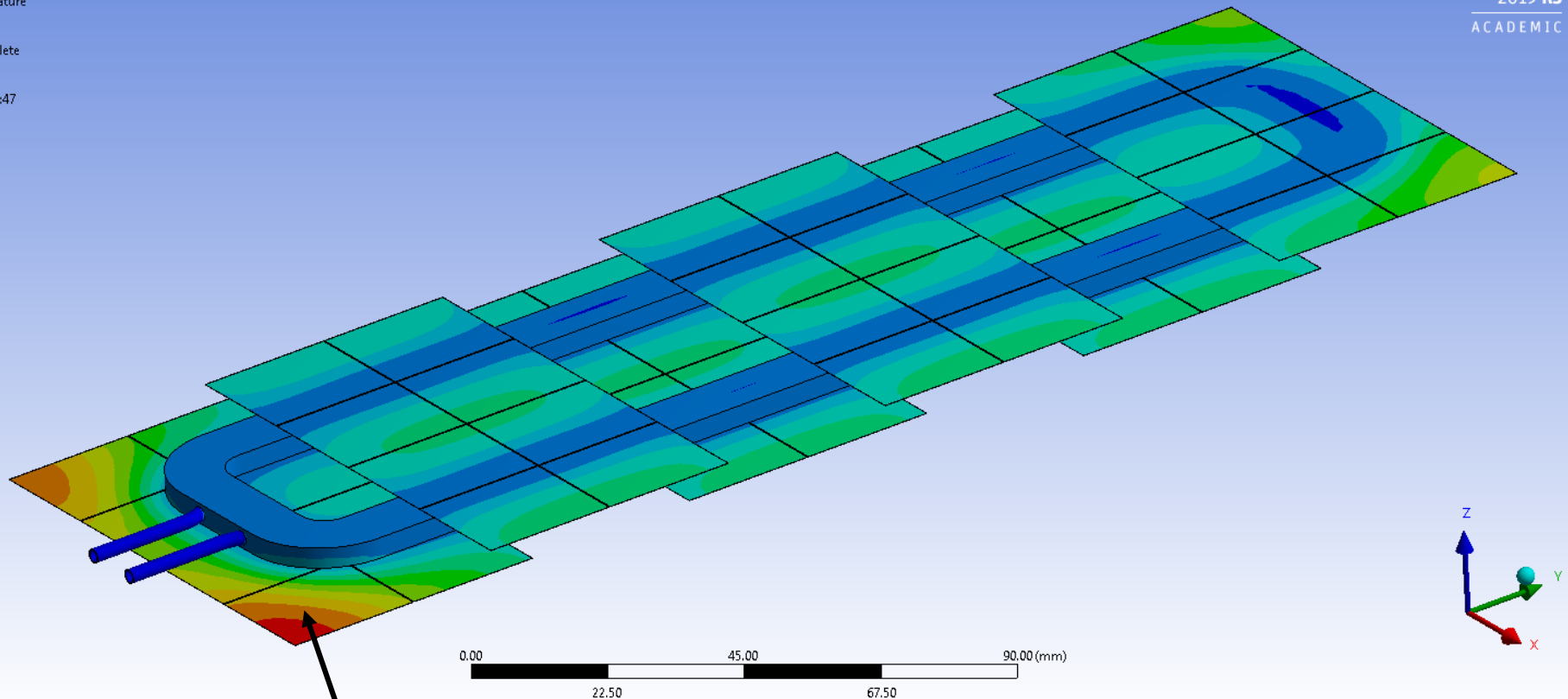
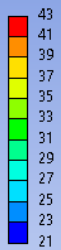
UNIVERSITY OF
LIVERPOOL

Tile Conceptual Design





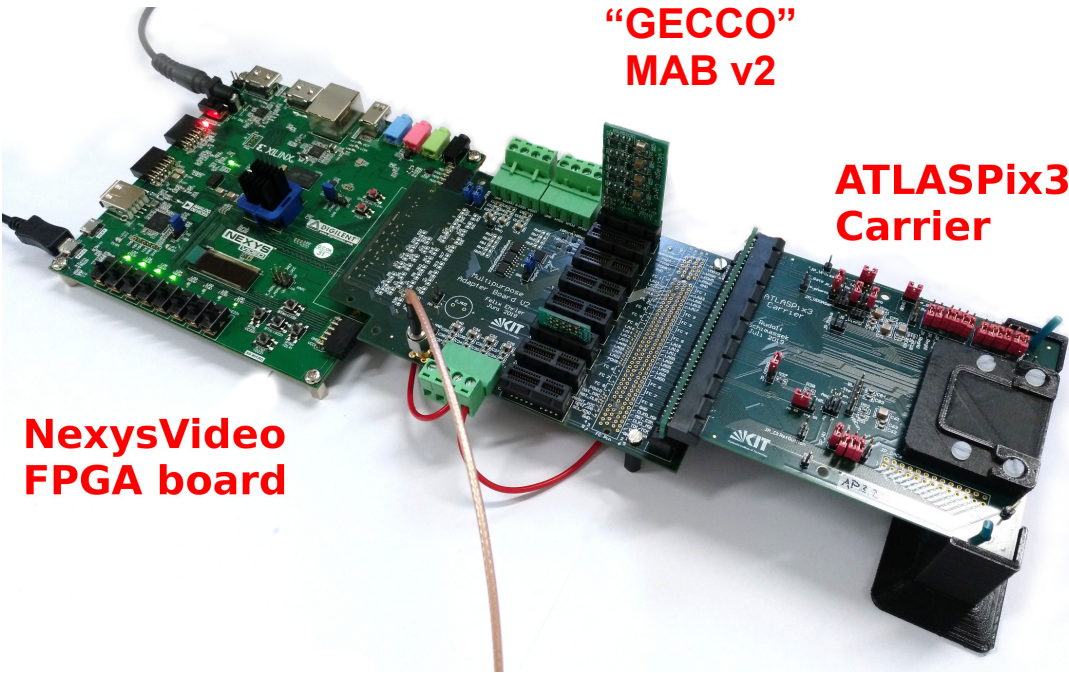
A: Steady-State Thermal
Temperature
Type: Temperature
Unit: °C
Time: 1
Custom Obsolete
Max: 43.8
Min: 22
27/01/2020 15:47



Add thermally conducting foam
in corners

Readout Systems: KIT single chip board

Starting point is the **ATLASPix3 single-chip card** produced by KIT and used for the tests



Gerber files for GECCO and function cards are available. Looking for a vendor (in China) for **production of more readout systems.**



DAQ: YARR

Yet Another Rapid Readout

<https://iopscience.iop.org/article/10.1088/1742-6596/898/3/032053>

YARR is a small **self-contained DAQ system**.

Linux PC with a x4 **PCIe slot for the FPGA card**

FPGA card: e.g. **Trenz TEF1001**, XpressK7,...

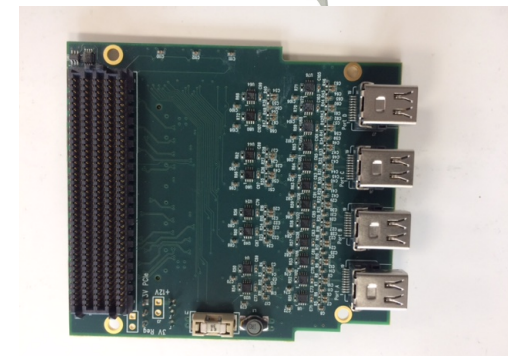
FMC cards for FE-I4 and RD53A

Up to **1.6GBit/s possible** with this setup.

We have used the YARR readout with a digital RD53A module in **Lancaster & Edinburgh**.

Todo: Adaptation to ATLASPix3 necessary:

- **FMC**
- **Software**



CaRIBou Readout System

UniGe+BNL development

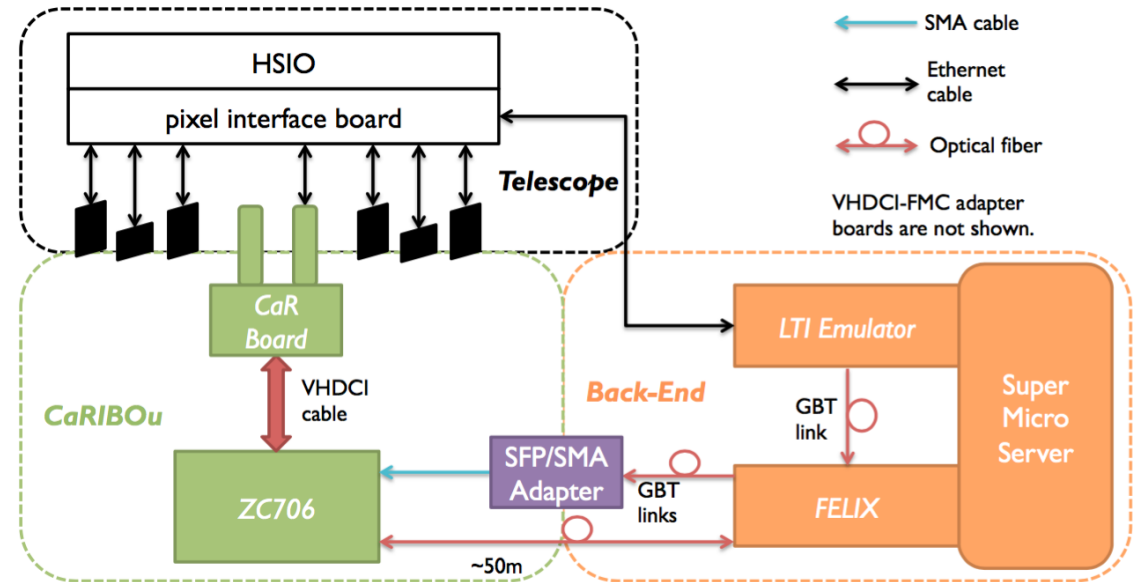
ZC706 + CaR-board based

ATLASPix3 is implemented,

Continued support thus unclear

Comparatively expensive (~4kEUR)

Integrates with **FELIX**



Mathieu Beliot, AMSH18 results

Currently an **order for more** (and slightly updated) **CaR**-boards is prepared by CERN.

4 CaR boards have been requested for us.

A long-term major redesign of CaRIBou is underway, with the goal of replacing the (comparatively expensive) KC706 board.

Summary and Conclusion

Sensor:

Functional ATLASPix3 sensor available for prototyping
 Optimisation for a (Chinese) e^+e^- collider

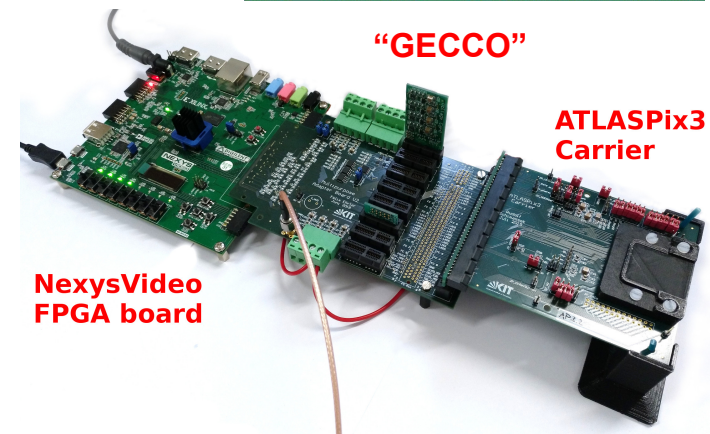
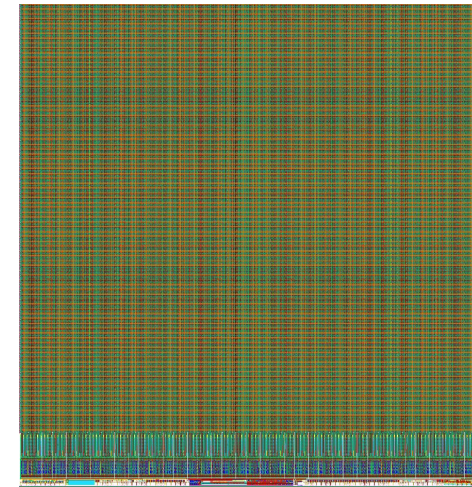
- Power consumption
- Investigate and work with Chinese foundry

Readout:

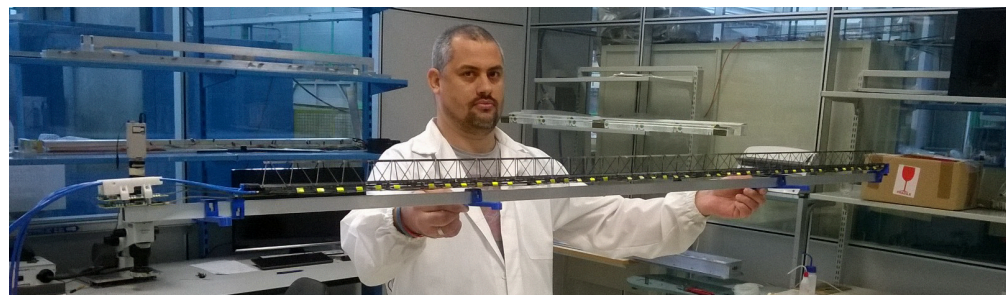
Flex design well progressed
 Follow up with all three alternatives.
 Distributions of readout systems to interested institutes

Staves:

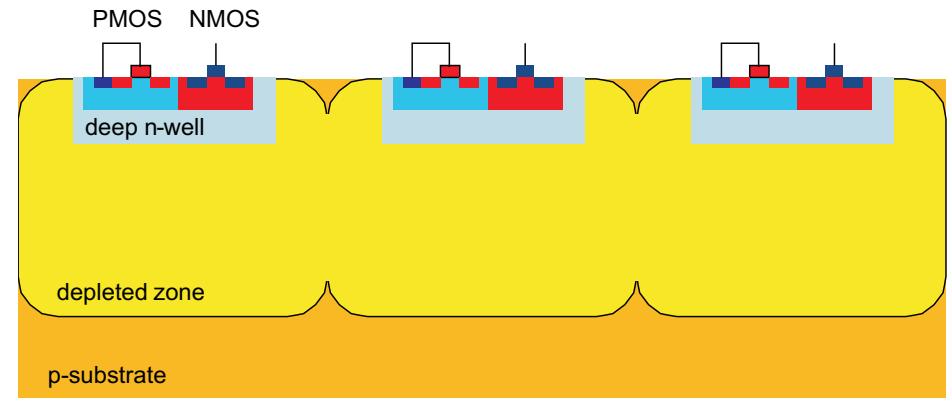
Experience with ALICE (and ATLAS) module staves
 We need a new stave design for the ATLASPix modules, geometry and material requirements
 We have approached a local (Beijing) company to design & fabricate the **truss supporting structure with carbon fibre**



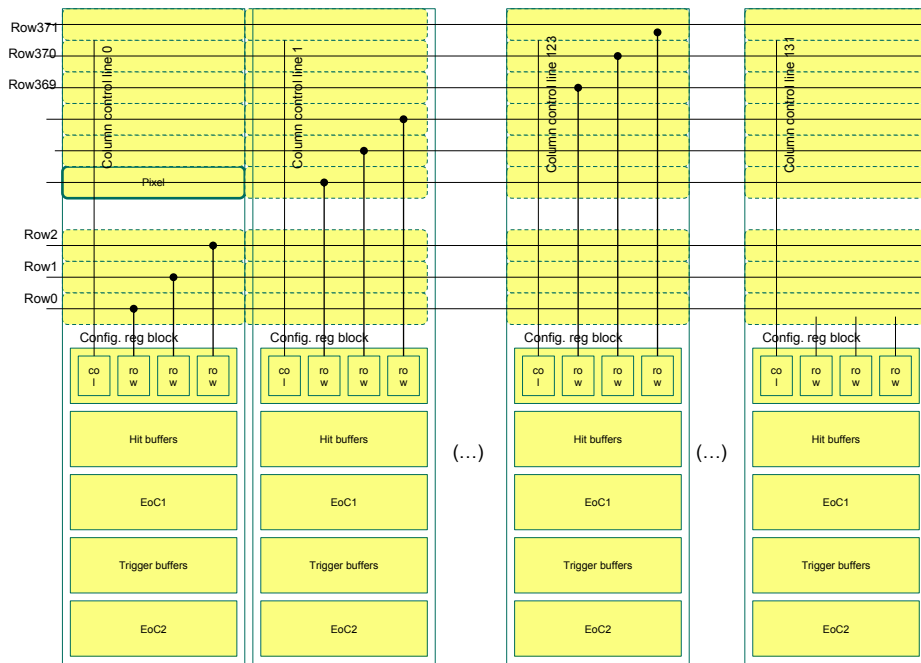
ALICE stave at Daresbury



HV-CMOS structure



Block scheme of the pixel matrix and column circuits



Pixel Schematics

