



ATLAS Pix3 based tracker demonstrator discussions

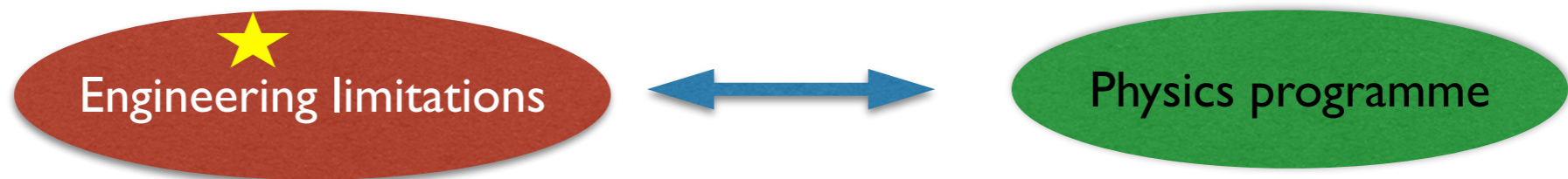
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Second UK workshop on HV-CMOS tracker for e^+e^- colliders, 1-June-2020

Starting point

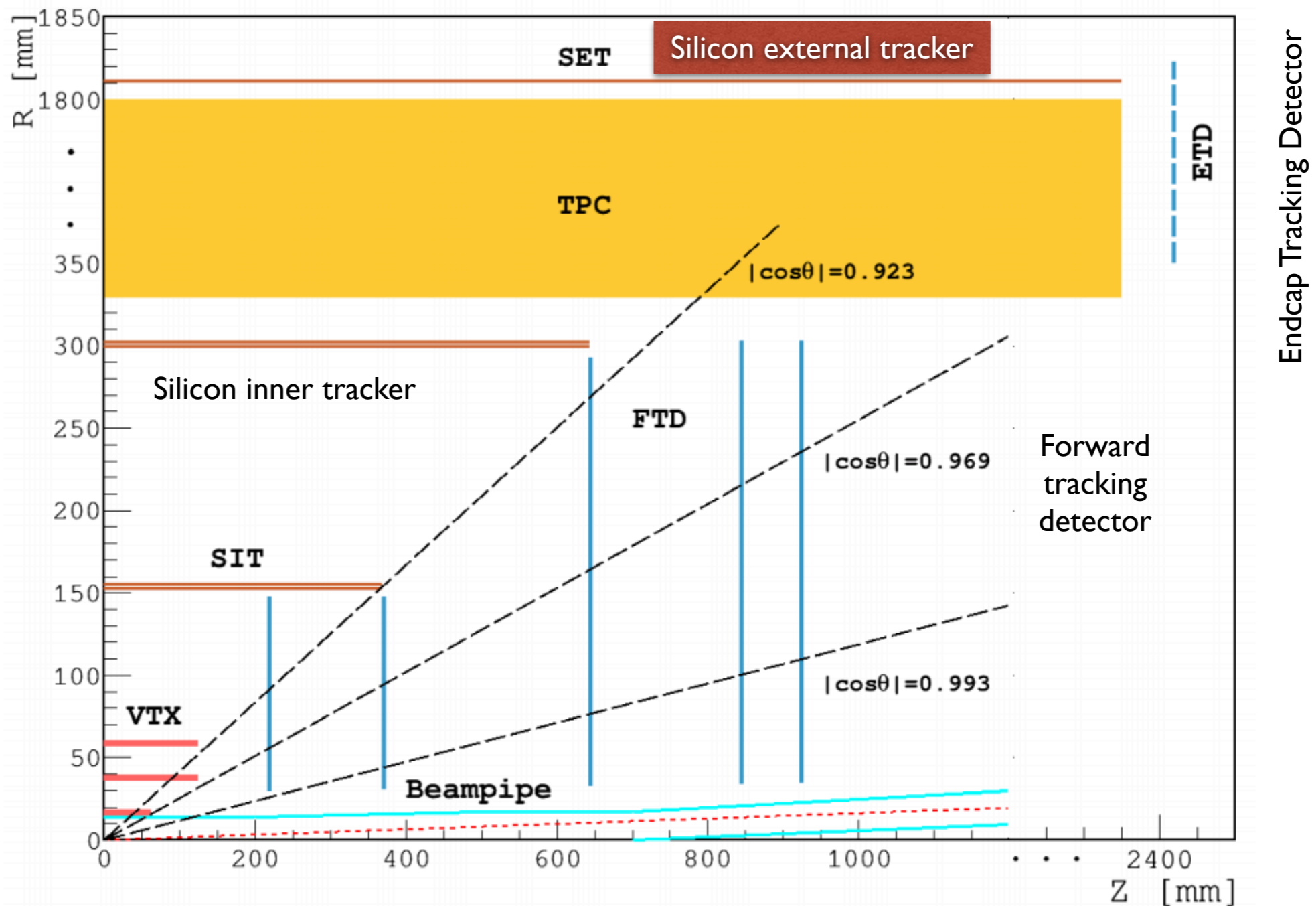
- There is essentially NO specifications on the tracker
 - A wishlist can be found via the CDRs from various proposals



- Goal of this demonstrator
 - Establish what can be achieved using the state-of-the-art solutions
 - We simply do not have resources (mostly limited by staff time) to do further
 - Define the challenges and directions for future R&D with more funding/staff time
 - At the end (~end of 2022), we will have a credible, UK unique, and flexible programme
 - Suitable for large area application for any e⁺e⁻ collider experiment
- What drive the key considerations for demonstrators?
 - Large area applications: low power, scalable, and modular
 - A long-term UK strategy on the HV-CMOS program

The “Baseline” Tracker in CDR

Caveat:
baseline is really just a starting point, fresh physics and R&D program are ongoing to redefine this



Except FTD 1+2, all use 2 layers of **back-to-back mounted single-sided strips at an stereo angle**
 Sensor: $10 \times 10 \text{ cm}^2$, pitch $50\mu\text{m}$, Thickness $<200\mu\text{m}$
Strip design with $\sim 300\text{-}400 \mu\text{m}$ thickness per layer alone gives $0.3\text{-}0.4\%$ X_0
Effective silicon area for strip: 160m^2 , pixelated design reduces to 80m^2

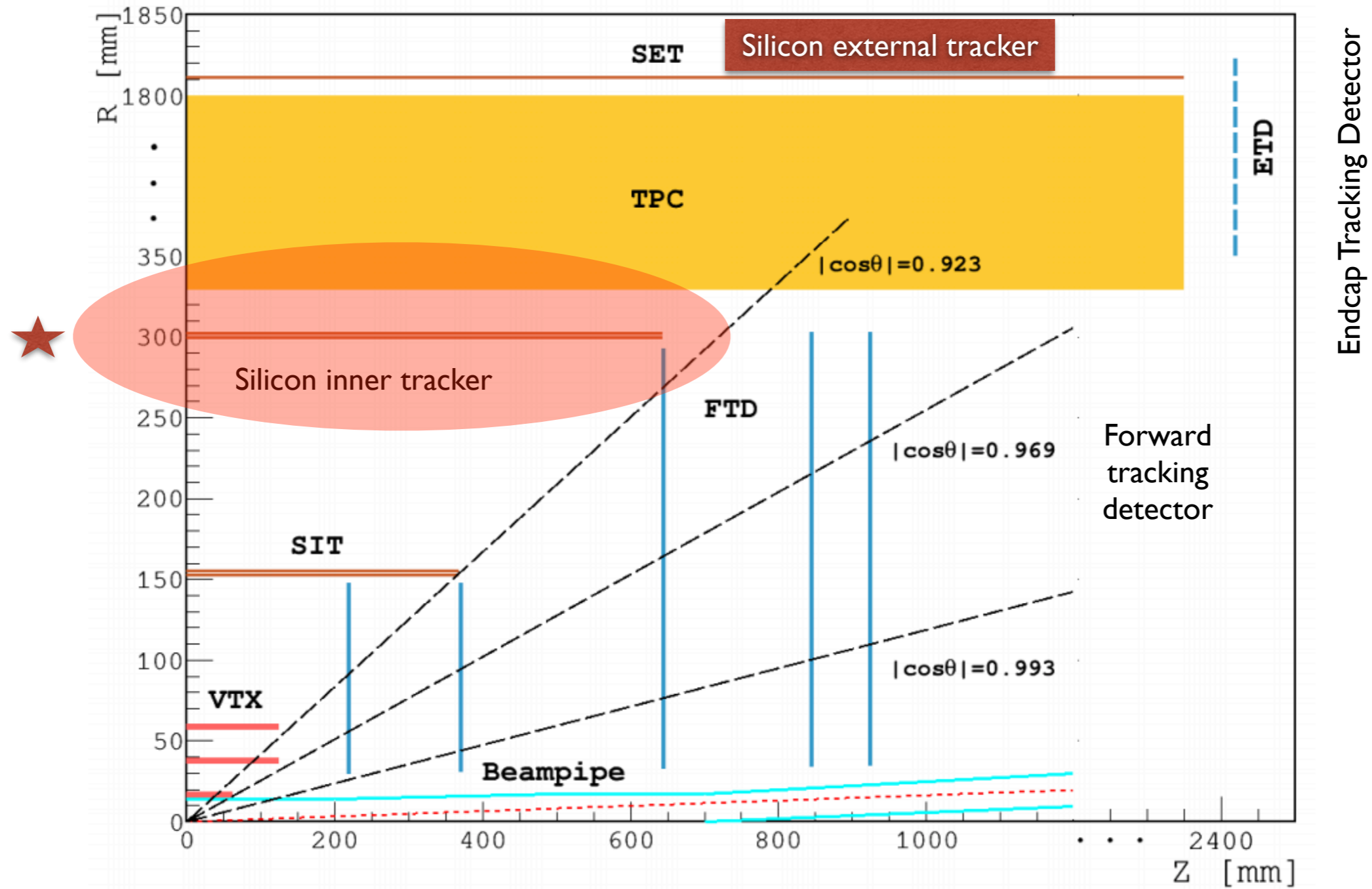
Closer look

	With TPC	All silicon
Barrel	SIT-L1: $R=0.15\text{m}, L=0.75\text{m} \rightarrow A=0.7\text{m}^2$ SIT-L2: $R=0.3\text{m}, L=1.33\text{m} \rightarrow A=2.5\text{m}^2$ SET: $R=1.8\text{m}, L=4.7\text{m} \rightarrow A=53\text{m}^2$?
Endcap	FTD D1-D5: 1.8 m^2 ETD: $R_{\text{out}}=1.82\text{m}, R_{\text{in}}=0.42\text{m} \rightarrow A=20\text{ m}^2$	
$\sigma_{\text{SP}}(r\phi)$	7 μm	
$\sigma_{\text{SP}}(z)$	Very loose $\sim 100\text{ }\mu\text{m}$	
Timing	25 ns	
Max* Occupancy	SIT-L1: 0.6%, SIT-L2: 10^{-3} , SET: 10^{-4}	
Radiation	TID $\sim < 1\text{kRad/year}$, NIEL $\sim < 10^{10}$ MeV neq / $\text{cm}^2\cdot\text{year}$	
dE/dX	-	2-3% @ p_T [2-10]
X/X_0	0.65% Barrel 0.5-0.65% Endcap	?

- SET+ETD: 73 m^2 out of the total area of 78 m^2
- Given the large difference w.r.t. the rest, we may end up with different technologies
- What are the realistic target we should aim for in this demonstrator?

*Assumption: Pixel dimension: $50\text{ }\mu\text{m} \times 350\text{ }\mu\text{m}$, readout time: 10us, Cluster size: 9 hits per track

The “Baseline” Tracker in CDR



December 2019 discussions (in RAL)

- Tracker prototype deliverables (2 Year plan)
 - A local support structure with sensors on
- Short-term milestones
 - 2-3 Quads with Zif connectors?
 - CF space frame - Hongbo
 - Cold plate
- Long-term R&D considerations
 - New sensor/chips
 - Chinese fab
 - Aluminium flexes?
 - Copper (1oz/ft², 35um thick) is about 0.2% radiation length
- Impact of the alignment on the overall tracker design
- Full size support for the outer layer

[Link to discussion google doc](#)

Goal for today's discussions

- We hope to converge on a set of **essentials** and **desirables** in the following 4 areas
 - Sensor and chips
 - Electrical and system
 - Readout and DAQ
 - Mechanical support structure

Sensors and chips

- Essential
 - ✓ ATLAS Pix3
- Desirables
 - Contribute to the subsequent engineering runs and submissions

Electrical system: Tile concept proposed by Tim Jones

- See talks by Tim in the last UK meeting [Link to Tim's talk](#)

Tile Conceptual Design

Overall: 8cm × 35cm

I/O Board. Receives power, control signals, CLK and trigger. Takes high-speed data from **48 ASICs** & multiplexes together to a few multi-Gb (optical?) links

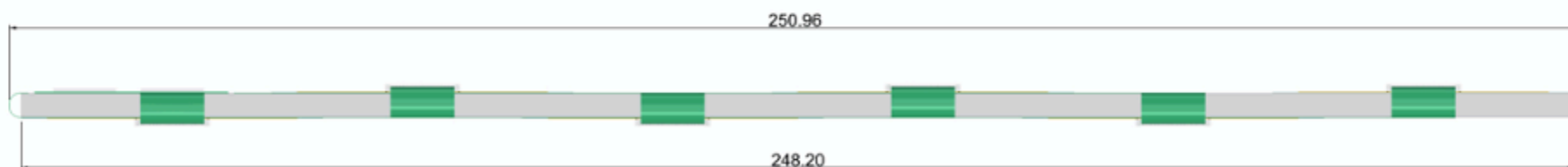
HV-CMOS Quad Module (6 on top and 3 on bottom) with Hybrid based on Ilya Tsurin's RD53A design

6 on bottom?

High-speed I/O Interconnect to route high speed signals from quads to I/O board

Thermo-mechanical support

Cables from under-side wrap around end and wire-bonded to I/O board



Electrical system

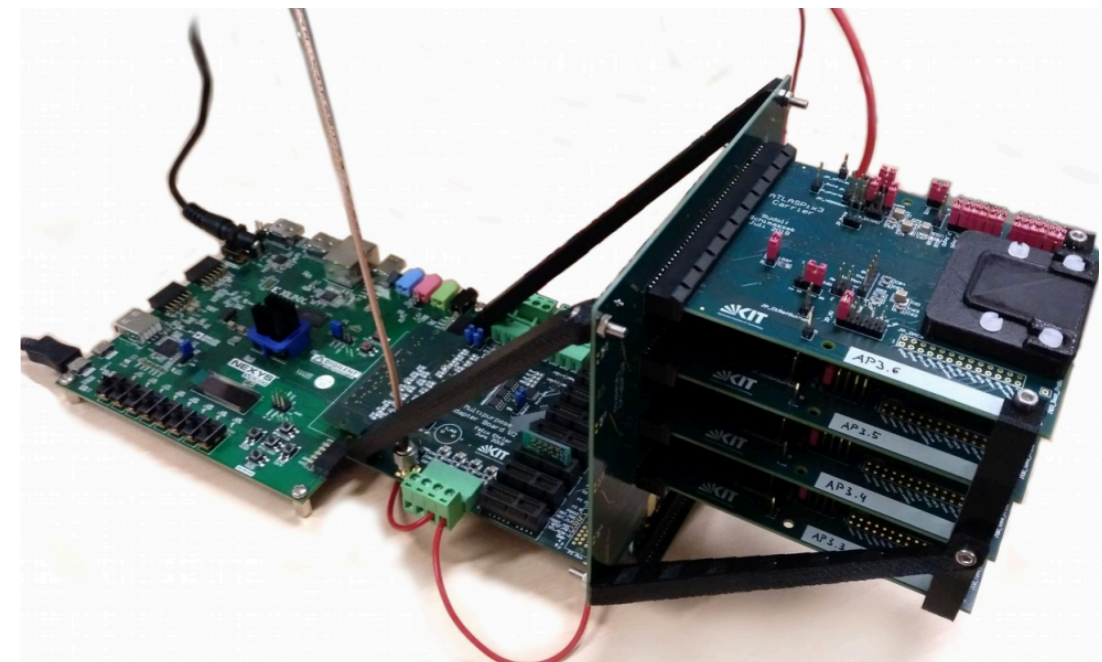
- We will start with charactering 1-2 quads
- Shall we aim to readout all 48 chips simultaneously
 - What can we gain in comparison to the 1-2 quad electrical modules
 - System design
 - First glimpse of potential service routing
 - Identify the “limit” of a modular design
- Essential electric solutions
 - Quad flex from Milano, see recent talks in [this link by Attilio Andreazza](#)
 - Bus-tapes
 - Is serial powering essential?
- Desirables:
 - Optical solution using GBTx or LpGBTx

Readout DAQ

- The KIT GECCO readout system
 - See Rudolf Schimassek's talks
 - [Link to CEPC tracker meeting talk](#)
 - [Link to UK e+e- collider HV-CMOS mtg](#)
 - Find out the max chips this can be configured
 - ✓ PCBs have been ordered



- YARR
 - Hardwares ready
 - Non-trivial firmware adaptation
- Caribou system
 - ATLAS Pix3 solution in principle ready
 - RD50 collaboration is organising purchase for the next version
 - Most UK institutes do not have yet the expertise



Mechanical support - essentials

- Support structure
 - 8cm × 66.6cm structure to be made for the intermediate tracker layer (SIT-L2 in CDR)
 - This can in principle host two tiles
 - Cold plate
- Cooling
 - Foam with Ti cooling and facesheet
 - Liverpool FEI4 demonstrator or the Strip stave might be a good starting point
 - Graphite (this was already explored in the UK Ring-0 prototype, see Jon's talk above)

Mechanical support - desirables

- Support structures
 - Space-frame like truss
- Cooling
 - Micro-channel